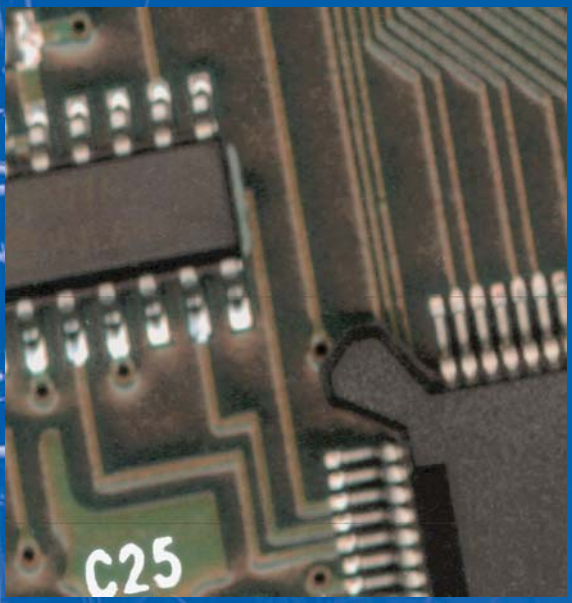
FINAL PROGRAMME

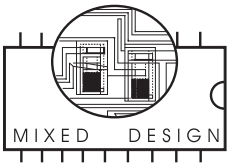
20th International Conference



MIXDES 2013

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

Gdynia, Poland
20 - 22 June 2013



20th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Gdynia, Poland 20 – 22 June 2013

MIXDES 2013 Timetable

Day 1	Thursday, June 20th, 2013		
	Room A	Room B	Room C
8:15	Conference Opening		
8:30	Plenary Session I		
9:30			
9:35	Session 1 (Part 1)	Session 5	Session 3 (Part 1)
10:55	*Coffee Break*		
11:15	Session 1 (Part 2)	Session 6	Sessions 3 (Part 2)
13:00	*Lunch*		
14:00	Introduction to Poster Session		
15:30	Poster Session		
19:00	*Welcome Party*		

Day 2	Friday, June 21st, 2013			
	Room A	Room B	Room C	Room D
8:00	Plenary Session II			
9:30				
9:35	Session 1 (Part 3)	Session 4	Special Session I (Part 1)	Special Session II (Part 1)
10:55	*Coffee Break*			
11:15	Session 1 (Part 4)	IEEE EDS and PAN meeting	Special Session I (Part 2)	Special Session II (Part 2)
12:45	*Lunch*			
14:00	*Tourist Activities*			

Day 3	Saturday, June 22nd, 2013		
	Room A	Room B	Room C
8:30	Plenary Session III		
9:30			
9:35	Session 1 (Part 5)	Session 9 (Part 1)	IEEE SSCS meeting (Part 1)
10:55	*Coffee Break*		
11:15	Session 1 (Part 6)	Session 9 (Part 2) & Session 8	IEEE SSCS meeting (Part 2)
13:00	*Lunch*		
14:00	Session 7 (Part 1)	Session 2 (Part 1)	EDUMEMS project meeting
15:00	*Coffee Break*		
15:20	Session 7 (Part 2)	Session 2 (Part 2)	
19:00	*Closing Ceremony at ship-museum Dar Pomorza*		

FROM THE ORGANISING COMMITTEE

Welcome to the 20th International Conference "Mixed Design of Integrated Circuits and Systems" – MIXDES 2013

We are very happy to meet you this year at the anniversary edition of International Conference "Mixed Design of Integrated Circuits and Systems". It has been 20 years since our first event in Dębe near Warsaw, when 42 people met together to discuss recent advances in VLSI design and technology. This year we are returning for the third time to the beautiful city of Gdynia – a symbol of rebirth of modern Poland after many years of captivity.

The MIXDES conference is one of the largest in the Central Europe in the field, encompassing interdisciplinary research in design, modelling, simulation, testing and manufacturing in various areas, such as micro- and nanoelectronics, semiconductors, sensors, actuators, biomedical applications and power devices. All submissions from 25 countries were reviewed and scored by members of the Programme Committee to put together a high quality technical programme of 116 papers organised in oral and poster presentations.

In addition to the regular programme, there will be six invited papers:

- *A Mixed-Design Technique for Integrated MEMS Using a Circuit Simulator with HDL*
  Hiroshi Toshiyoshi (The University of Tokyo, Japan) et al.
- *BSIM Compact MOSFET Models for SPICE Simulation*
  Yogesh Singh Chauhan (Indian Institute of Technology Kanpur, India) et al.
- *Design and Simulation of ESD-Resistant ICs*
  Valery Axelrad (SEQUOIA Design Systems, Inc, USA)
- *On the Use of Compact Modeling for RF/Analog Design Automation*
  Maria Helena Fino and Fernando Coito (Universidade Nova de Lisboa , Portugal)
- *The Art of Modeling and Predictive Simulation in Power Electronics and Microsystems*
  Gerhard Wachutka (Technische Universität München, Germany)
- *Top-down Drift-diffusion versus Bottom-up Quasi-ballistic Formalism in Device Compact Modeling*
  Xing Zhou (Nanyang Techn. Univ., Singapore) et al.

The program of MIXDES 2013 includes also two special sessions:

- *Compact Modelling for More than Moore*
  organised by Dr. Daniel Tomaszewski (Institute of Electron Technology, Poland) and Dr. Władysław Grabiński (GMC Suisse, Switzerland)
- *xTCA for Instrumentation*
  organised by Dr. Dariusz Makowski, Dr. Adam Piotrowski (Lodz University of Technology, Poland), Dr. Holger Schlarb (DESY, Germany) and Dr. Stefan Simrock (ITER, France)

We would like to take this opportunity to thank many individuals, especially the reviewers, who have worked so hard to make this meeting happen. We hope that you will enjoy your visit to Gdynia and meet us next year in Lviv – a beautiful Ukrainian city with lots of Polish heritage.

Yours Sincerely,
MIXDES 2013 Organising Committee

ORGANISING COMMITTEE

Prof.	A. Napieralski	(Chairman)
Dr.	M. Orlikowski	(Secretary)
Dr.	M. Napieralska	(Vice-Chairman)
Dr.	G. Jabłoński	
Mr.	P. Nowak	Department of Microelectronics and Computer Science,
Dr.	M. Piotrowicz	Lodz University of Technology, Poland
Prof.	J. Zarębski	Department of Marine Electronics,
Prof.	K. Górecki	Gdynia Maritime University, Poland
Prof.	W. Kuźmicz	Institute of Micro- and Optoelectronics, Warsaw University of Technology, Poland

IN COOPERATION WITH

Poland Section IEEE - EDS Chapter

Section of Microelectronics and Section of Signals, Electronic Circuits and Systems of the Committee of Electronics and Telecommunication of the Polish Academy of Sciences

Commission of Electronics and Fotonics of Polish National Committee of International Union of Radio Science - URSI

PROGRAMME COMMITTEE

Prof. M. Adamski	University of Zielona Gora, Poland
Prof. M. Bucher	Technical University of Crete, Greece
Prof. J. Cabestany	Universitat Politecnica de Catalunya, Spain
Prof. J.J. Charlot	Jean Jacques Charlot Consulting, France
Prof. Z. Ciota	Lodz University of Technology, Poland
Prof. J. Collet	LAAS - CNRS, Toulouse, France
Prof. A. Dąbrowski	Poznan University of Technology, Poland
Prof. G. De Mey	University of Ghent, Belgium **(Vice-Chairman)**
Prof. A. De Vos	University of Ghent, Belgium
Prof. J. Deen	McMaster University, Canada
Prof. J.M. Dorkel	LAAS - CNRS, Toulouse, France
Prof. A. Filipkowski	Warsaw University of Technology, Poland
Dr. D. Foty	Gilgamesh Associates, USA
Prof. M. Glesner	Technische Hochschule Darmstadt, Germany
Prof. L. Golonka	Wroclaw University of Technology, Poland
Dr. W. Grabiński	GMC, Switzerland
Prof. A. Handkiewicz	Poznan University of Technology, Poland
Prof. A. Hatzopoulos	Aristotle University of Thessaloniki, Greece
Dr. S. Hausman	Lodz University of Technology, Poland
Prof. A. Jakubowski	Warsaw University of Technology, Poland
Prof. A. Kobus	Institute of Electron Technology, Warsaw, Poland
Prof. A. Kos	AGH University of Science and Technology, Kraków, Poland
Prof. W. Kuźmicz	Warsaw University of Technology, Poland **(Programme Chairman)**
Prof. M. Lobur	Lviv Polytechnical National University, Ukraine
Dr. M.M. Louerat	Université Pierre et Marie Curie, Paris, France
Prof. T. Łuba	Warsaw University of Technology, Poland
Prof. B. Macukow	Warsaw University of Technology, Poland
Prof. J. Madrenas	Universitat Politecnica de Catalunya, Spain
Prof. A. Martinez	LAAS - CNRS, Toulouse, France **(Honorary Chairman)**
Prof. A. Materka	Lodz University of Technology, Poland
Prof. W. Mathis	University of Magdeburg, Germany
Prof. H.S. Momose	Toshiba Corp., Japan
Prof. J.M. Moreno	Universitat Politecnica de Catalunya, Spain
Dr. M. Napieralska	Lodz University of Technology, Poland
Prof. A. Napieralski	Lodz University of Technology, Poland **(General Chairman)**
Prof. J. Nishizawa	Semiconductor Research Institute, Japan
Dr. J.L. Noullet	INSA de Toulouse, France
Prof. M. Ogorzałek	AGH University of Science and Technology, Kraków, Poland
Prof. L. Opalski	Warsaw University of Technology, Poland

Prof.	A. Pfitzner	Warsaw University of Technology, Poland
Dr.	B.F. Romanowicz	Nano Science and Technology Institute, USA
Prof.	J.A. Rubio	Universitat Politecnica de Catalunya, Spain
Prof.	J. Rutkowski	Silesian University of Technology, Poland
Prof.	A. Rybarczyk	Poznan University of Technology, Poland
Dr.	J.-M. Sallese	Swiss Federal Institute of Technology, Switzerland
Prof.	D. Sankowski	Lodz University of Technology, Poland
Prof.	N. Stojadinović	University of Niš, Serbia
Prof.	V. Székely	Technical University of Budapest, Hungary
Prof.	T. Szmuc	AGH University of Science and Technology, Poland
Prof.	G. Szymański	Poznan University of Technology, Poland
Prof.	M. Tadeusiewicz	Lodz University of Technology, Poland
Dr.	D. Tomaszewski	Institute of Electron Technology, Warsaw, Poland
Dr.	P. Tounsi	INSA de Toulouse, France
Dr.	M. Turowski	Robust Chip Inc., USA
Prof.	R. Ubar	Tallinn Technical University, Estonia
Prof.	G. Wachutka	Technische Universitaet Muenchen, Germany
Prof.	K. Wawryn	Technical University of Koszalin, Poland
Prof.	B. Więcek	Lodz University of Technology, Poland
Prof.	S. Yoshitomi	Toshiba Corp., Japan
Prof.	J. Zarębski	Gdynia Maritime University, Poland
Prof.	M. Zubert	Lodz University of Technology, Poland

MAIN TOPICS

1. **Design of Integrated Circuits and Microsystems**
   Design methodologies. Digital and analog synthesis. Hardware-software codesign. Reconfigurable hardware. Hardware description languages. Intellectual property-based design. Design reuse.
2. **Thermal Issues in Microelectronics**
   Thermal and electro-thermal modelling, simulation methods and tools. Thermal mapping. Thermal protection circuits.
3. **Analysis and Modelling of ICs and Microsystems**
   Simulation methods and algorithms. Behavioural modelling with VHDL-AMS and other advanced modelling languages. Microsystems modelling. Model reduction. Parameter identification.
4. **Microelectronics Technology and Packaging**
   New microelectronic technologies. Packaging. Sensors and actuators.
5. **Testing and Reliability**
   Design for testability and manufacturability. Measurement instruments and techniques.
6. **Power Electronics**
   Design, manufacturing, and simulation of power semiconductor devices. Hybrid and monolithic Smart Power circuits. Power integration.

7. **Signal Processing**
   Digital and analog filters, telecommunication circuits. Neural networks. Artificial intelligence. Fuzzy logic. Low voltage and low power solutions.
8. **Embedded Systems**
   Design, verification and applications.
9. **Medical Applications**
   Medical and biotechnology applications. Thermography in medicine.
10. **Student Projects**

CONFERENCE CENTER

The conference will take place in:

Hotel Orbis Gdynia
Armii Krajowej 22
81-372 Gdynia, Poland
Tel. (+48) 586663040, Fax. (+48) 586208651
e-mail: H3417@accor.com
www: http://www.accorhotels.com/gb/hotel-3417-hotel-orbis-gdynia/index.shtml

ACCOMMODATION

The participants will be accommodated at the Conference Center.

REGISTRATION

The standard conference registration fee includes the admission to the conference, a copy of the proceedings CD and other conference materials, tourist activities, all lunches, the welcome party, the banquet, coffee and tea during the breaks. To encourage students to participate in the Conference, the student registration fee is available (welcome party and banquet not included).
The standard registration fee is 350 € or 1450 Złoty. However, the sponsorship allowed organisers to cover part of the fee for IEEE members. For details, please consult the price policy on the Conference web site.
The Book of Abstract and other conference materials will be distributed to participants at the registration desk. The Conference Proceedings CD will be distributed to the participants after the conference. The hardcopy of Conference Proceedings may be ordered during the conference registration at special discount price.

The registration desk will be located in the conference center. It will be working during the following hours:

19 June (Wednesday)	18:00 – 21:00 h
20 June (Thursday)	08:00 – 13:00 h, 14:00 – 18:00 h
21 June (Friday)	08:15 – 12:00 h
22 June (Saturday)	08:30 – 13:00 h, 14:00 – 18:00 h

GENERAL INFORMATION AND INQUIRIES

Dr. Mariusz Orlikowski

Lodz University of Technology
Department of Microelectronics and Computer Science
ul. Wólczańska 221/223 (building B18), 90-924 Łódź, Poland

e-mail: mixdes2013@dmcs.p.lodz.pl tel.: +48 (0) 604397239
www: http://www.mixdes.org fax: +48 (0) 426360327

THE CITY OF GDYNIA

We would like to invite you to Gdynia, the town which is sometimes called the sea capital of Poland. No other Polish town, and only few European cities, have such a long seafront and easy access to sea. It is some 12.5 km long, not counting the port area. Just strolling along the sea one can admire one of the largest sailing ships Dar Pomorza, built in 1930, which was recognised as the Most Beautiful White Frigate! For those who are not interested in ships there are wonderful opportinities to watch wildlife in the Sea Aquarium or in wildlife reserve Redłowska Kepa - the steep and high coast cut by ravines. In the reserve, high above the sea there is a beautiful mixed forest where one can find unique trees from Scandinavian woods whose seeds travelled across the Baltic Sea from Sweden. Although Gdynia was built in the 20th century, it possesses a few historical monuments including the Church of Saint Michael Archangel in Oksywie built in 1224 by the Norbertine nuns.

Gdynia is also a great city for shopping. The most attractive places for spending your money are Starowiejska and Świętojańska streets. There is also a modern and exclusive shopping center named „Batory", at the intersection of 10 Lutego and Władysława IV streets, More information is available on: **http://guide.trojmiasto.pl**

TOURIST ACTIVITIES

We would like to invite you to take the three-hour cruise on the Bay of Gdansk with a ship stylized on XVII century galleon.

During the trip you will get acquainted with a rich History of Gdynia and Gdansk and see the places, connected with the cities history, and a guide will tell some interesting facts about them. Those will be: Gdansk Shipyard, Wisloujscie Fortress and Westerplatte, where II World War began.

The boarding will start at 14:00 in Gdynia.

IMPORTANT PHONE NUMBERS

Ambulance	999	Fire Brigade	998
Police	997	Emergency phone	112

BANKING

Foreign exchange facilities are available at major airports and at larger hotels, as well as in many private offices, called “Kantor”. Credit cards can be used in many places such as banks, hotels, car-rental offices, restaurants, and large shops. Approximate currency exchange rate: 1 € = 4.3 złoty, 1 $ =3.3 złoty (for the up-to--date information refer to **http://www.nbp.pl**).

Credit cards:
Visa, American Express, MasterCard are the most common cards. However, other cards might be accepted.

Currency:
Generally, everywhere in Poland you pay in Polish zlotys. The currency units are złoty (zł, PLN) and grosz (gr), 1 zł = 100 gr. The Polish zloty is a fully convertible currency internally in Poland.

TRANSPORT

Gdynia is a city in the Pomeranian Voivodship of Poland and an important seaport at Gdansk Bay on the south coast of the Baltic Sea. Gdynia is part of a conurbation with the spa town of Sopot, the city of Gdańsk and suburban communities, which together form a metropolitan area called the Tricity with a population of over a million people. These cities, especially Gdańsk located 17 km from Gdynia, are a major, international transport junction. This is confirmed by the full range of transport opportunities the city possesses: road, rail, maritime, river and air transport.

Gdynia can be reached by train or road, you can also use Gdańsk Lech Walesa Airport. There are several direct busses from Warsaw to Gdynia.

There are also direct trains from Warszawa Centralna Station to Gdynia Główna Station, as shown below (seat reservation is obligatory):

Number	**38202**	**35202**	**15101**	**38108**	**35108**	**38108**	**15103**	**35106**
Runs	daily	daily	daily	daily	daily	daily	daily	daily
Train type	TLK fast	TLK fast	TLK fast	TLK fast	TLK fast	TLK fast	TLK fast	TLK fast
Warszawa	22:30	4:21	6:00	8:11	12:55	14:05	16:20	17:59
Gdynia	5:38	11:58	11:27	15:13	19:57	19:46	21:50	0:57

You can also use one of the international train arriving to Gdynia from Berlin:

Number	**555**
Runs	daily
Train type	EuroCity
Berlin Hbf.	15:37
Gdynia	22:39

Planes are available from Warszawa Airport to Gdańsk Airport as shown:

Runs	**Mo-Fr**	**Mo-Fr, Su**	**Mo-Sa**	**Mo-Fr, Su**	**Mo-Th, Sa-Su**	**daily**	**daily**
Warszawa	7:20	11:10	14:45	15:45	15:45	19:40	22:40
Gdynia	8:20	12:10	15:35	16:45	16:50	20:40	23:40

Planes are also available from a number of european cities to Gdańsk Airport. One can reach Gdańsk from Amsterdam, Kraków, Wrocław (by Eurolot), Frankfurt, Munich (by LOT and Lufthansa), Oslo (by Norwegian Air Shuttle), Berlin (by Air Berlin) and Copenhagen (by SAS). Also low cost airlines - WizzAir and Ryanair - operate from Gdańsk Airport in several directions. See http://www.airport.gdansk.pl/ for details.

The Centre of Gdynia (Gdynia Główna Railway Station) can be reached from airport by ZKM bus nr 510 (special fare 4.00 PLN, runs about 40 minutes) or by TAXI.

To travel Gdynia you can use the city public transport. One ticket is valid in one bus or trolleybus - in case of change one should use 2 tickets or hourly ticket.

Validity period	**Price of ticket**	
	Standard lines	**Fast lines, Night lines**
Single fare	3.00 PLN	4.00 PLN
Form Airport (510)	NA	4.00 PLN
One hour	3.60 PLN	4.60 PLN
24h	12.00 PLN	

The main conference building (ORBIS HOTEL) is about 20 minutes on foot from the Gdynia Główna train station. One should take the bus number 21 (direction SOPOT REJA, leave at 4th stop), 23 (direction KACZE BUKI, leave at 5th stop), 24 (direction DĄBROWA MIĘTOWA, leave at 5th stop), 25 or 28 (direction 3 MAJA – HALA, leave on 2nd stop) or 105 (direction REDŁOWO SZPITAL, leave at 2nd stop). TAXI from the station are also available.

PROGRAMME OF THE CONFERENCE

The programme of the MIXDES 2013 Conference will include oral presentations of contributed and invited papers, special sessions and poster session.
Except for the plenary and poster sessions, the programme of the conference will be divided into three parallel sessions, in accordance with discussed topics. The language of the Conference is English, neither translation nor interpretation will be provided.

The time of oral presentations:

- for invited papers: 20-25 min. for presentation and 5-10 min. for questions,
- for regular papers: 15 min. for presentation and 5 min. for questions.

Poster presentations:
The authors presenting their papers at the poster sessions will have at their disposal an A0 panel. Adhesive tape and scissors will be provided by organisers. During the first conference day, an introduction to poster session is planned, in which the authors are asked to present their work very shortly in front of the audience: 2-3 slides, within 1-2 minutes. The questions and discussions will be continued at the poster panels.

Lunches:
Lunches will be served each day at the conference center at the times indicated in the programme.

Welcome Party and Conference Banquet:
The Welcome Party will be organised after the Poster Session at the conference site. The Closing Ceremony and the Conference Banquet will be organised on "Dar Pomorza", a famous Polish sailing frigate, currently preserved in Gdynia as a museum ship.
The Welcome Party and the Conference Banquet are not included in the student registration fee.

WEATHER

June in Poland is generally sunny, with some showers, the temperatures can be typically 15 to 28 ˚C during days. During nights, the temperature can go down to 8-10 ˚C. So, we can suggest you to bring summer clothes, with a quite warm jacket or pullover, and an umbrella.

First Day: June 20th 2013 (Thursday)

Time — Room A

08:15 Conference opening
Chairmen: Prof. W. Kuźmicz, Prof. G. De Mey and Prof. A. Napieralski

08:30 Plenary Session I
Chairman: Prof. G. De Mey

A Mixed-Design Technique for Integrated MEMS Using a Circuit Simulator with HDL
H. Toshiyoshi (The Univ. of Tokyo, JAPAN), T. Konishi, K. Machida (NTT Advanced Techn. Corp., JAPAN), K. Masu (Tokyo Inst. of Techn., JAPAN)

Top-down Drift-diffusion versus Bottom-up Quasi-ballistic Formalism in Device Compact Modeling
X. Zhou, J. Zhang, B. Syamal, Z. Zhu, H. Zhou, S.B. Chiah (Nanyang Techn. Univ., SINGAPORE)

09:35 Session 1 (Part 1): Design of Integrated Circuits and Microsystems
Chairman: Prof. M. Bucher

A Circuit Implementation of an Ultra High Speed, Low Power Analog Fully Programmable MFG
M. Tohidi, A. Abolhasani, M. Mousazadeh, A. Khoei, K. Hadidi (Urmia Univ., IRAN)

A Continuous-Time Instrumentation Amplifier Employing a Novel Auto-Zeroing Structure
S. Marechal (EPFL, SWITZERLAND), O. Nys (Semtech Neuchâtel Sàrl, SWITZERLAND), F. Krummenacher (EPFL, SWITZERLAND), M. Chevroulet (Semtech Neuchâtel Sàrl, SWITZERLAND), M. Kayal (EPFL, SWITZERLAND)

A Flip-Flop Implementation for the DPA-Resistant Delay-Based Dual-Rail Pre-Charge Logic Family
S. Bongiovanni, M. Olivieri, G. Scotti, A. Trifiletti (Sapienza Univ. of Rome, ITALY)

A High Speed and Fully Tunable MFG with New Programmable CMOS OTA and New MIN Circuit
A. Abolhasani, M. Tohidi, M. Mousazadeh, A. Khoei, K. Hadidi (Urmia Univ., IRAN)

10:55 Coffee Break

11:15 Session 1 (Part 2): Design of Integrated Circuits and Microsystems
Chairman: Prof. Z. Ciota

A Simple 1 GHz Non-Overlapping Two-Phase Clock Generators for SC Circuits
B. Nowacki, N. Paulino, J. Goes (Univ. Nova de Lisboa, PORTUGAL)

Amplifier Structures in High-voltage SoI Processes
M. Jankowski, A. Napieralski (Lodz Univ. of Techn., POLAND)

An Analog Dual Delay Locked Loop Using Coarse and Fine Programmable Delay Elements
J. Jasielski, S. Kuta, W. Machowski (AGH Univ. of Science and Techn., POLAND), W. Kołodziejski (Higher Vocational School in Tarnow, POLAND)

Automated Design of Switched Current Sigma-Delta Modulator with a New Comparator Structure
P. Śniatała (Poznan Univ. of Techn., POLAND)

13:00 Lunch

14:00 Poster Session
Chairman: Prof. W. Kuźmicz

4-D Fuzzy Connectedness-Based Medical Image Segmentation Technique
J. Czajkowska (Univ. Siegen, GERMANY and Silesian Univ. of Techn., POLAND), J. Kawa (Silesian Univ. of Techn., POLAND), Z. Czajkowski, M. Grzegorzek (Univ. Siegen, GERMANY)

A Note on Fractional-Order Two-Terminal Devices in Filtering Applications
J. Petrzela (Brno Univ. of Techn., CZECH REPUBLIC)

A Simple Method for Extraction of Threshold Voltage of FD SOI MOSFETs
G. Gluszko, D. Tomaszewski, J. Malesinska, K. Kucharski (Inst. of Electron Technology, POLAND)

An Optimized Algorithm for Recognition of Complex Patterns Based on Artificial Neural Network (student project)
P. Gurzyński (Univ. of Computer Sciences and Skills, POLAND), T. Talaśka, R. Długosz (UTLS Bydgoszcz, POLAND), A. Świetlicka (Poznan Univ. of Techn., POLAND)

Application of a Genetic Algorithm for Dimension Optimization of the MEMS-based Accelerometer
M. Melnyk, A. Kernytskyy, M. Lobur (Lviv Polytechnic National Univ., UKRAINE), M. Szermer, P. Zając, W. Zabierowski (Lodz Univ. of Techn., POLAND)

Application of Hilbert-Huang Transform to Engine Knock Detection
J. Fiołka (Silesian Univ. of Techn., POLAND)

Architecture Design of the High Integrated System-on-Chip for Biomedical Applications
K. Różanowski (Military Inst. of Aviation Medicine, POLAND), T. Sondej (Military Univ. of Techn., POLAND)

Autonomous Wireless Sensor Network for Greenhouse Environmental Conditions Monitoring
B. Pękosławski, P. Krasiński, M. Siedlecki, A. Napieralski (Lodz Univ. of Techn., POLAND)

Behavioral Parameterized SPICE Models of Photovoltaic Modules
E. Gadjeva, M. Hristov (Tech. Univ. Sofia, BULGARIA)

Classification Support Algorithms for Patient's General Condition Based on Artificial Neural Network
P. Marciniak, Z. Ciota, R. Kotas (Lodz Univ. of Techn., POLAND)

Comparative Analysis of Pseudo Random Signals of the LFSR and DLFSR Generators (student project)
R. Stępień, J. Walczak (Silesian Univ. of Techn., POLAND)

Design of Wide Band OOK Transmitter for Biomedical Applications
P. Turcza, J. Młynarczyk (AGH Univ. of Science and Techn., POLAND)

Efficient Image Processing Application Using Residue Number System
D. Younes, P. Steffan (Brno Univ. of Techn., CZECH REPUBLIC)

Influence of Delay Mismatch on Digital Predistortion for Power Amplifiers
T. Götthans (Univ. Paris-Est, FRANCE and Brno Univ. of Techn., CZECH REPUBLIC), G. Baudoin, A. Mbaye (Univ. Paris-Est, FRANCE)

Laboratory Setup for Investigation of MPPT Algorithms of Photovoltaic Modules under Non-uniform Insolation (student project)
D. Moreno Galan (Univ. Politècnica de Catalunya, SPAIN), T. Torzewicz, Ł. Starzak, M. Piotrowicz, W. Marańda (Lodz Univ. of Techn., POLAND)

Medicament Dispensation System with Patient Supervision (student project)
P. Krasiński, K. Kowalczyński, B. Pękosławski, A. Napieralski (Lodz Univ. of Techn., POLAND)

OctaLynx D: RISC Microprocessor Dedicated for Dynamic Thermal Management
M. Frankiewicz, R. Gał, A. Gołda, A. Kos (AGH Univ. of Science and Techn., POLAND)

Optimized Architecture of High Order CIC Filters
M. Pristach, M. Pavlik, J. Haze, L. Fujcik (Brno Univ. of Techn., CZECH REPUBLIC)

Project and Realization of a Two-Wheels Balancing Vehicle (student project)
P. Bethke (Univ. of Computer Sciences and Skills, POLAND), R. Długosz, T. Talaśka (UTLS Bydgoszcz, POLAND)

Smartphone Application for Automatic Classification of Environmental Sound
M. Mielke, R. Brück (Univ. Siegen, GERMANY)

Software Development for uTCA-based LLRF Control System
A. Piotrowski (Lodz Univ. of Techn., POLAND)

Tests of a Readout Front-end Electronics for a Pixel Detector Based on Inverter Amplifier
R. Kłeczek, P. Gryboś (AGH Univ. of Science and Techn., POLAND)

The DC Measurement Method of Thermal Resistance of IGBTs
K. Górecki, P. Górecki (Gdynia Maritime Univ., POLAND)

The Sundial Based Sun-Tracking System with AVR Microcontroller (student project)
M. Amirpour, M. Mousazadeh, M. Tohidi, K. Hadidi (Urmia Univ., IRAN)

15:30 Coffee break during Poster Session

19:00 Welcome Party

Time **Room B**

09:35 Session 5 : Testing and Reliability
Chairman: Prof. W. Pleskacz

A Logic Level Countermeasure Against CPA Side Channel Attacks on AES
R. Menicocci, A. Trifiletti, F. Trotta (Sapienza Univ. of Rome, ITALY)

On In-System Programming of Non-volatile Memories
A. Tsertov (Tallinn Univ. of Techn., ESTONIA), S. Devadze, A. Jutman, A. Jasnetski (Testonica Lab, ESTONIA)

Reliability Study on Technology Trends Beyond 20nm
E. Amat, A. Calomarde, A. Rubio (Univ. Politècnica de Catalunya, SPAIN)

10:55 Coffee Break

11:15 Special Session 6 : Power Electronics
Chairman: Prof. G. Wachutka

A Single-chip Vertical Integration Approach Suitable for Medium Power Switching Cells and Converters
A. El Khadiry, A. Bourennane, M. Breil (LAAS-CNRS and Univ. Toulouse, FRANCE), F. Richardeau (LAPLACE and Univ. Toulouse, FRANCE)

Analysis in Commutation of a New High Voltage Thyristor Structure for High Temperature
G. Toulon, A. Bourennane, K. Isoird (LAAS-CNRS, FRANCE)

Calculation of Dynamic MPP-Tracking Efficiency of PV-Inverter Using Recorded Irradiance
W. Marańda, M. Piotrowicz (Lodz Univ. of Techn., POLAND)

Parameter Estimation of the Electrothermal Model of the Ferromagnetic Core
K. Górecki, M. Rogalska, J. Zarębski (Gdynia Maritime Univ., POLAND)

Report on Efficiency of Field-Installed PV-Inverter with Focus on Radiation Variability
M. Piotrowicz, W. Marańda (Lodz Univ. of Techn., POLAND)

SiC Power JFET Electrothermal Macromodel
F. Masana, J. Chavarría, D. Biel, A. Poveda, F. Guinjoan, E. Alarcón (Univ. Politècnica de Catalunya, SPAIN)

13:00 Lunch

Time	Room C

09:35 Session 3 (Part 1): Analysis and Modelling of ICs and Microsystems
Chairman: Prof. A. Rybarczyk

A Discrete Model of the DC Charge-up Phase in RFID Rectifiers
H. Rabén, J. Borg, J. Johansson (Luleå Univ. of Techn., SWEDEN)

An Analysis of Full Adder Cells for Low-Power Data Oriented Adders Design
I. Brzozowski, D. Pałys, A. Kos (AGH Univ. of Science and Techn., POLAND)

Analythical Characterization of Variable Width Integrated Spiral Inductors (student project)
F. Passos, M.H. Fino (Univ. Nova de Lisboa, PORTUGAL), E.R. Moreno (CSIC-IMSE, SPAIN)

Characterization of Transistors Fabricated in Evolving Lapis Semiconductor Silicon-on-Insulator 0.2μm Technology
S. Głąb, M. Baszczyk, P. Dorosz, W. Kucewicz, M. Sapor (AGH Univ. of Science and Techn., POLAND), Ł. Mik (PWSZ Tarnow, POLAND)

10:55 Coffee Break

11:15 Session 3 (Part 2): Analysis and Modelling of ICs and Microsystems
Chairman: Prof. A. Dąbrowski

Closed-loop Oscillator Circuit for Piezoresistive Carbon Nanotube NEMS Resonators
C. Kauth, M. Pastre, M. Kayal (EPFL, SWITZERLAND)

Power Network Transient Stability Electronics Emulator Using Mixed-Signal Calibration
G. Lanz, L. Fabre, G. Lilis, T. Kyriakidis, D. Sallin, R. Cherkaoui, M. Kayal (EPFL, SWITZERLAND)

Sensitivity Simulative Evaluation Methodology in 315/433MHz RKE System
M. Jableka, H. Niemiec, A. Ryszko, T. Klatka, M. Szelest (Delphi Poland S.A., POLAND), G. Jiang (Delphi - Kokomo Technical Center, USA)

Variability-aware Gradual Aging for Generating Reliability Figures of a Neural Measurement System
N. Hellwege, N. Heidmann, D. Peters-Drolshagen, S. Paul (Univ. Bremen, GERMANY)

13:00 Lunch

Second day: June 21st 2013 (Friday)

Time **Room A**

08:00 Plenary Session II
Chairman: Prof. W. Kuźmicz

BSIM Compact MOSFET Models for SPICE Simulation
Y.S. Chauhan (Indian Inst. of Techn. Kanpur, INDIA), S. Venugopalan, C.C. Hu, N. Paydavosi (Univ. of California Berkeley, USA), P. Kushwaha (Indian Inst. of Techn. Kanpur, INDIA), S. Jandhyala, J.P. Duarte (Univ. of California Berkeley, USA), S. Agnihotri, C. Yadav, H. Agarwal (Indian Inst. of Techn. Kanpur, INDIA), A. Niknejad (Univ. of California Berkeley, USA)

Design and Simulation of ESD-Resistant ICs
V. Axelrad (SEQUOIA Design Systems, Inc, USA)

Industrialization and Application of the New Crate Standard MTCA.4
H. Schlarb (DESY, GERMANY)

09:35 Session 1 (Part 3): Design of Integrated Circuits and Microsystems
Chairman: Prof. J.M. Moreno

Architecture and Simulation Results of a High-Speed Multichannel Integrated Circuit for Optical Radiation Sensors
Ł. Kotynia, A. Napieralski (Lodz Univ. of Techn., POLAND)

Cascode Amplifiers with Low-Gain Variability Using Body-Biasing Temperature and Supply Compensation
N. Pereira, L.B. Oliveira, J. Goes, J. Oliveira (Univ. Nova de Lisboa, PORTUGAL)

CMOS Implementation of a New High Speed, Glitch-Free 5-2 Compressor for Fast Arithmetic Operations
M. Tohidi, M. Mousazadeh, K. Hadidi, A. Khoei (Urmia Univ., IRAN)

Computer-Aided Detection of Plagiarism in Integrated-Circuit Layouts
D. Kasprowicz, H. Wada (Warsaw Univ. of Techn., POLAND)

10:55 Coffee Break

11:15 Session 1 (Part 4): Design of Integrated Circuits and Microsystems
Chairman: Prof. Z. Ciota

Development of Ionizing Radiation Detectors Integrated with Readout Electronics
D. Obrębski, A. Szymański, D. Tomaszewski, M. Grodner, J. Marczewski (Institute of Electron Techn., POLAND), J. Pieczyński (Fraunhofer Institute IMS, GERMANY)

Double Feedforward 0.6 V LNA with High Gain and Low Noise Figure
J. Oliveira, I. Bastos, L.B. Oliveira, J. Goes (Univ. Nova de Lisboa, PORTUGAL), M. Silva (INESC-ID Lisboa, PORTUGAL)

Dual Stage Charge-Sensitive Amplifier with Constant-Current Feedback for Time-over-Threshold Processing Dedicated for Silicon Strip Detectors
K. Kasiński, R. Kłeczek, P. Gryboś, R. Szczygieł (AGH Univ. of Science and Techn., POLAND)

Wide-Frequency-Range Low-Power Variable-Length Ring Oscillator in UMC CMOS 0.18µm
M. Frankiewicz, A. Kos (AGH Univ. of Science and Techn., POLAND)

12:45 Lunch

14:00 Tourist Activities

Time **Room B**

09:35 Session 4: Microelectronics Technology and Packaging
Chairman: Prof. A. Napieralski

Beam Intensity Measurements in the Large Hadron Collider (student project)
M. Krupa (CERN, SWITZERLAND and Lodz Univ. of Techn., POLAND), L. Soby (CERN, SWITZERLAND)

Comparison of Commercial Brands of PEDOT:PSS in Electric "Capattery" Integrated in Textile Structure
S. Odhiambo, G. De Mey (Ghent Univ., BELGIUM), W. Deferme, J. Stryckers (Hasselt Univ., BELGIUM), L. Van Langenhove, C. Hertleer (Ghent Univ., BELGIUM)

Design Space of Twin Gate Junctionless Vertical Slit Field Effect Transistors
L. Barbut, F. Jazaeri, D. Bouvet, J.-M. Sallese (EPFL, SWITZERLAND)

Heavily Doped Junctionless Vertical Slit FETs with Slit Width below 20 nm
L. Barbut, F. Jazaeri, D. Bouvet, J.-M. Sallese (EPFL, SWITZERLAND)

10:55 Coffee Break

11:15 IEEE EDS and PAN meeting

12:45 Lunch

Time **Room C**

09:35 Special Session I (Part 1): Compact Modeling for More than Moore
Chairmen: Prof. M. Bucher and Dr. D. Tomaszewski

Low-Power RF Modeling of a 40nm CMOS Technology Using BSIM6
M.-A. Chalkiadaki, C.C. Enz (EPFL, SWITZERLAND)

A Swept Parameter Technique for Statistical Circuit Simulation
M. Brinson (London Metropolitan Univ., UK)

Modeling of a THz Radiation Detector Built of Planar Antenna Integrated with MOSFET
P. Kopyt (Warsaw Univ. Tech., POLAND)

Unified Charge Model for Short-Channel Junctionless Double Gate MOSFETs
T. Holtij, M. Graef, F. Hain, A. Kloes (Tech. Hochschule Mittelhessen, GERMANY), B. Iniguez (Univ. Rovira i Virgili, SPAIN)

10:55 Coffee Break

11:15 Special Session I (Part 2): Compact Modeling for More than Moore
Chairmen: Prof. M. Brinson and Dr. D. Tomaszewski

Two-dimensional Physics-based Modeling of Electrostatics and Band-to-Band Tunneling in Tunnel-FETs
M. Graef, T. Holtij, F. Hain, A. Kloes (Tech. Hochschule Mittelhessen, GERMANY), B. Iniguez (Univ. Rovira i Virgili, SPAIN)

Characteristic Parameters Evaluation of Hall Cells with High Performance
M.-A. Paun, J.-M. Sallese, M. Kayal (EPFL, SWITZERLAND)

A Compact Model of AlGaN/GaN HEMTs Power Transistors Based on a Surface-Potential Approach
P. Martin, L. Lucci (CEA-LETI, FRANCE)

A Compact Model of VES-BJT Device
W. Kuźmicz, P. Mierzwiński (Warsaw Univ. of Techn., POLAND)

A Simple Method for Extraction of Threshold Voltage of FD SOI MOSFETs
G. Gluszko, D. Tomaszewski, J. Malesinska, K. Kucharski (Inst. of Electron Technology, POLAND)

12:45 Lunch

Time **Room D**

09:35 Special Session II (Part 1): xTCA for Instrumentation
Chairman: Dr. Dariusz Makowski

MTCA.4 Based LLRF System for the European XFEL
J. Branlard, G. Ayvazyan, V. Ayvazyan, M. Grecki, M. Hoffmann, T. Jeżyński, F. Ludwig, U. Mavrič, S. Pfeiffer, H. Schlarb, C. Schmidt, H. Weddig, B. Yang (DESY, GERMANY), P. Barmuta, S. Bou Habib, Ł. Butkowski, K. Czuba, M. Grzegrzółka, E. Janas, J. Piekarski, I. Rutkowski, D. Sikora, Ł. Zembala, M. Żukociński (Warsaw Univ. of Techn., POLAND), W. Cichalewski, W. Jałmużna, D. Makowski, A. Mielczarek, A. Napieralski, P. Perek, A. Piotrowski, T. Poźniak, K. Przygoda (Lodz Univ. of Techn., POLAND), M. Kudła, J. Szewiński (National Centre for Nuclear Research, POLAND), K. Oliwa, W. Wierba (Polish Academy of Sciences, POLAND)

Femtosecond Precision via RF Backplane in MTCA Crates
K. Czuba, A. Łysiuk (Warsaw Univ. of Techn., POLAND), P. Barmuta (Warsaw Univ. of Techn., POLAND and Katholieke Univ. Leuven, BELGIUM), T. Jeżyński (DESY, GERMANY), T. Leśniak (Warsaw Univ. of Techn., POLAND), F. Ludwig, H. Schlarb (DESY, GERMANY)

Management Funtionality Extension for RTM and eRTM in MTCA.4 Crates
T. Jeżyński (DESY, GERMANY)

MTCA Fast Digitizer for Direct RF Measurements
S. Bou Habib (Warsaw Univ. of Techn., POLAND)

MTCA.4 Compliant Piezo Driver RTM for Laser Synchronization
K. Przygoda (Lodz Univ. of Techn., POLAND), M. Felber, H. Schlarb (DESY, GERMANY)

10:55 Coffee Break

11:15 Special Session II (Part 2): xTCA for Instrumentation
Chairman: Dr. Adam Piotrowski

Design and Preliminary Evaluation of Integrated Radiation Spectrometer for Longitudinal e-Bunch Diagnostics at FELs
G. Jabłoński, Ł. Kotynia, D. Makowski, A. Mielczarek, P. Perek, A. Napieralski (Lodz Univ. of Techn., POLAND), B. Steffen (DESY, GERMANY)

Diagnostic Use Case Examples for ITER Plant Instrumentation and Control
S. Simrock (ITER, FRANCE)

AMC Frame Grabber Module with PCIe Interface
A. Mielczarek, P. Perek, D. Makowski, M. Orlikowski, G. Jabłoński, A. Napieralski (Lodz Univ. of Techn., POLAND)

Software Components of MTCA-based Image Acquisition System
P. Perek, M. Orlikowski, G. Jabłoński, A. Mielczarek, D. Makowski (Lodz Univ. of Techn., POLAND), K. Zagar, S. Isaev (COSYLAB, SLOVENIA)

12:45 Lunch

Day 3: June 22nd 2013 (Saturday)

Time **Room A**

08:30 Plenary Session III
Chairman: Prof. A. Napieralski

On the Use of Compact Modeling for RF/Analog Design Automation
M.H. Fino, F. Coito (Univ. Nova de Lisboa, PORTUGAL)

The Art of Modeling and Predictive Simulation in Power Electronics and Microsystems
G. Wachutka (Tech. Univ. München , GERMANY)

09:35 Session 1 (Part 5): Design of Integrated Circuits and Microsystems
Chairman: Prof. J. Cabestany

Design and Measurements Results of 7-bit Low-Power, Low Area SAR A/D Converter for Pixel Systems
P. Otfinowski, P. Gryboś (AGH Univ. of Science and Techn., POLAND)

FPGA Implementation of Hybrid Fixed Point - Floating Point Multiplication
A. Amaricai, O. Boncalo, O. Sicoe, M. Marcu (Politeh. Univ. of Timisoara, ROMANIA)

Gain Enhancement and Input Parasitic Capacitance Reduction of Single-Stage OTAs by Using Differential Voltage Combiners
R. Santos-Tavares, E. Santin, R. Lopes, J. Oliveira, J. Goes (Univ. Nova de Lisboa, PORTUGAL)

NRSD8 - Neural Recording and Spike Detection Multichannel Integrated Circuit Designed in 180nm CMOS Technology
P. Kmon (AGH Univ. of Science and Techn., POLAND)

10:55 Coffee Break

11:15 Session 1 (Part 6): Design of Integrated Circuits and Microsystems
Chairman: Prof. A. Kobus

Design of CMOS Analog Integrated Readout Circuit for NMOS THz Detectors
C. Kołaciński, D. Obrębski (Institute of Electron Techn., POLAND)

Technology Migration of Analogue CMOS Circuits Using Hooke-Jeeves Algorithm and Genetic Algorithms in Multi-Core CPU Systems
M. Naumowicz, M. Melosik, P. Katarzyński (Poznan Univ. of Techn., POLAND)

Universal Design Method of n-to-2^n Decoders
I. Brzozowski, Ł. Zachara, A. Kos (AGH Univ. of Science and Techn., POLAND)

Video Scaling Processor Targeted for Low-Power Applications
M. Bogusz, D. Modrzyk (Evatronix SA, POLAND)

High Input- and Output-impedance Functionality Implementation in HV SoI Voltage Buffers
M. Jankowski, A. Napieralski (Lodz Univ. of Techn., POLAND)

13:00 Lunch

14:00 Session 7 (Part 1): Signal Processing
Chairman: Prof. A. Dąbrowski

Hardware Implementation of the PBAS Foreground Detection Method in FPGA
T. Kryjak, M. Komorkiewicz, M. Gorgon (AGH Univ. of Science and Techn., POLAND)

A Method of Initial Search Region Reduction for Acoustic Localization in Distributed Systems
S. Astapov, J. Berdnikova, J.-S. Preden (Tallinn Univ. of Techn., ESTONIA)

Digital Fractional-order Control of a Position Servo
A. Tepljakov, E. Petlenkov, J. Belikov, S. Astapov (Tallinn Univ. of Techn., ESTONIA)

15:00 Coffee Break

15:20 Session 7 (Part 2): Signal Processing
Chairman: Prof. Z. Ciota

Fast Prototyping of Automatic Real-time Event Detection Facilities for Video Monitoring Using DSP Module
T. Marciniak, A. Chmielewska, R. Weychan, A. Dąbrowski (Poznan Univ. of Techn., POLAND)

High Performance FPGA-based Implementation of a Parallel Multiplier-Accumulator
M. Cieplucha (Warsaw Univ. of Techn., POLAND)

Mobile Robot Platform for Real-Time Search Algorithms (student project)
J. Pochmara, R. Koppa, K. Kamiński, W. Grygiel
(Poznan Univ. of Techn., POLAND)

19:00 Closing Ceremony at ship-museum Dar Pomorza

Time **Room B**

09:35 Session 9 (Part 1): Medical Applications
Chairman: Prof. A. Pfitzner

A 2.3-dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz (student project)
R. Borrego, J. Oliveira, J. Goes (Univ. Nova de Lisboa, PORTUGAL)

Application of Olfactory Event-Related Potentials for Diagnosis of Neurodegenerative Diseases
Z. Ciota, R. Kotas, A. Napieralski (Lodz Univ. of Techn., POLAND)

FATE: One Step Towards an Automatic Aging People Fall Detection Service
J. Cabestany, J.M. Moreno, C. Perez, A. Sama, A. Catala (Univ. Politècnica de Catalunya, SPAIN)

Mobile Device for Quantitative Sensory Testing (student project)
J. Mruczkiewicz, K. Plec, M. Majchrzycki, A. Rybarczyk (Poznan Univ. of Techn., POLAND)

10:55 Coffee Break

11:15 Session 9 (Part 2) & Session 8: Medical Applications & Embedded Systems
Chairman: Prof. J.M. Moreno

Optimization Model for Risk Stratification of Sudden Cardiac Death
M. Kamiński, R. Kotas, P. Mazur, B. Sakowicz, A. Napieralski (Lodz Univ. of Techn., POLAND)

REMPARK: When AI and Technology Meet Parkinson Disease Assessment
J. Cabestany, C. Perez, J.M. Moreno, A. Sama (Univ. Polite`cnica de Catalunya SPAIN), A. Bayes (C.M. Teknon, SPAIN), A. Rodriguez (Nat. Univ. Galway, IRELAND)

System for Multichannel Recording of the Electrophysiological Activity of a Brain Tissue In-Vivo
M. Żołądź, P. Kmon, J. Rauza, P. Gryboś (AGH Univ. of Science and Techn., POLAND), T. Błasiak (Jagiellonian Univ., POLAND)

Analysis of Timing Resources for Highly Predictable Real-Time Systems Models
Ł. Golly, A. Pułka (Silesian Univ. of Techn., POLAND)

IEEE 802.15.4 Wireless Network Application in Real-Time Automation Systems
P. Krasiński, B. Pękosławski, A. Napieralski (Lodz Univ. of Techn., POLAND)

13:00 Lunch

14:00 Session 2 (Part 1): Thermal Issues in Microelectronics
Chairman: Prof. J. Zarębski

A Set of Temperature Sensors and Maximum Temperature Selection Circuit
A. Gołda, A. Kos (AGH Univ. of Science and Techn., POLAND)

Distributed Electrothermal Modeling Methodology for MOS Gated Power Devices Simulations
E. Marcault, J.-L. Massol, P. Tounsi, J.-M. Dorkel (LAAS-CNRS, FRANCE)

Extension of Thermal Influence Coefficients Method to Frequency Domain
K. Gnidzińska, G. Jabłoński, A. Napieralski (Lodz Univ. of Techn., POLAND), G. De Mey (Ghent Univ., BELGIUM)

Influence of Scaling on IC Temperature in FinFET Microprocessor Technologies
M. Janicki, P. Zając, M. Szermer, A. Napieralski (Lodz Univ. of Techn., POLAND)

15:00 Coffee Break

15:20 Session 2 (Part 2): Thermal Issues in Microelectronics
Chairman: Prof. G. Wachutka

Measuring System for Determining Thermal Parameters of Semiconductor Devices
J. Zarębski, K. Górecki, J. Dąbrowski (Gdynia Maritime Univ., POLAND)

Numerical Modeling of Passive Low Temperature Co-fired Ceramics Coolers Using Design of the Experiment
D. Jurków (Wrocław Univ. of Techn., POLAND)

Parameter-based Temperature-Controlled Oscillator Driven by Optimum Control of Throughput Method
A. Gołda, A. Kos (AGH Univ. of Science and Techn., POLAND)

Time	Room C
09:35	IEEE SSCS kick off meeting (Part 1)
10:55	Coffee Break
11:15	IEEE SSCS kick off meeting (Part 2)
13:00	Lunch
14:00	EDUMEMS Project meeting

Kick off meeting of the
IEEE Solid-State Circuits Society Poland Chapter

We invite everybody who is interested in working within Poland Section of Solid-State Circuit Society Chapter for a kick-off meeting. The meeting will take place during 20th International Conference MIXDES 2013.

Place: Conference Venue: Hotel Orbis Gdynia (room C)
Armii Krajowej 22, Gdynia, Poland

June 22nd 2013 (Saturday)

Time	Room C
9:35	**Meeting opening, Session part 1** P. Gryboś, R. Kumar, M. Ogorzałek
	Challenges and Innovation Opportunities in Semiconductors R. Kumar (President & CEO, TCX Technology Connexions, USA)
	3D Integration for Circuits in Radiation Detection G. Deptuch (Fermi National Accelerator Laboratory, Batavia, USA)
10:55	**Coffee Break**
11:15	**Session part 2**
	A reason for REASON *... or How to Make Someting out of Nothing* W. Kuźmicz (Warsaw University of Technology, Poland)
	What's new at IEEE SSCS R. Kumar (President, IEEE Solid-State Circuits Society)
	Discussion: Chapter matters, activity plans
13:00	**Lunch**

Rakesh Kumar
President & CEO, TCX Technology Connexions, USA
President, IEEE Solid-State Circuits Society

Challenges and Innovation Opportunities in Semiconductors

Phenomenal growth in the use of mobile wireless products is fueling a resurgence of excitement in the semiconductor industry. In spite of increasing investment costs and predictions of doom and gloom a few years back, these are exciting times in the semiconductor innovation pipeline. After providing a brief background and status of the semiconductor industry and its recent drivers, this seminar will offer a discussion of the important challenges and opportunities. The author's recently published book, "Fabless Semiconductor Implementation", McGraw Hill, will serve as a reference text.

Grzegorz Deptuch
Fermi National Accelerator Laboratory, Batavia, USA

3D integration for circuits in radiation detection

Exploration of the vertically integrated circuits, also commonly known as 3D-IC technology, for applications in radiation detection started at Fermilab in 2006. This talk examines the opportunities that vertical integration offers by looking at various 3D designs. Early work by Fermilab has led to an international consortium for the development of 3D-IC circuits for High Energy Physics. For the first time, Fermilab has organized a 3D MPW run gathering more than 25 different designs submitted by the consortium.

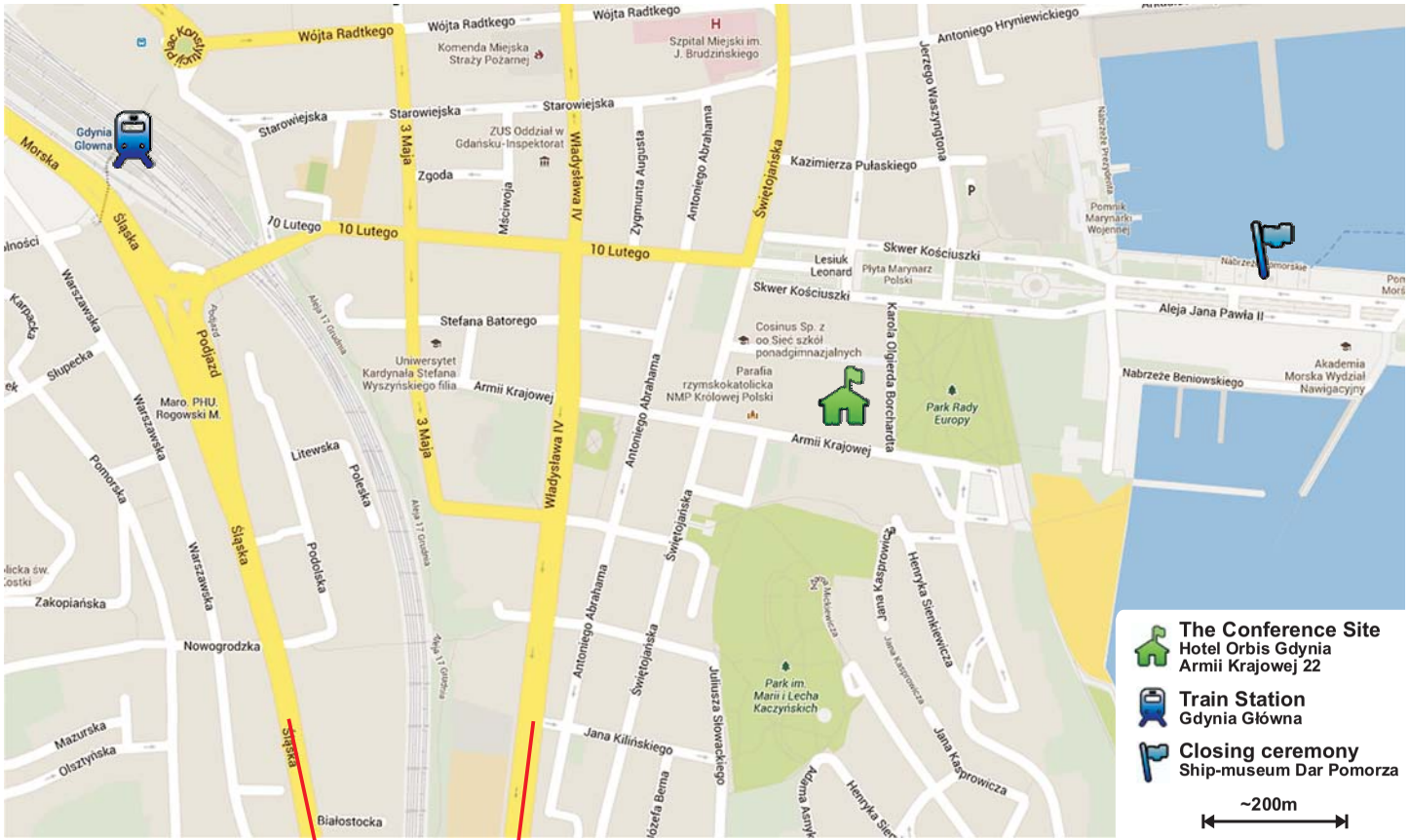
Wiesław Kuźmicz
Warsaw University of Technology, Poland

A reason for REASON
... or how to make something out of nothing

This is a talk about revival of microelectronics in Poland after a total collapse in 1989-1990 - actors, actions, the REASON project, current status and perspectives.

Google maps

Gdynia City Map




DAR POMORZA
Dar Pomorza