Design Considerations for Integrated SiGe BiCMOS Phase-Locked Loops in the Millimeter-Wave Band

Frank Herzel, Arzu Ergintav, Corrado Carta, Gunter Fischer
tIHP - Leibniz-Institut für innovative Mikroelektronik
Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
{herzel,ergintav,carta,gfischer}@ihp-microelectronics.com

Extended Abstract

We present design guidelines for analog phase-locked loops (PLL) at millimeter wave (mmWave) frequencies in SiGe BiCMOS technology. Emphasis is placed on a robust functionality with a relatively constant phase noise performance under ionizing radiation in space. The analog tuning range of the voltage-controlled oscillator (VCO) is split into coarse and fine tuning. Using negative feedback in the fine tuning loop of the PLL, the fine tuning control voltage is kept close to the VCO gain maximum for a constant PLL loop bandwidth. Together with self-triggered sub-band switching, a long lifetime of the PLL is expected, since any VCO degradation will be compensated keeping VCO gain and loop bandwidth fairly constant. An integrated SiGe-HBT based phase detector for mmWave PLLs is proposed, where a fractional-N PLL in the lower GHz range drives several simple mmWave PLLs in a phased-array transceiver.

An integration of the VCO and the loop filter together with the PLL core would give a significant cost advantage. However, the low quality factor of the variable capacitors (varactors) in the VCO results in a relatively high phase noise at mmWave frequencies. In order to meet the stringent phase noise requirements in space applications, a large loop bandwidth is mandatory in order to filter out VCO phase noise as much as possible. Using several phase-aligned mmWave PLLs would reduce the phase noise at the output of the receiver frontend. In order to achieve a programmable output frequency, the mmWave PLL (array) should be driven by a fractional-N PLL at a moderate frequency. The jitter performance of a hybrid OFDM system using such an architecture was analyzed in [1]. It was shown that the phase noise of the common low-frequency PLL can be reduced by one global pilot tracking loop, while the phase noise of the mmWave PLL array is much reduced due to noise averaging in conjunction with a large PLL bandwidth. A high frequency at the phase detector input was found to be essential for a low jitter of the mmWave PLL, since it allows a large loop bandwidth to be used for VCO phase noise reduction.

This paper presents a robust 28.3-33 GHz integer-N PLL design in a 130 nm SiGe-BiCMOS technology. It describes and compares two different phase detector (PD) versions using MOSFETs or SiGe HBTs, respectively. The first PLL uses high-voltage MOSFETs for the PD design which is limited to a few hundred MHz at the PD input. By contrast, a bipolar PD achieves several GHz. Fig. 1 shows a block diagram of the PLL with a bipolar PD using an input frequency around 2 GHz. A bipolar phase-frequency detector (PFD) followed

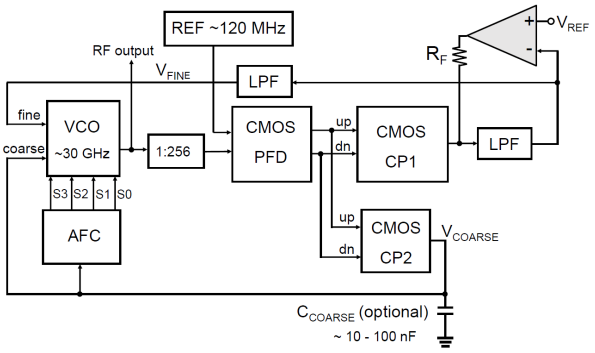

Fig. 1. Block diagram of a dual-loop PLL using a bipolar phase detector.

by an integrated differential bipolar amplifier is employed for a high speed. By using 1:16 frequency dividers, the input frequency to the CMOS PFD is reduced to about 125 MHz, a convenient frequency for the thick-oxide MOSFETs used for CMOS PFD and charge pump.

The coarse tuning voltage is depicted in Fig. 2 together with the fine tuning voltage $V_{\mathrm{FINE}} \approx V_{\mathrm{IN}-}$.

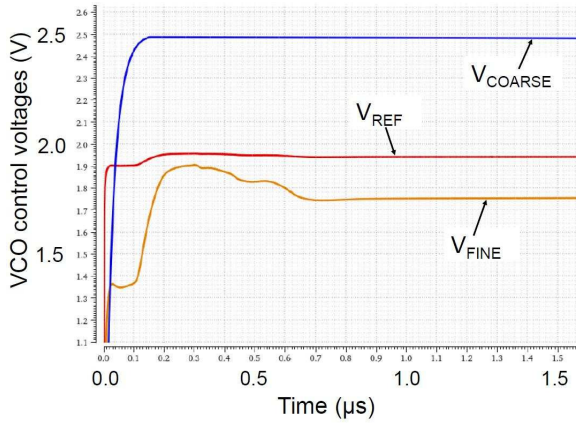

Fig. 2. Transistor-level simulation of VCO tuning voltages during frequency settling.

References

[1] F. Herzel, C. Carta and G. Fischer, "Jitter minimization of phase-locked loops for OFDM-based millimeter-wave communication systems with beam steering," *2024 31st International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*, Gdansk, Poland, 2024, pp. 118-123, doi: 10.23919/MIXDES62605.2024.10613942.