

CMOS OTA for Detector Readout Electronics Integrator in the ALICE FIT Project

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EXTENDED ABSTRACT

The paper discusses the design and optimization of a CMOS OTA (Operational Transconductance Amplifier) circuit for the FIT detector in the ALICE experiment at CERN, aimed at efficiently processing particle collisions in high-noise environments. The OTA scheme is visible in Figure 1.

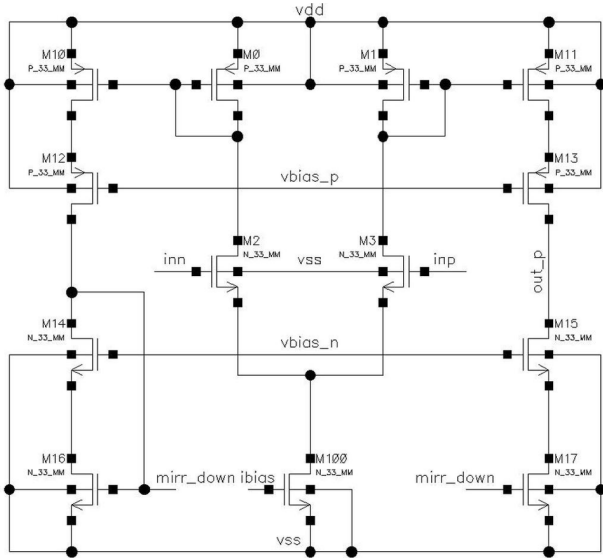


Fig. 1. Scheme of the designed OTA

The OTA is part of an integrated ASIC intended to replace current discrete components, providing a power-efficient, area-efficient solution while handling nanosecond analog pulses. The circuit is implemented using 180-nm CMOS technology within Cadence Virtuoso, and powered by a 3.3 V supply. The paper delves into the specific challenges of maintaining high

bandwidth, linearity, and signal stability, alongside reducing power consumption. The chosen OTA architecture, a symmetric CMOS with cascodes, offers a balanced trade-off between these factors, leveraging high currents and careful layout designs to mitigate process-related variations. Simulations reveal that while the OTA performs well under various conditions and corners, calibration systems are necessary to counteract inevitable mismatches.

These features culminate in an OTA that is smaller, uses less power, and maintains functional accuracy relative to its discrete predecessors, despite a reduced input voltage range due to technological constraints (Table I).

TABLE I
SUMMARY OF SIMULATION RESULTS

Parameter [units]	(a)	(b)	(c)
CMOS process [nm]	180	180	XFCB
Supply voltage [V]	± 1.65	± 1.65	± 5
Capacitive load [pF]	50	50	–
DC gain [dB]	53.31	52.91	63
PM [°]	90.81	90.43	56
GBW [MHz]	7.978	7.908	410
CMRR @DC [dB]	66.5	65.6	90
PSRR+ @DC [dB]	66.1	65.3	74
PSRR- @DC [dB]	46.2	45.1	74
Power [mW]	22.8	22.5	190
Area [mm ²]	–	0.044	9
FoM [MHz·pF/mA]	57.7	58	–

(a) Simulation (b) Post-extraction simulation (c) Discrete amplifier