Extraction of Open-Access-PDK Active Inductance Parameters with FOSS Tools

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Extended Abstract

A recent trend in support of integrated circuit (IC) design and manufacture has been the release of open-access production development kits (PDKs) [1] [2], encouraging the use of FOSS ECAD tools at every stage in the semiconductor manufacturing cycle [3]. This in turn under-pins a growing "Open-Hardware" movement [4] [5] particularly, through the merger of FOSS circuit simulators with freely available open-access PDK kits. Prior to the release of open-access PDKs, Verilog-A compact device modelling acted as a bridge between sub-micron semiconductor models and circuit simulation. This is still true, but the addition of PDK semiconductor processing data to the open-access IC design tool chain now allows the application of FOSS tools to be extended to the characterization of manufacturable IC circuit blocks. The main elements in the PDK/FOSS merger are model libraries, characterized by Verilog-A parameters extracted from measured device data. In parallel there has also been a steady improvement in FOSS circuit simulator modelling capabilities that link extended analysis and simulation features with post simulation graphical visualisation. These allow, at an early stage in the IC design/manufacture sequence, extraction of analogue block parameters from simulation output data. This paper introduces a number of extended Qucs-S/Ngspice circuit simulation capabilities and demonstrates their application in the analysis and design of a single ended CMOS active inductor cell designed with the IHP-SG13G2 BiCMOS technology node. Particular attention is given to the modelling and simulation of the fundamental two transistor CMOS active inductance based on a admittance approach that allows simple extraction of the inductor parameters from real and imaginary admittance properties and their differentiation in the frequency domain. Figure 1 shows a Qucs-S/Ngspice test bench for simulating the admittance of a CMOS active inductance over a GHz frequency band. Fig. 2 illustrates a set of typical Zin and Yin simulation data plots.

References

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[4] Open Source Hardware Association (OSHWA), "Opwn Source Hardware". [Accessed February 2025] [Online] Available: https://www.oshw.org.
[5] P2PF, "Open Source Hardware". [Accessed February 2025] [Online] Available: https://wikp2pfoundation.net/Open_Source_Hardware.

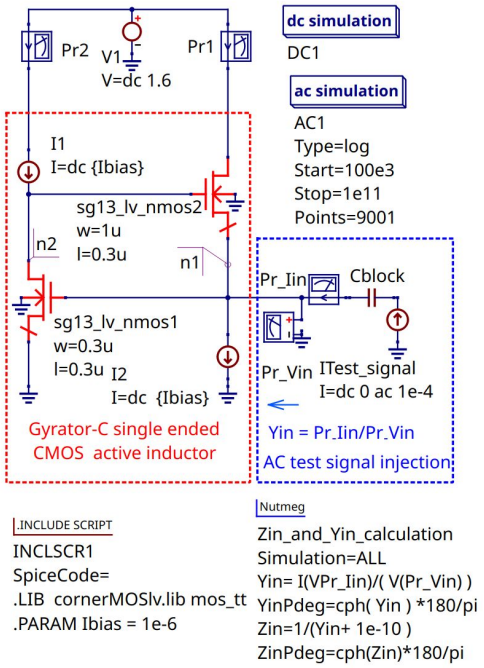

Fig. 1. A Qucs-S/Ngspice test bench for evaluating the a.c. performance of an IHP-Sg13g2 technology CMOS active inductance.

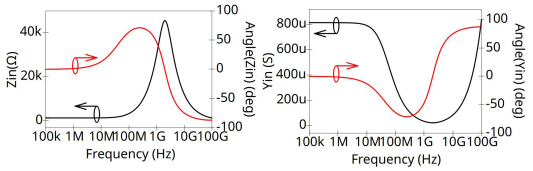

Fig. 2. Example IHP-Sg13g2 thin oxide technology CMOS active inductor Zin and Yin characteristics for $Ibias$ = 1μA