

Design of the Charge-Sampling Multiplying PLL in CMOS 40 nm

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EXTENDED ABSTRACT

One of the very popular PLLs is the subsampling-based architecture that main advantage is creating virtual clock multiplier which allow to avoid amplifying noise originating from charge pump. Also in locked state divider's phase noise is eliminated and power consumptions is lower. Drawback of this solution is necessity of interrupting oscillator output nodes by sampling process. Many approaches have been proposed to minimize such effects, like power gating operations, but still limitations were set by time needed for common mode setting or resonant steady-state time in the case of the LC tank [1, 2].

To overcome the above-mentioned issues, charge integrating phase detector was proposed [3]. Designed as a simple common source stage measures phase error by integrating charge on capacitor during only half time of VCO period. Principles of phase difference detection is presented in Fig. 1, where we can see two scenarios and corresponding detector outputs in locked state and VCO leading case. The negligible detection time (only 0.45% of the total clock reference period) minimize capacitance modulation effect.

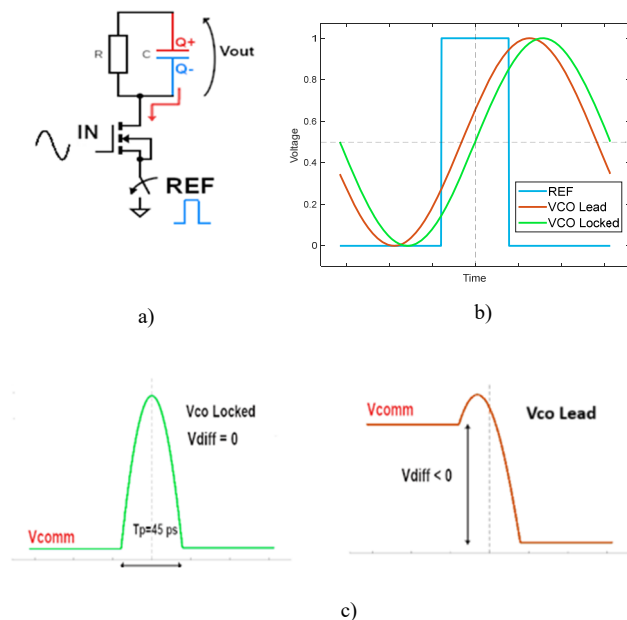


Fig. 1. Phase detection process overview: a) Phase Detector, b) PLL in locked and dislocked state, and c) resulting output voltage.

The charge sampling process is based on integrating current on a capacitance without applying any switches to hold the sampled voltage. The drawback of this solution is the discharging process, with time-constant $R_S C_S$ (impedance of common mode stage), by current flowing in parallel connected resistor (needed to avoid extra origin pole in PLL transfer function). However this disadvantage can be partially alleviated by using high common mode suppressing amplifier, as the ripples appear both on positive and negative PD output. Also choosing differential input VCO additionally suppress this effect. Here folded cascode operational transconductance amplifier (OTA) is used. For further improvement of the common mode gain, the tail current source is cascaded. The OTA is supported with common mode amplifier, as it is illustrated in Fig 2. Native NMOS is pertinent, as just one couple is sufficient in average voltage level block (source follower configuration). With these applications PLL's reference spur power can be lowered below -70 dBc.

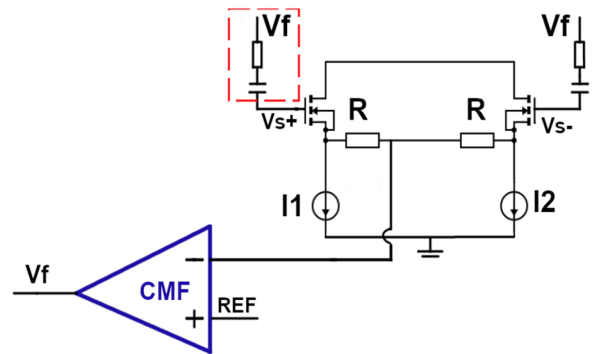


Fig. 2. CMF feedback.

REFERENCES

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