Implementation of a PLL Loop Circuit for Frequency Synthesis in 65 nm CMOS Technology

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***Abstract*—This paper presents the design and implementation of a phase-locked loop (PLL) circuit in 65 nm CMOS technology, dedicated to frequency synthesis and multiplication in radio frequency (RF) applications. The circuit processes an input signal of 13.56 MHz and generates a multiplied output signal of 867.84 MHz in the ultra high frequency (UHF) band, making it suitable for short-range communication systems such as radio-frequency identification (RFID) and near-field communication (NFC). The circuit was designed to ensure low phase noise, frequency stability, and fast locking time. The results demonstrate the feasibility of the proposed PLL architecture for modern wireless communication systems, highlighting its potential for integration into advanced RF applications.**

***Keywords*—VLSI, IC, PLL, phase-locked loop, CMOS, NFC, RFID, RF, HF, UHF, phase noise, stability.**

SUMMARY

The paper presents a complete design flow and performance analysis of a Phase-Locked Loop (PLL) system implemented in 65 nm CMOS technology, intended for use in short-range RF communication applications such as radio-frequency identification (RFID) and near-field communication (NFC).

Section I introduces the motivation and use cases for PLLs in modern RF systems, discussing their essential role in precise frequency synthesis for reliable data transmission. Section II provides a theoretical foundation by presenting a linearized model in the Laplace domain, defining key parameters like loop gain, and stability considerations. The use of Integer-N architecture is analysed and justified based on its influence on the transfer function.

Section III details the design process of individual PLL blocks. The PFD and charge pump are implemented in a configuration that ensures accurate phase and frequency error detection. A wide-swing cascode current mirror is used to achieve wide output voltage range and maintain current matching across PVT variations. The VCO is implemented as a current-starved ring oscillator with seven stages, incorporating Schmitt triggers for enhanced noise immunity and output stability. The third-order passive loop filter stabilizes the loop response, balancing responsiveness and stability. The frequency divider, implemented using six D flip-flops, provides the necessary frequency division factor of 64 and ensures synchronization between the PLL input (13.56 MHz) and the divider's output. Additionally, a 27.12 MHz clock signal, twice the reference frequency, can be potentially extracted from the second-to-last divider stage for potential NFC digital circuit applications.

Section IV discusses the verification and simulation results, including phase noise analysis, system stability evaluation, settling time measurements and current consumption under various process corners. The worst-case settling time is approximately 30 µs, and phase noise performance remains under -100 dBc/Hz at 10 MHz offset. Simulation results confirm that the PLL achieves fast synchronization within 50 µs, ensuring compliance with the ISO/IEC 14443 standard. The design demonstrates stable operation across various PVT conditions.

Section V concludes with a summary of the results and highlights directions for future research to further enhance the PLL's efficiency and performance. These include potential gain stabilization techniques for the VCO - improvements such as dynamic charge pump current scaling and digitally controlled filter trimming to enhance loop adaptability and robustness in changing environmental conditions.

Beyond the technical aspects, this study underscores the relevance of PLL-based frequency synthesis in modern communication technologies, where signal accuracy and stability are crucial. The proposed architecture balances performance, efficiency, and integration feasibility, making it a compelling candidate for next-generation wireless applications. Further research will explore circuit optimizations to enhance power efficiency and improve performance under extreme operating conditions.

These results highlight the feasibility of the proposed PLL for integration into modern wireless communication systems, offering a compact and efficient solution for high-frequency signal generation. The findings presented in this work contribute to ongoing advancements in RF circuit design, paving the way for more efficient and reliable frequency synthesis techniques.