

A Thermal Behavior of Lateral (VESTIC) BJTs on SOI Substrate

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Abstract—This paper analyzes the thermal behavior of lateral (Vertical Slit Transistor Integrated Circuits, VESTIC) and vertical BJTs on SOI substrates, focusing on self-heating effects, heat dissipation mechanisms, and thermal stability. The buried oxide (BOX) layer in SOI significantly impacts heat flow, leading to localized hot spots in vertical BJTs and more distributed heating in lateral BJTs. Using numerical simulations and experimental data, we evaluate thermal management strategies and their implications for complementary bipolar logic (CBip). The findings highlight the need for optimized device layouts and biasing techniques to mitigate self-heating, ensuring stable and efficient operation of SOI-based bipolar circuits.

Keywords—lateral BJT; VESTIC; SOI; self-heating; thermal management

SUMMARY

This paper investigates the thermal behavior of lateral bipolar junction transistors (BJTs), specifically those fabricated using VESTIC (Vertical Slit Transistor Integrated Circuit) technology, on silicon-on-insulator (SOI) substrates. The study contrasts lateral BJTs with traditional vertical BJTs, emphasizing self-heating effects, heat dissipation mechanisms, and implications for logic circuit stability and performance.

The unique geometry of lateral BJTs—where current flows parallel to the wafer surface—results in a more distributed heat

generation profile compared to the localized hot spots observed in vertical BJTs. On SOI substrates, the buried oxide (BOX) layer inhibits vertical heat conduction, making lateral heat spreading a critical pathway. This limitation accentuates the importance of thermal-aware design techniques such as layout optimization, the use of pillar metal contacts (acting as thermal vias), and careful biasing strategies to mitigate thermal runaway.

The analysis draws on experimental data, electrothermal simulations, and literature comparisons, indicating that lateral BJTs, particularly the VES-BJT design, offer superior thermal behavior for certain applications due to their planar heat dissipation characteristics. Furthermore, the work explores thermally stabilized complementary bipolar logic (CBip), which employs matched NPN and PNP lateral BJTs on SOI for CMOS-like operation. Proper thermal management, including resistive biasing and circuit-level stabilization, allows these logic gates to function reliably and adapt their performance based on operating conditions.

Ultimately, the paper positions VESTIC-based lateral BJTs as a compelling technology for energy-efficient, high-speed bipolar logic, with thermal behavior as both a challenge and a design lever. The findings open opportunities for hybrid logic architectures combining bipolar speed with CMOS-like control.