

High-Accuracy ECG Signal Acquisition Using a Power-Efficient 6-bit Level-Crossing ADC

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SUMMARY

This paper presents a novel approach using level-crossing ADCs (LC-ADCs), which provide a more power-efficient solution by sampling only when the input signal exceeds predefined amplitude thresholds. A 6-bit LC-ADC architecture that eliminates the need for an n-bit DAC and uses a single comparator, incorporating integrated sample-and-hold and logic functions, is proposed. This design drastically reduces power consumption while maintaining accuracy, making it particularly suitable for low-power biomedical applications. Simulation results in 180 nm CMOS technology with 1.8-V power supply demonstrate the system's high performance, including a Figure-of-Merit (FoM) that outperforms traditional designs. The proposed LC-ADC architecture is shown to be highly efficient, with significant reductions in power usage and FoM to 90 nW and 0.115 fJ/step, offering an ideal solution for long-term, energy-constrained biomedical signal monitoring.

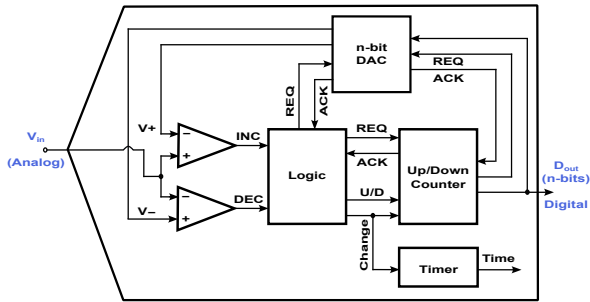


Fig. 1. Block diagram of the conventional LC-ADC using two comparators, an n-bit DAC, a logic block, a timer, and an up/down counter

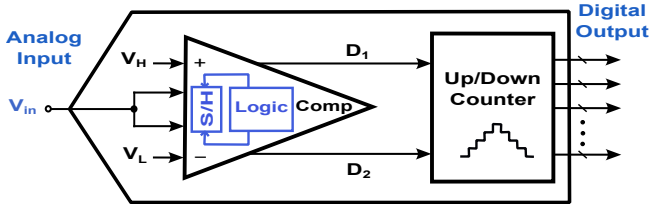


Fig. 2. Block diagram of the proposed LC-ADC, consisting of a comparator with integrated S/H and logic blocks, along with an up/down counter

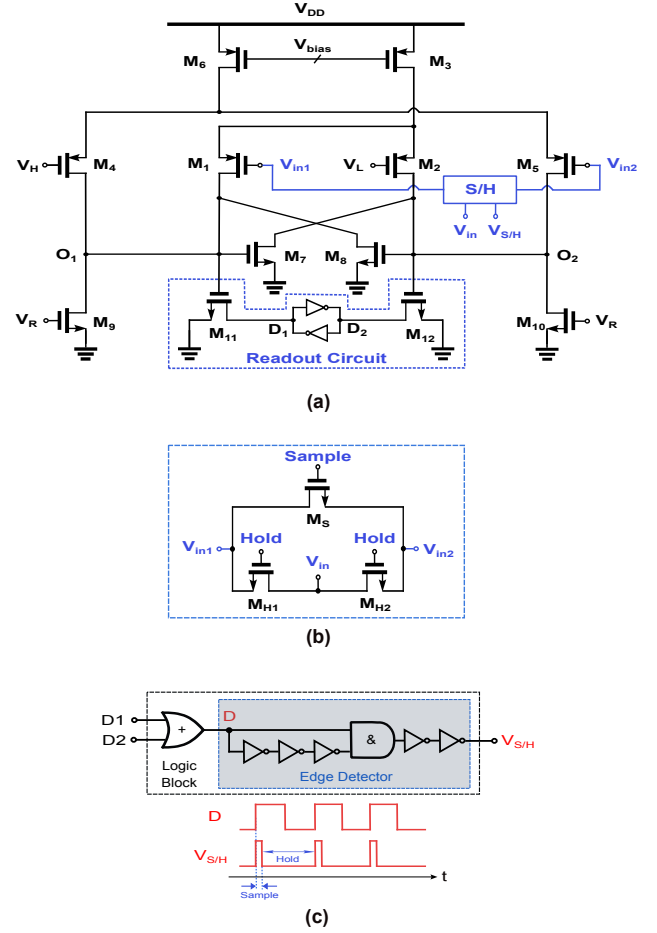


Fig. 3. Transistor level structure of the comparator block including: (a) core current comparator and readout circuit, (b) sample and hold (S/H) circuit, and (c) embedded logic block with edge detector and its input and output pulses

TABLE I
PERFORMANCE COMPARISON WITH OTHER LC-ADCs

Reference	16	17	22	23	This Work
Process (nm)	180	180	180	180	180
Supply (V)	0.55-1	0.5	1	1.8	1.8
Power (nW)	186	60-220	18	220	90
BW (kHz)	1	1	2.5	10	15
ENOB (bit)	6.2-7.9	5.6	6.2-7.7	6.8	5.7
FoM (fJ/conv.)	165	124	98	198	115
Sim./Meas.	Meas.	Meas.	Sim.	Sim.	Sim.