An Integrated Phase Noise Generator for Sensitivity Measurements on Superconducting Qubits

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Extended Abstract

A fully integrated phase noise generator for sensitivity measurements is presented. It is based on a charge pump phase-locked loop (CP-PLL) design with controllable loop parameters. Bandpass-shaped phase noise spectra with controllable peak frequency and phase noise power can be generated. Based on a second-order PLL model and simple stochastic differential equations, phase noise models in frequency and time domain are derived. As an illustration, a 3.5 GHz CP-PLL designed in a 130 nm BiCMOS technology is simulated with different control parameters for phase noise shaping. The approach lends itself to sensitivity measurements of superconducting qubits for quantum computers and for modeling such systems.

Clock generation circuits are needed in many electronic systems including radar sensors, communication systems and quantum computers. Phase noise (PN) in the clock signal results in a random position of the signal's zero crossings known as timing jitter. Jitter reduces the ranging precision in radar systems [1] and increases the bit-error rate (BER) in digital communication [2]. In quantum computers, PN can alter the quantum state of superconducting qubits [3], [4]. To evaluate how well a system handles a noisy clock, a source with specific PN characteristics can be used. This allows engineers to determine performance factors like jitter attenuation or bit error rate under real-world conditions. The degree of performance degradation due to PN does not only depend on the noise power quantified by the phase jitter variance, but also on the noise frequency. Generally, fast noise is more harmful than slow noise, since the latter can often be reduced in the system by signal processing and filtering [5]. In the case of superconducting qubits, resonance effects might occur if the noise frequency is close to the Rabi frequency, i.e., the rotation speed for a single-qubit gate. As future quantum controllers might be required to work close to the quantum processor, i.e., at cryogenic temperatures, a small form factor and a low power dissipation in the clock generation circuit become essential. Therefore, a silicon-based single-chip realization of the clock generation circuitry is highly desirable.

This paper presents an integrated charge pump phase-locked loop (CP-PLL) suitable for generation of both overdamped and underdamped frequency dynamics. The underdamped case results in a bandpass-like peak in the PN spectrum with adjustable position and height. This will allow the sensitivity of superconducting qubits to be measured as a function of frequency. Based on a numerically generated Wiener process, we derive a time-domain simulation model for the corresponding PLL phase noise with realistic parameters.

Fig. 1 shows the modeled phase noise spectra for the overdamped PLL and the weakly damped PLL. The position of the peak in the underdamped PLL PN spectrum can be moved by varying the loop filter capacitance.

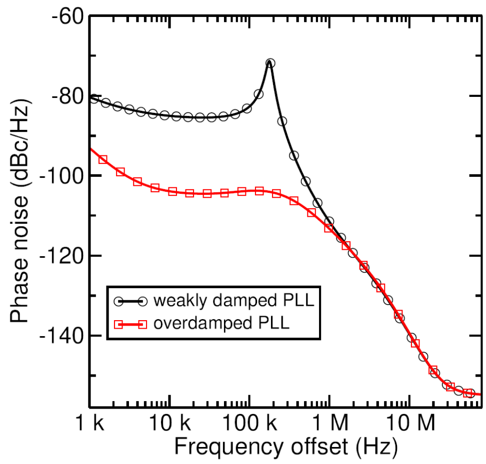

Fig. 1. Modeled phase noise spectra for a weakly damped PLL (I_{CP}=110 μA, I_{OS}=28 μA, C=200 pF) and a strongly overdamped PLL (I_{CP}=1 mA, I_{OS}=28 μA, C=2.2 nF).

References

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