Design of a Gaussian Activation Function Generator for Neural Network Applications

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***Abstract*—This paper introduces a novel method for the design of a Gaussian activation function generator. To achieve enhanced accuracy in Gaussian function generation, an original higher-order mathematical approximation is employed. A further improvement in approximation precision is obtained through the implementation of a newly proposed variable transformation technique. The highly accurate approximation function is realized in CMOS technology by means of two types of computational circuits: a squaring circuit and a multiplier/divider circuit. The simple and accurate implementation of these computational structures also contributes to the overall high precision of the proposed Gaussian activation function generator. The current-mode operation on which these CMOS computational circuits are based significantly improves the frequency response of the proposed generator and additionally enables low-voltage operation, with a supply voltage of 0.9 V. Biasing all MOS transistors at extremely low current levels ensures low-power operation, the maximum power consumption being approximately 2.5 µW. The silicon area required for the proposed Gaussian activation function generator is approximately 30 µm². The functionality of the proposed generator is validated through simulations performed using a 0.18 µm TSMC CMOS process, with SPICE simulation results confirming the theoretical analysis.**

***Keywords*—Gaussian activation function generator, neural networks, approximation function, VLSI design, current-mode operation**

SUMMARY

The Gaussian function is widely employed in numerous application domains, including neuro-fuzzy systems, classification tasks, pattern recognition, backpropagation neural networks, on-chip unsupervised learning, and wavelet transform implementations.

The accurate generation of the Gaussian function while minimizing hardware resource utilization, along with the capability of fine-tuning its parameters, represents a primary objective in the design of Gaussian function synthesizer circuits. Numerous Gaussian function implementations have been reported in the literature, employing a broad range of design methodologies.

Despite their advantages, these computational structures are susceptible to technological variations and exhibit performance degradation with temperature changes. Moreover, for most existing solutions, reconfiguring the specific characteristics of the generated Gaussian function remains relatively challenging.

This paper introduces a novel method for the design of a Gaussian activation function generator. To achieve enhanced accuracy in Gaussian function generation, an original higher-order mathematical approximation is employed. A further improvement in approximation precision is obtained through the implementation of a newly proposed variable transformation technique. The highly accurate approximation function is realized in CMOS technology by means of two types of computational circuits: a squaring circuit and a multiplier/divider circuit. The simple and accurate implementation of these computational structures also contributes to the overall high precision of the proposed Gaussian activation function generator. The current-mode operation on which these CMOS computational circuits are based significantly improves the frequency response of the proposed generator and additionally enables low-voltage operation, with a supply voltage of 0.9 V. Biasing all MOS transistors at extremely low current levels ensures low-power operation, the maximum power consumption being approximately 2.5 µW. The silicon area required for the proposed Gaussian activation function generator is approximately 30 µm². The functionality of the proposed generator is validated through simulations performed using a 0.18 µm TSMC CMOS process, with SPICE simulation results confirming the theoretical analysis.