A 400 fs Resolution Vernier TDC with Adaptive Voltage Scaling

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***Abstract*—This paper proposes the development of a 3-bit Vernier TDC with a sub-ps time resolution to be used as a phase detector in a PLL. Furthermore, this work also implements an adaptive voltage scaling scheme by incorporating a regulator in conjunction with a PTAT current source to mitigate fluctuations in resolution across PVT conditions. Both components were implemented and simulated using a 16 nm FinFET technology node. The aforementioned system achieves an average time resolution of 400 fs with a maximum PVT variance of 52 fs, presenting a INL of 0.054 LSB, while consuming 1.46 mW of power and occupying a silicon area of 188 µm².**

***Keywords*—time-to-digital converters, adaptive voltage scaling, CMOS inverters**

I. Introduction

All-digital Phase Locked Loops (ADPLL) have emerged as an alternative to Phase Locked Loop (PLL), offering an improved scalability with continued CMOS technology scaling.. The performance of these digital systems is strongly affected by quantization limits of their key time-domain blocks - namely, the Time-to-Digital Converter (TDC) and Numerically Controlled Oscillator (NCO) [1]. In particular, the TDC as a time-mode circuit, act as a precise stopwatch that converts time-domain information into a digital word. Since the fine-tuning of the PLL output signal requires the detection of small time differences, the TDC must provide high time resolution and exceptional linearity. In addition, the system must ensure minimal variation in resolution over a variety of operating conditions. However conventional TDC architectures, often exhibit significant resolution variations in PVT conditions, limiting the performance and reliability of ADPLLs.

In this work, we propose a Vernier TDC architecture supplied by a dedicated voltage regulator that implements an adaptive voltage scaling (AVS) [2], referenced by a PTAT current source [3], to minimize the time resolution variability across PVT conditions.

II. Proposed Circuits

The proposed 3-bit TDC functions as a fine-tune detector and employs a Vernier structure to measure the phase difference using two types of inverter-based delay cells with slightly different delays. The resulting phase difference is evaluated by a C²MOS data flip-flop that acts as an arbiter [4].

In order to guarantee delay stability under PVT variations, the TDC is supplied by a voltage regulator based on adaptive voltage scaling (AVS). Rather than referencing a fixed bandgap voltage, the regulator generates a dynamic reference derived from the voltage drop of a biased short-circuited inverter. This renders the regulated voltage inherently dependent on process voltage variations. The employment of a PTAT bias current enables the regulated supply to adapt to temperature, thereby maintaining the inverter transconductance and ensuring minimal variation in the Vernier cell delay.

TABLE I.
TDCs performance comparison.

	[5]	[6]	[7]	This work
Technique	2D Vernier	Vernier	Spiral 2D Vernier	Vernier + AVS
Tech. (nm)	65	28	45	16
LSB (ps)	4.8	1.5	1.25	**0.40**
INL (LSB)	3.3	0.6	0.34	**0.054**
Power (mW)	1.7	0.43	0.33	1.46
ENOB	4.9	NA	7.58	2.92
Area (µm²)	2×10^4	2290	4×10^5	188
FOM (pJ/step)	0.81	NA	0.022	1.92
Δ LSB (fs)	NA	NA	NA	**52**

III. Simulation Results

The proposed system shows a small conversion offset of 360 fs for output code 0 and maximum delay of 3.14 ps for the maximum output code 7. This results in an average time resolution T_{LSB} of 397 fs and a INL of 0.054 LSB, having a total current consumption of 1.22 mA. This system also exhibits a time resolution variation of 52 fs in PVT.

IV. Conclusion

This paper proposed a 3-bit Vernier-based TDC with adaptive voltage scaling, developed using a 16 nm FinFET process. It has been demonstrated that the incorporation of adaptive voltage scaling markedly enhances the converter's resilience to PVT variations, thereby ensuring stable performance across diverse operating conditions.

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