Digital Signal Tuning System for MEMS Excitation

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SUMMARY

Resonant micromechanical sensor elements, such as micro-electromechanical system (MEMS) cantilevers, have emerged as crucial components in various applications [1], [2]. These resonators rely on precise excitation at their resonance frequency, necessitating the utilization of highly accurate electronic oscillators [3] and requiring high-resolution frequency control. Achieving the required frequency precision while meeting stringent demands on phase noise presents a significant challenge in the design of such systems [4]. The circuit presented in this paper is intended to drive MEMS resonators in resonance while striking a favorable balance of tunability and noise.

Here, we propose an approach to balance tunability and phase noise in oscillator design for resonant micromechanical sensors. The presented system uses a high-precision master clock, i.e. a crystal oscillator, at its input, and employs mixed-signal processing to achieve tunability without sacrificing phase noise performance. This method operates with a square wave signal. The fundamental frequency of the square wave will subsequently be extracted using the sharp bandpass filtering property of the MEMS resonator. We term this the Digital Signal Tuning System (DSTS).

The DSTS produces an output frequency about 10 times lower than the clock reference with very high tuning resolution. This is accomplished by first dividing the reference clock with a gross division to bring it into the range of the desired resonance frequency. The division factor $D = 10$ is chosen to further reduce phase noise, as the noise decreases with $1/D^2$ [5]. Fine-tuning is then achieved by periodically dropping individual pulses from the reference clock. Dropping input pulses leads directly to a longer output signal period resulting in a lower frequency.

The system has four digital inputs (clock, latch, programming and reset) and one clock output. Internally, it consists of three counters (input, output and program), several flip-flops for internal states and basic logic gates. The circuit is operating as follows. To create a defined state, a pulse to the reset input resets all counters and flipflops. Next, by toggling the programming input, k is set to any value up to 511. Afterwards, a pulse on the latch input copies the program counter to the input counter. In the last step, a clock signal is applied to the clock input, to generate the desired output clock.

When the input clock is running, the output counter counts to five. Upon reaching this value, the counter toggles a T-flipflop, which controls the output signal, and resets itself to zero. This effectively divides the input clock by a factor of 10. Simultaneously, the input counter counts downwards from k that was programmed in the beginning. When this counter reaches zero, the next pulse of the input clock is skipped at the output counter and the input counter is again set to the previously programmed value k. Every dropped input pulse leads to a longer signal period at the output of the circuit, effectively lowering the output frequency.

To compare the sensor system's performance, the limit of detection (LOD) is used as a figure of merit. The measurements are carried out in three different configurations. First, the resonator is excited with a regular sine wave in its respective resonance frequency by the signal generator. Next, the excitation signal of the signal generator is changed to a rectangular wave of the same frequency. In a third measurement, the resonator is excited by the DSTS system.

In all three configurations, the noise amplitude density spectrum is almost identical (DSTS: 22 $nA/Hz^{1/2}$, sine: 23 $nA/Hz^{1/2}$, square: 22 $nA/Hz^{1/2}$). Regarding the amplitude spectrum of the signal measurement, the signals are again very close (DSTS: 5.7 mA/T, sine: 5.7 mA/T, square: 5.8 mA/T). Accordingly, the LOD for all tree cases is very similar (DSTS: 3.82 $nT/Hz^{1/2}$, sine: 3.95 $nT/Hz^{1/2}$, square: 3.71 $nT/Hz^{1/2}$). The results demonstrate, that the sensor system performance is comparable across all investigated setups, indicating, that the DSTS ASIC can be used as a drop-in replacement for a bench-top signal generator in this application.

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