IP Release and Cross-Foundry Design Migration for 3D-MRAM Technology

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SUMMARY

This paper presents a practical methodology in the 3D-MRAM intellectual property (IP) design by focusing on two key aspects: automated layout migration approach for advanced CMOS process technology and a quality-driven IP release flow. The proposed migration methodology integrates drawing-layer mapping, layer synthesis, device remapping, and iterative DRC/LVS verification to ensure design correctness in the target technology. The technology migration and IP release flows described in this paper improve design productivity, reduce manual effort and provide a scalable framework applicable to a broad range of semiconductor IP design projects.

Magnetoresistive Random Access Memory (MRAM) is an emerging non-volatile memory technology that stores data using the magnetic states of Magnetic Tunnel Junctions (MTJs), rather than electric charge as in conventional SRAM or DRAM. Owing to its non-volatility, high endurance, fast access speed, and ultra-low standby power, MRAM has become an attractive embedded memory candidate in the System-on-Chip (SoC) applications.

3D-MRAM further enhances conventional MRAM by vertically stacking multiple MTJ layers within a CMOS process flow, thereby achieving significantly higher memory density without increasing the silicon footprint. Our project developed a 3D-MRAM memory system in a 28-nm CMOS technology. The system integrates 3D-MRAM memory arrays with analog peripheral circuits, read/write sensing circuits, control logic, and embedded SRAM block. Circuit design and physical layout were implemented using full-custom methodology based on foundry provided process design kits (PDKs) and technology rules.

This paper presents CAD methodologies to deploy 3D-MRAM technology and IP designs across multiple technologies for SOC customers. The main contributions of this work are twofold as follows:

1) An automated layout migration methodology for transferring full-custom 3D-MRAM design databases from a mature process to an advanced technology node.
2) A production-oriented IP release methodology for 3D-MRAM including physical signoff for quality assurance.

Here is the summary of contents in this paper. We describe the IP release workflow, with emphasis on physical verification and signoff checks as key quality-control measures. By incorporating comprehensive physical verification and cross-view I/O consistency checking, the IP release flow improves the reliability and deployment readiness of the released IP database. Then we review layout migration methods and presents our methodology for cross-technology layout migration on this 3D-MRAM IP project. It details the implementation of drawing-layer mapping and synthesis between foundries, automation using Cadence PVS tool platform and LVS verification methodology for the converted design database.

The primary objective of the layout migration is to minimize manual redesign effort, enable rapid turnaround time, and ensure the correctness of the converted layout database. Note that the proposed layout migration methodology is primarily applied to the peripheral circuits surrounding the 3D-MRAM memory core. The memory core itself typically requires custom layout optimization in the target process to achieve the best area efficiency and performance.

Layout migration between two semiconductor foundries requires establishing a clear correspondence between their respective drawing layers. Although CMOS processes from different foundries share many common physical layers, the target technology may introduce new, modified, or differently defined layers that are not present in the original process. To address these differences, we adopt a layer mapping and synthesis methodology to migrate the layout design database. Cadence Physical Verification System (PVS) tool is used as the execution engine to perform layer mapping, layer synthesis, geometric transformations including polygon sizing as well as LVS checks.

As semiconductor technologies continue to scale, modern VLSI systems require higher performance, lower power consumption, and reduced die area, placing increasing emphasis on efficient and reliable semiconductor IP. In this context, automated and methodologies for IP release workflow and cross-foundry layout migration automation described in this paper have become increasingly important.