A Low-Power Low-Offset DAC-Less LC-ADC for Biomedical Signal Acquisition

Farzad Modarresi
Department of Electrical and Computer Engineering
Islamic Azad University
Mahabad, Iran
f.modarresi@gmail.com

Abdollah Amini
Department of Electrical, Computer and Biomedical Engineering
University of Pavia
Pavia, Italy
abdollah.amini01@universitadipavia.it

Summary

This paper presents a low-power DAC-less level-crossing analog-to-digital converter (LC-ADC) designed for biomedical signal acquisition. In contrast to conventional uniform-sampling ADCs, level-crossing converters generate samples only when the input signal crosses predefined amplitude levels, making them particularly suitable for sparse biomedical signals and enabling significant power reduction. The proposed architecture eliminates the conventional n-bit digital-to-analog converter (DAC), thereby reducing circuit complexity and power consumption compared to traditional LC-ADC implementations. Furthermore, an offset-cancellation mechanism is incorporated to suppress comparator offset and improve conversion accuracy. The proposed 8-bit LC-ADC is designed and simulated in a standard $0.18\,\mu$m CMOS technology using HSPICE. Simulation results show that the converter operates from a 5 V supply while consuming approximately $30\,\mu$W of power. For input bandwidths ranging from 50 Hz to 3 kHz, the converter achieves an effective number of bits (ENOB) of 7.6 bits and a figure-of-merit (FoM) of 15.9 pJ/conv, demonstrating its suitability for low-power biomedical sensing applications.

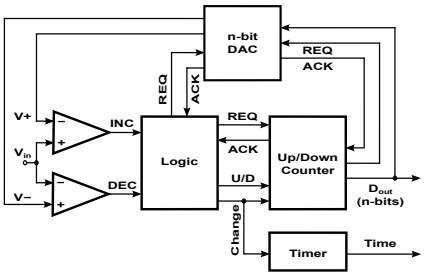

Fig. 1. Block diagram of a conventional LC-ADC.

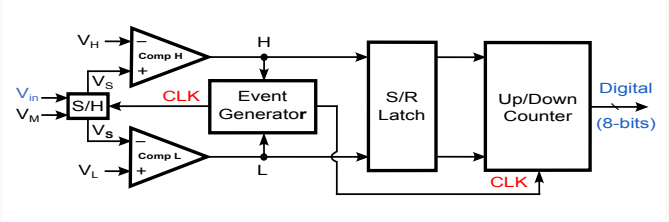

Fig. 2. Total block diagram of the proposed level-crossing ADC.

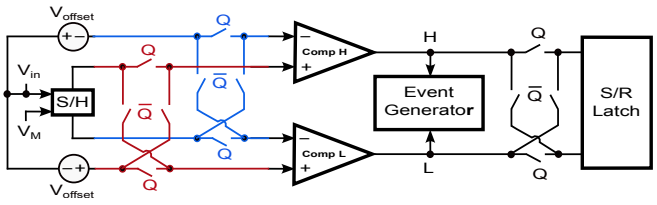

Fig. 3. Embedded offset-cancellation (chopping) mechanism.

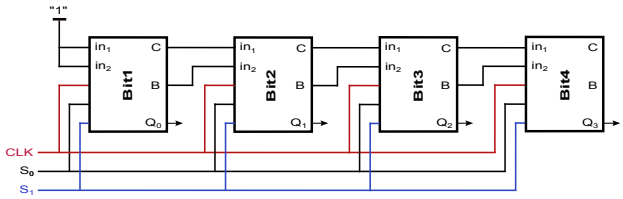

Fig. 4. Proposed 4-bit counter block diagram.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED LC-ADC WITH PREVIOUS WORKS

Parameter	[1]	[2]	[3]	[4]	This work
Technology (nm)	90	180	500	600	180
Resolution (bits)	8	8	6	8	8
Bandwidth (kHz)	0.2–3.4	1	0.2–5	5.4	0.05–3
Power (μW)	45	25	118.6	100	30
FoM (pJ/conv)	28.5	48.8	165.6	36	19.5

References

[1] B. Schell and Y. Tsividis, "A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2472–2481, Nov. 2008.

[2] M. Trakimas and S. Sonkusale, "An adaptive resolution asynchronous ADC architecture for data compression in energy-constrained sensing applications," *IEEE Trans. Circuits Syst. I: Regul. Pap.*, vol. 58, pp. 921–934, May 2011.

[3] W. Tang *et al.*, "Continuous-time level-crossing sampling ADC for biopotential recording systems," *IEEE Trans. Circuits Syst. I*, vol. 66, no. 6, pp. 1407–1418, Jun. 2013.

[4] D. Chen, Y. Li, D. Xu, J. Harris, and J. Principe, "Asynchronous biphasic pulse signal coding and its CMOS realization," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2006, pp. 2293–2296.