

# Readout Board for the CBM Silicon Tracking System: Design Constraints, Powering Concept and Functional Validation

Patryk Semeniuk<sup>1,2,3</sup>, Joerg Lehnert<sup>1</sup>, Ralf Kapell<sup>1</sup>

<sup>1</sup>GSI Helmholtzzentrum für Schwerionenforschung GmbH, Planckstraße 1, 64291 Darmstadt, Germany

<sup>2</sup>Goethe University Frankfurt, Max-von-Laue-Straße 1, 60438 Frankfurt am Main, Germany

<sup>3</sup>AGH University of Krakow, Mickiewicza 30, 30-059 Kraków, Poland

## EXTENDED ABSTRACT

The Compressed Baryonic Matter (CBM) experiment at FAIR investigates strongly interacting matter at high net-baryon densities using high-rate heavy-ion collisions. The experiment employs a free-streaming data acquisition concept in which time-stamped detector data are continuously transported to the First Level Event Selector (FLES) computing farm for online event building and selection.

Within this architecture, the Silicon Tracking System (STS) requires a readout chain capable of sustaining high data throughput while fulfilling strict mechanical and system-integration constraints imposed by the detector environment.

The STS Readout Board (STS-ROB) implements the intermediate readout layer between the detector front-end electronics and the Common Readout Interface (CRI) based back-end data acquisition system. The board aggregates data streams from front-end boards equipped with STS-XYTER ASICs and forwards them towards the back-end through high-speed optical links.

The STS-ROB integrates three GBTx devices (one transceiver and two transmitter-only devices) forming the central aggregation stage of the readout chain. Detector data from the front-end boards are transported to the ROB via electrical GBT E-Links operating at 320 Mb/s. The reference clock and control information are received from the back-end by the ROB via the optical downlink and subsequently distributed through the electrical interface towards the detector electronics.

With up to 14 uplinks per GBTx and three GBTx devices per board, the architecture supports up to 42 electrical uplinks corresponding to an aggregated payload bandwidth of approximately 13.44 Gb/s. The aggregated payload is transmitted to the back-end via three optical uplinks operating at 4.8 Gb/s each using VTRx and VTTx optical modules from the CERN Versatile Link project.

The design of the STS-ROB evolved from the earlier Common Readout Board (CROB) prototype used during the development phase of the STS readout chain. The final detector-

form-factor implementation was driven by strict integration constraints of the STS detector, including limited space for electronics and cabling inside the support structure. Compared to the CROB prototype, the redesigned board significantly reduces the PCB area while preserving the high-speed electrical and optical routing required for reliable data transmission.

A key aspect of the system architecture is the external powering concept. Instead of generating the low-voltage rails directly on the readout board, the STS-ROB is powered by a dedicated Readout Powering Board (RPOB). The RPOB hosts radiation-tolerant FEAST\_MP DC/DC converters and distributes the 1.5 V and 2.5 V supply rails to up to four STS-ROB boards simultaneously, enabling a compact ROB/POB stack compatible with the final detector integration concept.

Functional validation of the STS-ROB was performed in a representative laboratory setup using an optical connection to a CRI board acting as the back-end interface and multiple FEB8 front-end boards connected through the electrical interface. The validation campaign addressed communication stability on both electrical and optical links, monitoring of key operational parameters, and the characterization of start-up and recovery behaviour relevant for system commissioning and acceptance testing.

Long-duration optical transmission tests demonstrated stable link operation with no detected bit errors during multi-day runs. Automated register write-readback tests and fixed-pattern transmission modes verified reliable end-to-end operation of the complete readout chain.

Continuous monitoring via the on-board GBT-SCA ADC confirmed stable thermal and electrical operating conditions during extended runs, demonstrating millivolt-level stability of the 1.5 V and 2.5 V supply rails and steady-state board temperatures during long-term operation.

The presented results demonstrate that the STS-ROB fulfills the functional and integration requirements of the CBM Silicon Tracking System and provides a robust and scalable interface between the detector front-end electronics and the back-end data acquisition system.