A Sub-300-pW Voltage Reference with -227-dB PSR Using ΔV_{GS} and Multi-Loop Regulation

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Extended Abstract

This work presents an ultralow-power CMOS voltage reference (VR) designed for power-constrained microsystems such as biomedical sensors, wearable electronics, and environmental monitoring devices. In these applications, integrated circuits are often supplied by unstable, energy-harvested sources, delivering low and widely-fluctuating voltage levels. Therefore, VR able to maintain high stability in such operating conditions, while consuming extremely low power, are needed. To address these requirements, the hereby presented VR combines a ΔV_{GS}-based core and a scalable multi-loop regulation approach to achieve exceptionally low power-supply rejection (PSR) and line sensitivity (LS) metrics.

Traditional bandgap references deliver good temperature stability and chip-to-chip reproducibility, but they are generally unideal for ultralow-power, low-voltage systems, due to their reliance on bipolar junction transistors (BJTs) and resistors, implying larger area occupation and power consumption. CMOS-only references, especially those leveraging MOSFETs operating in deep weak inversion, have thusly become an appealing alternative. In particular, simple 2-transistor (2T) references can achieve picowatt-level consumption, but they are typically affected by poor immunity to supply variations.

To address this limitation, the proposed architecture combines a temperature-compensated core with an optimized multi-stage regulation mechanism. In the first place, a ΔV_{GS}-based reference core is used to generate a temperature-stable reference voltage, V_{ref}. Such a core is composed by two stacked diode-connected MOSFETs sized with different channel lengths, receiving bias current from a third device stacked in the same circuit branch. The difference between their threshold voltages, induced by the reverse short-channel effect, produces a complementary-to-absolute-temperature (CTAT) voltage component. This term is combined with a proportional-to-absolute-temperature (PTAT) component derived from a difference of overdrive voltages. Acting on the ratio between the aspect ratios of the two core transistors, the temperature slope of the PTAT quantity can be adjusted up to realizing first-order temperature compensation of V_{ref}.

To improve immunity to supply voltage variations, this work introduces a multi-loop regulation structure on top of the ΔV_{GS}-based core, whereby additional regulating devices are stacked above the core and self-biased exploiting intermediate nodes. Each additional regulation stage effectively multiplies the suppression factor of supply variations by the intrinsic gain of the regulating device. Analytical modeling provided in the paper shows that the LS results to be inversely proportional to the product of the intrinsic gains of all regulating transistors. While multi-loop regulation has been previously applied to basic 2T-VRs, it is hereby combined with a ΔV_{GS}-based core for the first time. Besides, more notably, a systematic analysis is also provided to show that, through proper sizing of the regulating devices, optimum operation across diverse supply voltages can be achieved. Specifically, following the proposed guidelines, it is possible to obtain that, upon decreasing supply voltage, the upper-most stacked transistors enter the triode region first, while transistors at the bottom of the stack enter triode conditions last. This implies that, even with supply voltages too low to allow saturation biasing of all stacked transistors, V_{ref} generation is preserved rather than totally disrupted, with reasonable reduction of supply immunity.

Electrical simulations were performed for VR designs realized with a 0.18 µCMOS process. Implementations with up to 4 regulation stages are compared through extensive sets of simulations, providing supporting evidence to the analytical models concerning LS and supply range. Specifically, it is shown how increasing the number of regulation stages dramatically improves LS: from about 210 ppm/V of the basic configuration to as low as 0.0153 ppb/V (-227-dB PSR at dc), evaluated under 0.8-V supply. At the same time, correct generation of V_{ref} is preserved down to 0.4-V supply, with acceptable reduction of supply immunity. These findings prove that properly designed multi-loop regulated VRs with a high number of regulation stages should be preferred regardless of the supply level, hence resulting to be ideal for scenarios with widely-fluctuating supply voltages. On top of this, power consumption below 300 pW, temperature coefficient around 20 ppm/°C (from -20 to 80 °C), and strong robustness to process corner and random mismatch variations are attained.

The achieved LS and PSR results represent substantial improvements with respect to the state of the art, providing strong motivation for future fabrication of the designed VR. Moreover, the design guidelines proposed to allow versatile operation of the multi-loop regulation scheme under diverse supply voltage levels also constitute innovative insight. These results entail strong suitability of the proposed VR architecture for inclusion in energy-harvested microsystems subject to strict power constraints, low supply voltage levels, and widely fluctuating operating conditions.