An LDO with 1 A at 1 Ω Load, 3.95 fs FoM and 70 dB PSRR for TEC Controller Applications

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***Abstract*—A frequency compensation scheme for low-dropout regulators (LDOs) is presented to achieve stability in high loop-gain architectures without altering the load capacitor when implemented in 65 nm CMOS technology. The technique improves the linearity of the LDO, allowing the regulator to be applied in thermoelectric cooler (TEC) controller systems. Cross-coupled current mirrors are used to increase transconductance, strengthen the negative feedback mechanism, improve transistor matching, and raise the output resistance. As a result, the design achieves higher gain, better linearity, and an improved figure of merit (FoM) compared with conventional current mirror structures. Simulation results demonstrate the effectiveness of the proposed approach, showing a loop gain above 90 dB, a power supply rejection ratio (PSRR) of 70 dB at 1 MHz, and an FoM of 3.95 fs at a load current of 1 A.**

***Keywords*—Power management, voltage regulator, load regulation, line regulation, PSRR, frequency compensation, LDO stability.**

I. Introduction

Low-dropout (LDO) regulators are critical building blocks in modern power management integrated circuits, required to supply stable voltages to sensitive analog and digital loads. In thermoelectric cooler (TEC) controller applications, the LDO must simultaneously support a heavy load current of up to 1 A into a 1 Ω load, maintain high loop gain for good line and load regulation, and provide strong rejection of power supply noise. Conventional single-ended current mirror topologies fall short in meeting all these requirements together, as they limit the achievable transconductance, output resistance, and overall loop gain. Miller compensation and load-capacitor tuning have been explored as stability techniques, but they either sacrifice bandwidth or require off-chip passive components, increasing cost and board area [1].

II. Proposed Technique

The proposed design employs *cross-coupled current mirrors* in the error amplifier core. This structure increases the effective transconductance (g_m) without additional bias current by leveraging the differential cross-coupling, which simultaneously strengthens the negative feedback path and improves transistor matching through correlated biasing. The raised output resistance, combined with higher g_m, pushes the loop gain well above 90 dB. Crucially, stability is achieved entirely through the internal compensation scheme — no modification of the external load capacitor is required, making the design suitable for integration in TEC driver systems without additional passive components [2].

III. Results and Discussion

The proposed LDO was designed and simulated in 65 nm CMOS 1P6M technology with a supply voltage of 2.5 V and a load current of 1 A. The design achieves a loop gain of 91 dB, a PSRR of 71 dB at 1 MHz, and a record-low FoM of 3.95 fs. Compared with prior works, the design in [1] (0.18 μm) supports only 100 mA load with an 80 dB loop gain, 60 dB PSRR, and FoM of $\sim$31.5 fs. The work in [2] (0.18 μm) achieves 150 mA load, 70 dB loop gain, 50 dB PSRR, and FoM greater than 16.5 fs. The design in [3] (0.25 μm) reports 50 mA load, 55 dB loop gain, 68 dB PSRR, and FoM greater than 16.5 fs. The proposed work outperforms all these designs, particularly achieving a more than $4\times$ improvement in FoM, while being the only design to support a full 1 A load current in 65 nm CMOS technology.

Monte Carlo simulations across 1000 runs confirm PSRR of 70 dB with a standard deviation of 0.35 dB, validating fabrication robustness. PVT analysis shows a loop gain variation of only 8 dB and PSRR variation of 5 dB across temperature from $-20°$C to 100°C and supply from 2.25 V to 2.75 V. The output noise at 1 MHz is 27.7 nV/$\sqrt{\text{Hz}}$, and the settling time is approximately 32 μs [3].

IV. Conclusion

A compact internal frequency compensation scheme for LDO regulators in TEC controllers is presented. By using cross-coupled current mirrors, the design achieves 91 dB loop gain, 71 dB PSRR at 1 MHz, and a FoM of 3.95 fs at a 1 A load in 65 nm CMOS, without needing external capacitor tuning. This makes it a practical and efficient choice for integrated TEC power management systems.

References

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