An Active-Passive 2^{nd}-order CTΣΔM Using Single FIR Feedback for Battery Monitoring

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***Abstract*—This paper presents a 2^{nd}-order hybrid (active-passive) CTΣΔM for battery monitoring. The ΣΔM uses a single 4-tap FIR DAC feedback path and adds zeros to each RC integrator for stabilization. This modulator was designed in 65nm CMOS technology. It dissipates 237μW from a 1.2V supply with a clock of 20MHz. The modulator occupies an estimated area of 0.209mm^2. Electrical transient noise simulations show, that for a signal bandwidth of 20KHz, 10KHz and 5KHz the modulator has a maximum SNDR of 93.29dB, 96.75dB and 99.52dB, respectively, under typical conditions, with minimums of 89.28dB, 92.35dB and 94.53dB and maximums of 94.61dB, 99.25dB and 101.3dB. The modulator has a DR of 95.3dB, 97.1dB and 100.1dB, under typical conditions, with minimums of 89.3dB, 91.6dB and 94.6dB and maximums of 97.5dB, 99.5dB, 102.5dB, for 20KHz, 10KHz and 5KHz bandwidths, respectively. FOM_W of 157.2, 211.3 and 306.7 fJ/conv.-step, for typical conditions, with minimums of 67.8, 95.8 and 151.9fJ/conv.-step and maximums of 618.2, 565.3 and 896.9fJ/conv.-step, for bandwidths of 20KHz, 10KHz and 5KHz, respectively.**

***Keywords*—Analog to Digital Converter (ADC), Sigma-Delta Modulator (ΣΔM), Continuous Time (CT), Ring amplifier (RA)**

SUMMARY

The proposed CTΣΔM uses an active integrator and a passive integrator with FIR feedback. Since the majority of the area is occupied by the integrating capacitors, resistors and the feedback resistors. The resistors' values can get significantly large in the passive integrator because since this circuit does not have gain, therefore, it was decided to use integrators with an extra zero, so that the second feedback isn't needed for stabilization, thus reducing the area by eliminating the resistors associated to this feedback path. Figure 1 shows the proposed modulator and Figure 2 the resistive FIR DAC circuit. The modulador coefficients values were optimized in order to maximize performance and minimize area using a high-level model. A 4-tap FIR was chosen due to insignificant SNDR penalty and greater simplicity when comparing the CIFB with 4-tap and 12-tap versions. Figure 3 shows the schematic of the amplifier which is based on the critically damped ring amplifier . To increase the gain, the damping $\frac{1}{gm}$ stages are deleted, resulting in moving the poles at nodes V_o and V_{o2} closer to DC. The pole at the V_o node is moved closer to DC by adding a load composed by R_z and C_z, making this the dominant pole and stabilizing the amplifier. This is possible because the required GBW is only 200MHz and therefore it is possible to trade bandwidth for DC gain.

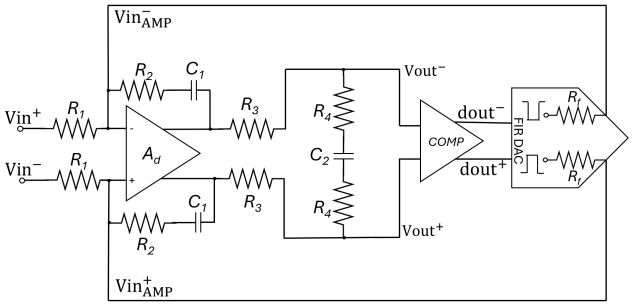

Fig. 1. Proposed CTΣΔM

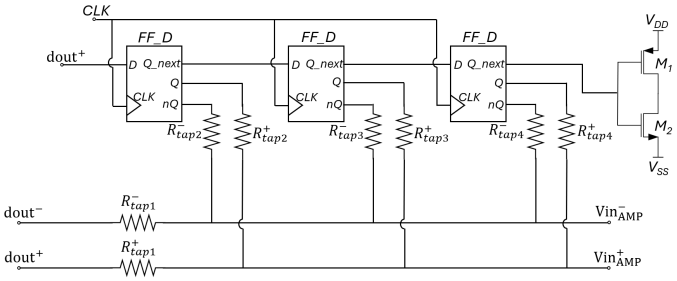

Fig. 2. FIR schematic

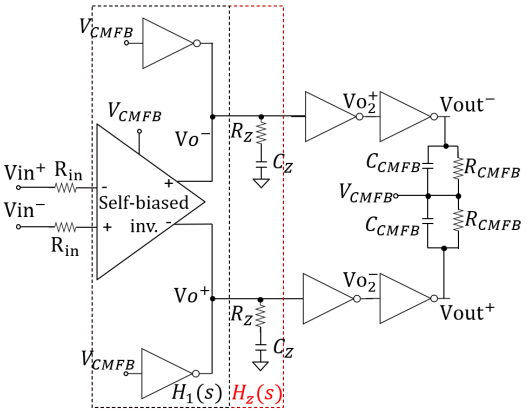

Fig. 3. Modified critically damped ring amplifier with extra zero