

Charge-Modulated Conductance and Synaptic Behavior in Access-Region WSe₂/h-BN/Gr van der Waals Floating-Gate Transistors for Nonvolatile Memory

Shu-Ping Lin^{1,2}

¹ Department of Electronics and Electrical Engineering, National Yang Ming Chiao Tung University, Hsinchu 300093, Taiwan

² Bachelor Program in Intellectual Creativity Engineering, National Chung Hsing University, Taichung 40227, Taiwan

E-mail: splin1@nycu.edu.tw; splin@email.nchu.edu.tw

Abstract—Neuromorphic hardware requires nonvolatile memory and continuously tunable conductance to emulate synaptic plasticity in biological neural systems. Here, we report a van der Waals floating-gate field-effect transistor (FGFET) based on WSe₂/hexagonal boron nitride (h-BN)/ graphene (Gr) heterostructure and systematically investigate its memory and synaptic characteristics. Charge trapping in the Gr floating gate produces a pronounced memory window, enabling stable and nonvolatile modulation of channel conductance. Under gate-voltage pulse stimulation, the device exhibits excitatory and inhibitory postsynaptic current (EPSC/IPSC)-like responses, with conductance states gradually tuned by pulse amplitude, number, and duration. These results demonstrate that the WSe₂/h-BN/Gr floating-gate platform is a promising candidate for neuromorphic synaptic applications.

Keywords—neuromorphic devices; access region; van der Waals floating-gate transistor; synaptic plasticity; excitatory and inhibitory postsynaptic current.

I. INTRODUCTION

The increasing demand for data-intensive and parallel computation has exposed fundamental energy-efficiency limitations in conventional von Neumann architectures due to the physical separation of memory and processing units. In contrast, biological synapses inherently integrate signal transmission and information storage within a single structural unit, inspiring the development of neuromorphic hardware capable of emulating synaptic functionality at the device level [1, 2].

Two-dimensional (2D) materials offer a compelling platform for developing varied neuromorphic devices owing to their atomic thickness, clean van der Waals interfaces, and tunable electronic properties [3]. In particular, floating-gate architectures incorporating Gr and layered semiconductors enable charge-storage-mediated modulation of channel conductance without continuous power consumption [4]. Based on this concept, we design and fabricate a WSe₂/h-BN/Gr van der Waals FGFET to investigate nonvolatile memory behavior and synaptic plasticity within a single electronic device.

II. MATERIALS AND METHODS

Each of the 2D materials, including Gr, h-BN, and WSe₂ flakes, was mechanically exfoliated and sequentially assembled onto a SiO₂/Si substrate (300 nm SiO₂) through van der Waals stacking using a dry-transfer technique (Fig. 1). Source and drain electrodes were defined by electron-beam lithography. Electrical characteristics were performed using a Lakeshore cryogenic probe station coupled with a Keysight B1500A semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

The transfer characteristics (Fig. 2(a)) of the WSe₂/h-BN/Gr FGFET exhibit a pronounced memory window (~90 V threshold shift), indicating efficient charge injection through the h-BN

tunneling layer and effective charge storage in the Gr floating gate [5]. The linear output characteristics (Fig. 2(b)) at low drain bias indicates good ohmic contact, ensuring stable carrier transport and reliable operation.

To further evaluate synaptic functionality, pulse-response measurements were conducted. Under gate-voltage pulse stimulation, the device generates EPSC/IPSC-like transient responses, driven by charge trapping/detrapping in the floating gate. The channel conductance can be continuously tuned by varying pulse amplitude, duration, and number [6]. Furthermore, the conductance state can be systematically tuned by adjusting the pulse amplitude, pulse number, and pulse duration, leading to gradual and history-dependent evolution of the channel current. Such progressive and analog conductance modulation closely resembles synaptic weight updates in biological neural networks, demonstrating the capability of the floating-gate architecture to emulate spike-dependent synaptic plasticity.

IV. CONCLUSION

The WSe₂/h-BN/Gr van der Waals FGFET effectively integrates nonvolatile memory and synaptic functionality, highlighting its suitability for neuromorphic computing systems. Future work aims to extend functionality toward optoelectronic synapses via optical excitation.

ACKNOWLEDGMENT

This work was supported by the Taiwan Semiconductor Research Institute (TSRI) and the Czech Technical University in Prague (CTU) through the TSRI-CTU Joint Research Center. The authors gratefully acknowledge the National Institutes of Applied Research (NIAR), Taiwan, for financial support and assistance in facilitating the international collaborative research project TSRI-2026-JRC201.

REFERENCES

- [1] S.P. Lin, A. Ghosh, K.L. Chen, H.L. Hsiao, M.Y. Tsai, Y.F. Lin, *Mater. Sci. Eng. R-Rep.* 163 (2025) 11.
- [2] Y.F. Zhang, L.S. Wang, Z.X. Huang, W. Deng, X. Yan, F.X. Chen, *Appl. Mater. Today* 46 (2025).
- [3] J. Wang, F. Ma, W. Liang, M. Sun, *Materials Today Physics* 2 (2017) 6-34.
- [4] D. Kahng, S.M. Sze, *At&T Tech J* 46(6) (1967) 1288 - 1295.
- [5] E. Wu, Y. Xie, S. Wang, C. Wu, D. Zhang, X. Hu, J. Liu, *Nanotechnology* 31(48) (2020) 485205.
- [6] C. Yao, G. Wu, M. Huang, W. Wang, C. Zhang, J. Wu, H. Liu, B. Zheng, J. Yi, C. Zhu, *ACS Applied Materials & Interfaces* 15(19) (2023) 23573-23582.



Fig. 1. Optical microscopy image of the fabricated WSe₂/h-BN/Gr FGFET.

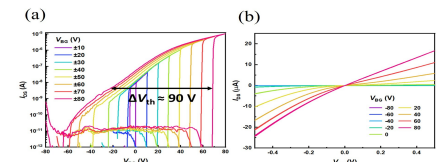


Fig. 2. Electrical characteristics of the WSe₂/h-BN/Gr FGFET. (a) Transfer curves at various VDS. (b) Output characteristics.

