

# A CMOS Double Balanced Mixer Using Current Bleeding and Negative Impedance Techniques

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**Abstract**—This paper presents a CMOS double-balanced Gilbert-cell mixer implemented in 65-nm RF CMOS technology for low-power RF receiver applications. The proposed design integrates current-bleeding and negative-impedance techniques to achieve simultaneous improvement in conversion gain, noise figure (NF), and linearity. The negative-impedance network compensates parasitic effects, enhancing gain and bandwidth, while current bleeding reduces flicker-noise up-conversion and improves linearity. The mixer operates at 4.6 GHz with a 1 V supply and consumes 4.78 mW power. Post-layout results show a conversion gain of 16.4 dB, NF of 18.2 dB, and IIP3 of 8.2 dBm. Monte Carlo and PVT simulations confirm robust performance. The proposed design achieves an excellent trade-off among gain, noise, linearity, and power efficiency.

**Keywords**—CMOS mixer, current bleeding, negative impedance, RF circuits, conversion gain

## I. INTRODUCTION

Double-balanced mixers [1], [2] are essential components in modern RF systems, enabling frequency translation while suppressing LO and RF feedthrough. They are widely used in applications such as communication receivers, sensing systems, and instrumentation. However, achieving a simultaneous trade-off among conversion gain, noise figure (NF), and linearity remains a key challenge, especially under low-voltage and low-power constraints.

## II. PROPOSED MIXER ARCHITECTURE

The proposed mixer is based on a Gilbert-cell [3] topology consisting of a transconductance stage, switching stage, and load stage. The RF input is converted to current using a differential pair, while the LO-driven switching stage performs frequency translation.

To improve performance, a current-bleeding [4] technique is introduced, where auxiliary transistors divert part of the bias current away from the switching stage. This reduces voltage drop, suppresses flicker-noise up-conversion, and enhances linearity.

Additionally, a cross-coupled capacitor is employed to introduce negative impedance at the RF stage. This compensates parasitic capacitances, reduces the Miller effect, and improves gain and bandwidth. The combined techniques result in improved overall mixer performance without increasing power consumption.

## III. RESULTS AND DISCUSSION

The proposed mixer is implemented in 65-nm CMOS technology and operates at 4.6 GHz with a 1 V supply. Schematic simulations achieve a conversion gain of 18.5 dB and NF of 10.1 dB. After layout extraction, the gain reduces to 16.4 dB and NF increases to 18.2 dB due to parasitic effects.

Two-tone simulations show an IIP3 of 8.2 dBm, indicating improved linearity. Monte Carlo simulations with 1000 samples demonstrate a mean output of 32.25 mV with a standard deviation of 1.02 mV, confirming robustness against process variations. PVT analysis further validates stable performance across different operating conditions.

The slight degradation in gain and NF after layout is mainly attributed to interconnect parasitics and additional capacitances introduced during routing. However, the performance remains within acceptable limits, demonstrating the effectiveness of the proposed design. The current-bleeding technique contributes to improved linearity, while the negative-impedance approach enhances gain and bandwidth, resulting in a balanced overall performance.

## IV. CONCLUSION

A low-power CMOS double-balanced mixer using current bleeding and negative impedance techniques is presented. The design achieves improved conversion gain, linearity, and noise performance with low power consumption. The results confirm that the proposed architecture is suitable for low-voltage RF receiver front-end applications.

## REFERENCES

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