Low Power Low Phase Noise Stacked Quadrature Ring Oscillator

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***Abstract*—Traditional ring oscillators are usually designed to have an odd number of inverter stages, however modern communication systems use quadrature signals, which cannot be directly produced by a single-ended odd-numbered ring oscillator.**

Development of single-ended even-numbered ring oscillators is therefore necessary to directly produce quadrature output. This paper aims to improve the performance of an already existing QRO (Quadrature Ring Oscillator) by introducing a strong injection locking technique, achieved with stacking the oscillator's inverters to reduce the circuit power consumption.

The proposed oscillator was implemented using a 65nm CMOS technology, this technique shows a phase noise deterioration of around 4.6 dBc/Hz (@ 10MHz) although presenting only a 1 dBc/Hz (@ 10MHz) FOM reduction, this is possible due to the proposed oscillator's consumption being less than half that of a Classic QRO topology when operating at the GHz range.

***Keywords*—Quadrature output, Ring oscillator, CMOS, Oscillator**

I. Introduction

Traditional ring oscillators are usually designed to have an odd number of inverter stages, this is because an even-numbered inverter ring oscillator latches up during startup, achieving a stable operating point. Modern communication systems, use quadrature signals to increase communication rates, however single-ended odd-numbered inverter ring oscillators cannot directly generate quadrature outputs, instead relying on half frequency dividers or double ended inverters to generate them. Therefore additional circuitry needs to be added to a traditional ring oscillator topology to avoid latch ups on single-ended even-numbered ring odcillators in order to produce a quadrature output.

Markus et al, developed a QRO topology that is capable of oscillating using a single-ended even-numbered inverter ring. Using that topology as a basis this paper aims to improve the oscillator performance using stacked inverters, to reduce the circuit's power consumption, and in turn increase performance.

This paper is divided into 5 sections. Section I is the Introduction and presents an overview of what the paper aims to achieve. Section I describes the QRO topologies used in this paper and the reason for their development. Section III studies the design process of each circuit and provides an insight over how to optimize each topology. Section IV presents each topology's results obtained via simulation. Finally section V concludes the paper.

A. Classic Quadrature Ring Oscillator

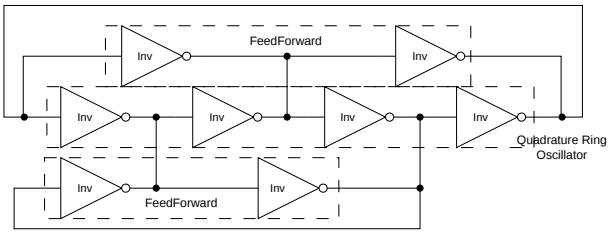

Fig. 1. Classic Quadrature Ring Oscillator Topology

B. Proposed Quadrature Ring Oscillator

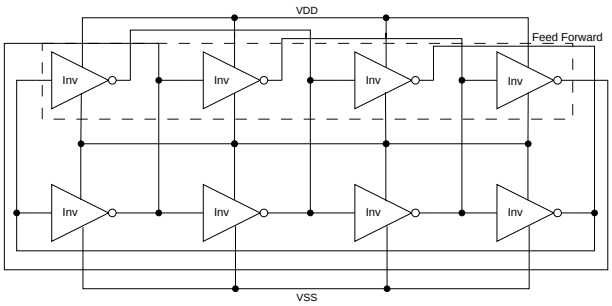

Fig. 2. Proposed Quadrature Ring Oscillator Topology

This paper manages to improve the performance of a Classic QRO by adjusting the sizes of it's non-ring inverters, whislt maintaining an oscillatory output improves the aforementioned oscillator's performance allowing it to achieve a better overall FOM. This was then built uppon by stacking the non-ring inverters with the ring inverters allowing for a reuse of current and a reduction in power consumprion, whilst maintaining oscillation, this reduced the oscillator's phase noise performance but kept a similar FOM performance to the Classic QRO, with the caveat of decreasing the oscillator frequency.

Simulation results show a 4.6 dBc/Hz (@ 10MHz) increase from the Classic QRO's phase noise, whilst both oscillate at similar frequencies, with only a 1 dBc/Hz (@ 10MHz) FOM increase, validating it's similar performance even with half the power consumption.