# RC Time-Constant Calibration Scheme Using a DPLL

João Paulo Carvalho, Nuno Paulino
NOVA School of Science and Technology
Center of Technology and Systems (UNINOVA-CTS)
Associated Laboratory of Intelligent Systems (LASI)
NOVA University of Lisbon, 2829-516 Caparica, Portugal
jpr.carvalho@campus.fct.unl.pt, nuno.f.paulino@fct.unl.pt

Blazej Nowacki
Specialty Analog & PHY IP Division, Renesas
Lisbon, Portugal
blazej.nowacki.zc@renesas.com

***Abstract*—This paper presents a mixed-signal calibration scheme for RC time constants. The calibration adjusts a programmable resistor array controlled by a 5-bit word inside a digitally controlled oscillator. Calibration is based on a DPLL locking mechanism, which generates the appropriate calibration digital code for given operating conditions. The calibration loop was evaluated across process, voltage and temperature (PVT) corners and Monte-Carlo simulations. The proposed architecture was implemented in 65 nm *TSMC* technology, achieving a tuning accuracy ranging from -2.1% to 1.6% with an occupied area of 0.01 mm$^2$. The area of the circuit was estimated (140% of the combined area of all components).**

***Keywords*—RC calibration, Digital Phase Locked Loop (DPLL), Digitally Controlled Oscillator (DCO), Phase and Frequency Detector (PFD)**

## SUMMARY

The block diagram of the closed loop calibration system, based on a Digital Phase Locked Loop (DPLL) is depicted in Fig. 1. The oscillation frequency of a Digitally Controlled Oscillator (DCO) Fig. 2, is compared to reference frequency, whose period matches the nominal RC value, using a phase and frequency detector (PFD). The output of the PFD is applied to the loop filter (LF) and the output of this filter produces the digital word that determines the value of the programmable resistor inside the DCO, closing the PLL feedback loop. The PFD generates 2 pulses, *Up* and *Dwn* whose pulse width is directly proportional to the instantaneous phase difference. This difference is accumulated over time in the LF producing a 5 bit calibration code that is going to adjust the DCO oscillation frequency by controlling the resistive array.

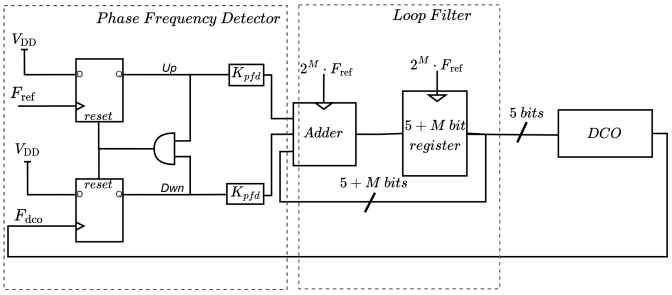


Fig. 1. Calibration loop

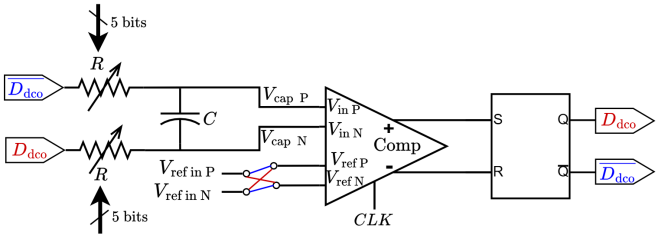


Fig. 2. DCO schematic

The proposed DCO is depicted in Fig. 2. Differentially, the passive integrator generates a nonlinear ramp until its amplitude reaches $V_{refP}$, upon which the direction of integration is inverted, until $V_{refN}$ is reached, generating a signal that oscillates between $\pm\Delta V_{ref}$.

The digital loop filter has a sampling frequency $F_s = 2^M \cdot F_{ref}$, which allows to measure the pulse width of *Up* and *Dwn* with an *M* bit resolution. The increased resolution forces the accumulator inside the LF to store an additional M bits beyond the previous 5, used to calibrate the DCO.

In order to validate the proposed calibration scheme, the circuit was designed in a 65nm CMOS technology, using poly resistors and mim capacitors. The error in the pole location associated with the locking code for each tested corner is reported in *Table* I. The analysis was extended by applying an offset to the locking code. The resulting pole location errors were significantly reduced. Therefore, in addition to implementing a mechanism that guarantees convergence to steady state across all corners, the final calibration code was reduced by 2 least significant bit. This offset code was ultimately adopted as the final calibration value.

TABLE I
POLE LOCATION ERROR USING LOCKING CODES

| Variables | Corners | | | |
|---|---|---|---|---|
| | SS | | FF | |
| | T=125°C | T=-40°C | T=125°C | T=-40°C |
| **DPLL Lock Code** | 31 | 31 | 8 | 8 |
| Lock freq (MHz) | 12.195 | 12.5 | 12.5 | 12.5 |
| **Final Calibration Code** | 29 | 29 | 6 | 6 |
| Error in pole freq (%) | 0.3 | 1.3 | -1.67 | -0.2 |