A Low Power, Low Area, Current Sampling Based Sense Amplifier Optimized for RRAM Readout Logic

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I. Introduction

This work presents a low power, low area, sense amplifier in current sensing enhanced architecture designed for enabling reliable readout of RRAM Resistive Switching RAM (RRAM) [1] based devices in standard and differential readout scheme. The proposed circuit can sense currents as low as 50nA at readout voltages as low as 0.3V. The sense amplifier is designed for 130nm CMOS fabrication node and will be incorporated as one of the crucial submodules of RRAM based PUF. To address the security and reliability requirements, additional optimizations against common power line vector attacks are also introduced.

II. Architecture

The Current-Sampling-Based Sense Amplifier (CSB-SA) architecture is evaluated. Our design builds upon the proposal presented in [2] as a direct extension, introducing optimizations specifically for ReRAM cells within the target process node, and enhancements addressing the potential vulnerabilities. The CSB-SA circuit utilizes shared transistors operating in two distinct regimes across sequential time phases: first for current sampling, and subsequently for current projection and amplification. Through this approach, the voltage offset resulting from V_{TH} variability is largely canceled at the hardware level [2]. Initial designs target the 130 nm CMOS process from STM, and RRAM integrated on back-end process. The complete schematic diagram of the entire CSB-SA circuit is shown in Fig. 1.

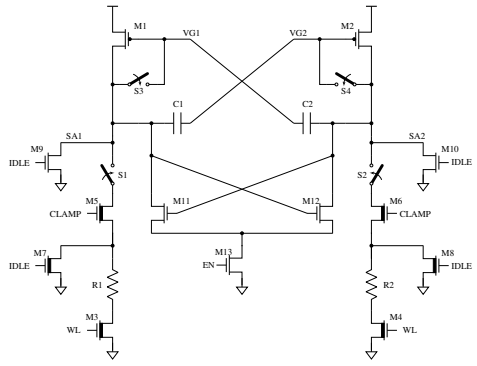

Fig. 1. Schematic of the evaluated Current Sampling Based Sense Amplifier.

TABLE I
PARAMETERS OF PROPOSED SENSE AMPLIFIER

Parameter	*Symbol*	*Conditions*	*Value*
Average Read Energy	E_{read}	Full evaluation cycle	1.8 pJ/bit
Total Read Time (PUF)	T_{read}	For minimal ΔR evaluation	270 ns
Total Read Time (Memory)	T_{read}	Conventional ReRAM read (LRS vs HRS)	15 ns
Current Resolution	ΔI_{min}	Achieved with 100% yield	50 nA
Resistance Margin	ΔR	Required for Zero-BER	40 kΩ
Bit Error Rate	BER	At optimal Safe Operating Area (SOA)	0%

III. Conclusions

The functional correctness and performance of the proposed RRAM-optimized design were comprehensively verified in 130nm CMOS technology through transient and statistical Monte Carlo simulations. The circuit achieves a high current resolution of 50nA with 100% yield and a total read time of 270ns. With an average energy consumption of 1.8 pJ/bit, the design is highly competitive compared to conventional read circuits that often exceed 2–5 pJ/bit.The architecture demonstrates robust hardware security resilience; it is protected against Fault Injection attacks as disturbances are suppressed by the physical isolation of the C_{MIN} capacitors. Its configuration ensures that radical energy efficiency does not degrade the offset tolerance strictly required in cryptographic

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References

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