A Low-area, Digitally Controlled Low Dropout Regulator with Calibration Logic Optimized for RRAM Control

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I. Introduction

This work presents a low area, programmable on-chip Low Dropout (LDO) [1] regulator. The proposed design utilizes a hybrid architecture with single pass FET output power transistor and multistage digital control logic placed in the feedback loop. Design is optimized for on-chip synthesis of voltages required for the forming, programming and readout of RRAM devices [2], especially in memory and security applications. The discussed version implements a 6-bit digital control word enabling discrete voltage levels with 0.1 V step in a 0.2 - 4.0 V range making the architecture compatible with wide range of RRAM devices and applications.

II. Architecture

The core topology integrates a single PMOS pass device with a multistage digital control logic block situated within the feedback loop. The primary regulation loop relies on a cascode Error Amplifier (EA) [3] utilizing a PMOS differential input pair. This input stage configuration permits operation with a near-ground reference voltage (V_{REF} = 200 mV), directly defining the lower boundary of the regulator's tuning limit. Adjusting the output voltage by modifying the resistive feedback ratio, rather than directly tuning the reference voltage, proportionally scales the system's Noise Gain. This inherent scaling guarantees lower amplification of intrinsic noise and offset errors at low output voltage levels.

To provide the required discrete voltage scaling, the feedback network incorporates a programmable resistive divider divided into two functional segments. The upper branch acts as a 6-bit string DAC, delivering discrete voltage levels across a wide 0.2 V to 4.0 V dynamic range with an approximate step of 100 mV. To suppress voltage glitches during significant code transitions and enforce monotonic output characteristics, the resistor string is structurally segmented: the Least Significant Bits (LSBs) are governed by natural binary code, while the Most Significant Bits (MSBs) are controlled via a thermometer code. Frequency compensation is achieved via a pole-splitting technique, coupled with a series nulling resistor ensuring phase stability.

III. Conclusions

Comprehensive Monte Carlo simulations validate the robustness of the architecture. The implemented calibration routine effectively compresses the initial untrimmed output spread (from -99 mV to +80 mV) down to an accuracy of $< \pm 22$ mV, with a maximum absolute error restricted to under 48 mV across the entire code range. The regulator demonstrates strict monotonicity with maximum Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) deviations held below 0.5 LSB under worst-case process variance. Frequency-domain stability analysis confirms absolute stability, achieving a phase margin of approximately 60° under both critical zero-load scenarios and maximum extended load conditions of 1.6 mA.

TABLE I
Parameters of proposed LDO

Parameter	***Symbol***	***Conditions***	***Value***
Untrimmed Output Accuracy	$\Delta V_{\text{OUT,untrim}}$	Monte Carlo (40 runs), @ 4.0V target, Min $\sim$ Max	-99 mV $\sim$ +80 mV
Untrimmed Standard Deviation	σ_{untrim}	Monte Carlo (40 runs), @ 4.0V target	41.05 mV
Trimmed Output Accuracy	$\Delta V_{\text{OUT,trim}}$	Monte Carlo (40 runs), @ 4.0V target, Min $\sim$ Max	$< \pm 22$ mV
Trimmed Standard Deviation	σ_{trim}	Monte Carlo (40 runs), @ 4.0V target	12.78 mV
Maximum Absolute Error	Max(AE)	Post-trim, worst-case across all programmable codes	< 48 mV

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