An Asynchronous Circuit for Pattern Comparison Based on Programmable Gates and Asynchronous Incrementers and Decrementers

Marta Kolasa[1], Michał Długosz[2], Tomasz Talaśka[1,3], Rafał Długosz[1,4]
[1] Bydgoszcz University of Science and Technology, Faculty of Telecommunication, Computer Science and Electrical Engineering,
ul. Al. Prof. S. Kaliskiego 7, 85-796 Bydgoszcz, Poland
[2] Poznan University of Technology, Faculty of Control, Robotics, and Electrical Engineering,
ul. Jana Pawła II 24, 60-965 Poznań, Poland
[3] Gdansk University of Technology, Faculty of Electronics, Telecommunications and Informatics
ul. Gabriela Narutowicza 11/12, 80-233, Gdańsk, Poland
[4] Aptiv Services Poland,
ul. Podgórki Tynieckie 2, 30-399, Kraków, Poland

SUMMARY

Pattern comparison is one of the fundamental operations performed in artificial intelligence and pattern recognition systems. Such systems frequently rely on similarity measures, among which the Hamming distance is one of the most commonly used. Efficient hardware implementation of these measures requires appropriate digital components capable of both bitwise comparison and accumulation of the detected differences.

From the hardware perspective, pattern comparison essentially consists of two stages: comparing corresponding bits and counting the number of mismatches. The comparison operation is typically realized using XOR gates, while the counting stage requires accumulation mechanisms. For long patterns, for example 512- or 1024-bit vectors, the implementation becomes significantly more challenging, as circuit complexity directly influences area, power consumption, and processing speed.

Conventional implementations are usually based on standard CMOS logic gates, where each logical function is realized using classical gate structures. Although this approach is well established and reliable, it often leads to large and complex circuits, especially in massively parallel architectures requiring numerous replicated modules. Therefore, there is a strong motivation to develop more compact solutions that reduce transistor count while maintaining high efficiency.

In this work, a previously developed programmable logic gate is utilized. Depending on a control signal, the gate can operate either in NAND or NOR mode. The circuit is implemented at the transistor level and enables fully asynchronous (clock-less) operation. Moreover, its structure allows relatively simple realization of asynchronous increment and decrement circuits, which can be effectively used for accumulation of partial results during pattern comparison.

The proposed gate can therefore serve as a compact and high-speed building block for hardware implementations of Hamming distance computation. In particular, it enables construction of asynchronous counters that do not require a global clock signal, which may provide advantages in both processing speed and energy efficiency.

The gate was applied to the design of asynchronous increment/decrement (Dec/Inc) structures forming the basis of hardware-oriented pattern comparison circuits. In the proposed approach, bitwise comparison results are accumulated asynchronously, eliminating the need for global synchronization. Owing to its scalability and compact architecture, the solution is especially well suited for large-scale parallel implementations used in artificial intelligence and pattern recognition systems, where reduction of hardware complexity becomes crucial for high-dimensional data processing.

The proposed gate has been successfully integrated into complete pattern comparison architectures, including asynchronous circuits dedicated to Hamming distance evaluation. Its applicability in hardware-accelerated algorithms has been verified through transistor-level simulations, confirming its suitability for efficient implementation of pattern recognition systems.

A single Dec/Inc circuit requires $3 \cdot (b - 1)$ two-input NOR/NAND gates, where b denotes the number of bits. For a pattern length of 1024 bits, the counter resolution must satisfy $b = 11$, since the accumulated value may reach 2048. In such a case, a complete chain of 1024 Dec/Inc circuits requires 30,720 NOR/NAND gates. Compared with implementations based on conventional logic gates, this corresponds to a reduction of approximately 430,000 transistors.