Realisation of Simple Logic Circuits Using a Quantum Processing Unit - A Case Study

Mariusz Zubert, Przemysław Duniec
Department of Microelectronics and Computer Science
Lodz University of Technolog
Łódź, Poland
e-mail: mariusz.zubert@p.lodz.pl,
przemyslaw.duniec@dokt.p.lodz.pl

Krzysztof Hałagan
Department of Molecular Physics
Lodz University of Technology
Łódź, Poland
e-mail: krzysztof.halagan@p.lodz.pl

SUMMARY

This paper examines the feasibility of implementing selected classical logic circuits on a superconducting quantum processor architecture. A half-adder and an 8-bit Hamming SECDED (Single Error Correction, Double Error Detection) encoder were implemented using native gates and evaluated via noise-aware simulations based on the IBM Heron r2 quantum processor unit. The half-adder achieved functional and logical correctness with a state accuracy of 96.24%, indicating only moderate degradation under realistic noise conditions. In contrast, the significantly deeper SECDED encoder produced the ideal codeword in 73.45% of cases, while 26.55% of outcomes deviated from the expected result, including 11.82% classified as uncorrectable or ambiguous. Benchmarking results show that single-qubit gates are not the primary source of errors; instead, performance is limited by two-qubit CZ operations, circuit depth, qubit-pair non-uniformity, routing overhead, and limited readout-error mitigation. The results suggest that while simple logic circuits are feasible on current superconducting architectures, more advanced circuits may benefit from platforms with denser or more flexible connectivity.

ACKNOWLEDGMENT

The simulations were performed using the noise and error profiles of the IBM Heron r2 made available through the IBM Quantum Platform.

REFERENCES

[1] M. Skoneczny, Y. Van Rentergem, and A. De Vos, in Reversible Fourier transform chip, Poznan, Jun. 2008, pp. 281–286.

[2] S. Burignat and A. De Vos, ‘Test of a majority-based reversible (quantum) 4 bits ripple-carry adder in adiabatic calculation’, presented at the Proceedings of the 18th MIXDES 2011, Gliwice, pp. 368–373.

[3] R. Landauer, ‘Irreversibility and Heat Generation in the Computing Process’, IBM J. Res. Dev., vol. 5, no. 3, pp. 183–191, Jul. 1961, doi: 10.1147/rd.53.0183.

[4] C. H. Bennett, ‘Logical Reversibility of Computation’, IBM J. Res. Dev., vol. 17, no. 6, pp. 525–532, Nov. 1973, doi: 10.1147/rd.176.0525.

[5] T. Toffoli, ‘Reversible computing’, in Automata, Languages and Programming, vol. 85, J. Bakker and J. Leeuwen, Eds, in Lecture Notes in Computer Science, vol. 85, Berlin, Heidelberg: Springer Berlin Heidelberg, 1980, pp. 632–644. doi: 10.1007/3-540-10003-2_104.

[6] R. P. Feynman, ‘Quantum Mechanical Computers’, Opt. News, vol. 11, no. 2, p. 11, Feb. 1985, doi: 10.1364/ON.11.2.000011.

[7] A. De Vos, Reversible Computing: Fundamentals, Quantum Computing, and Applications, 1st edn. Wiley, 2010. doi: 10.1002/9783527633999.

[8] S. Burignat and A. De Vos, ‘A Review on Performances of Reversible Ripple-Carry Adders’, Int. J. Electron. Telecommun., vol. 58, no. 3, pp. 205–212, Sep. 2012,

[9] A. De Vos, S. De Baerdemacker, and Y. Van Rentergem, Synthesis of Quantum Circuits vs. Synthesis of Classical Reversible Circuits. in Synthesis Lectures on Digital Circuits & Systems. Cham: Springer International Publishing, 2018.

[10] X. Zhong and G. Jin, ‘Application of Hamming Code Based Error Correction Algorithm in Quantum Key Distribution System’, in 2020 IEEE 3rd ICET, Chengdu, China: IEEE, May 2020, pp. 857–861. doi: 10.1109/ICET49382.2020.9119567.