A 30 μW 2.4-GHz LNA With 5.6 dB NF Exploiting Trifilar Transformer Coupling for Smart AIoT Electronics

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SUMMARY

Designing a 2.4-GHz LNA in the ultra-low-power regime is challenging because both the available transconductance and the voltage headroom are severely limited. As the bias current is reduced, the designer must simultaneously preserve gain, suppress noise, maintain acceptable linearity, and realize a practical 50-Ω input match. For smart electronics, these tradeoffs are even more stringent because the receiver often serves as an always-on interface that dominates standby power. Accordingly, ultra-low-power RF design is not merely an incremental circuit problem, and it is also an enabling technology for long-lifetime AIoT nodes and future autonomous sensing platforms.

To address these issues, this work presents a 2.4-GHz ultra-low-power LNA employing complementary current reuse and trifilar transformer coupling, as shown in Fig. 1. By merging two source-coupled transformer paths into a single trifilar structure, the proposed design simultaneously boosts the effective gm of the NMOS and PMOS devices, improves magnetic coupling efficiency, and reduces area overhead. In addition, a g_m/I_D-based bias design is adopted to maximize current efficiency in subthreshold operation, while complementary bias optimization helps alleviate even-order distortion.

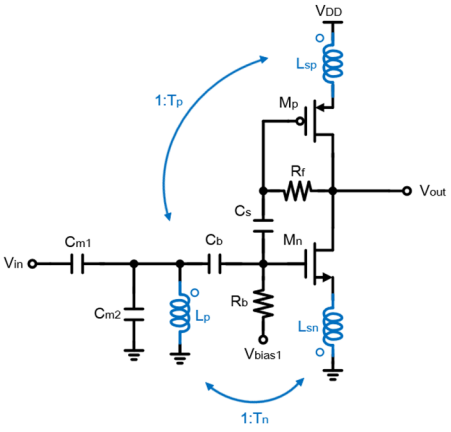

Fig. 1. Proposed current reuse LNA.

Fig. 2 shows the proposed LNA implemented in a 90-nm CMOS technology. The LNA consumes only 30 μW from a 0.6-V supply. The LNA achieves a voltage gain of 13.8 dB, a noise figure (NF) of 5.6 dB, and an input third-order intercept point (IIP3) of -6.2 dBm at 2.4 GHz. TABLE I compares the proposed design with representative ultra-low-power LNAs, and . The proposed design achieves a FoM of 14.8. With its strong energy efficiency and compact passive implementation, the proposed LNA is a promising RF front-end building block for BLE devices, always-on wireless sensing, AIoT nodes, and future battery-operated smart electronics.

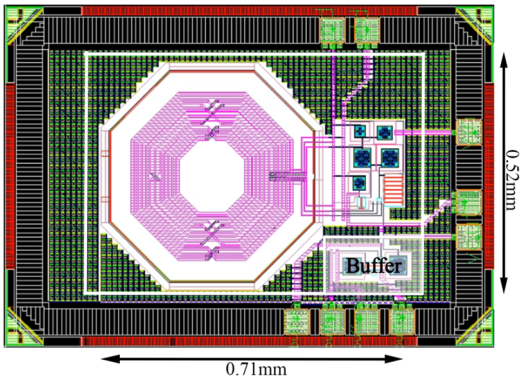

Fig. 2. Chip layout of proposed LNA.

TABLE I.
COMPARISONS OF ULTRA-LOW-POWER LNA

Reference	This work	[1]	[3]	[4]	[10]	[11]	[12]
CMOS Tech. (nm)	90	90	28	65	40	180	130
Frequency (GHz)	2.4	0.04 -0.8	0.02 -4.5	2.4	2.4	2.4	2.4
A_V (dB)	13.8	14.3	15.2	17.4	14.2	14.7	16.3
NF (dB)	5.6	6.5	2.1	2.8	3.3	4.8	1.7
IIP3 (dBm)	-6.2	-5.7	-3.5	-10.7	-13.2	2	-0.9
V_{DD} (V)	0.6	1.2	1	0.7	0.8	1.8	0.5
Power (mW)	**0.03**	0.49	4.5	0.48	0.03	0.58	1.44
***FOM**	**14.8**	0.8	0.9	1.5	7.2	7.4	7.7

$$FoM = \frac{Gain(V/V)\cdot IIP3(mW)}{(F-1)\cdot P_{DC}(mW)}$$