A Pathfinding PDK Toward 10nm FD-SOI Technology

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***Abstract*—The FAMES pilot line is a unique opportunity for Europe to promote advanced semiconductor technologies, one of its objectives being to develop a pathfinding PDK for a future 10nm FD-SOI process technology. This work will describe the path taken from the first process assumptions to designing standard cells libraries and delivering the PDK, with an emphasis on existing FD-SOI technologies, key design rules, associated layout constraints on standard cells topology, Design-Technology Co-Optimization (DTCO) and validation of the PDK on different designs.**

***Keywords*—FAMES, FD-SOI, 10nm, PDK, DRM, model, DRC, LVS, PEX, TCAD, simulation, DTCO, Standard cells, SSTI**

SUMMARY

Building a pathfinding PDK requires a wide range of skills and data, assembled altogether with a validation loop as shown on Fig. 1. This work will focus on how we applied this loop to the construction of our 10nm FD-SOI technology, aiming at a more Moore projection of existing FD-SOI industrial process nodes. We will go through technological features summarized on Table I in order to detail what makes this technology different from the previous nodes and which gains can be expected from a physical implementation point of view.

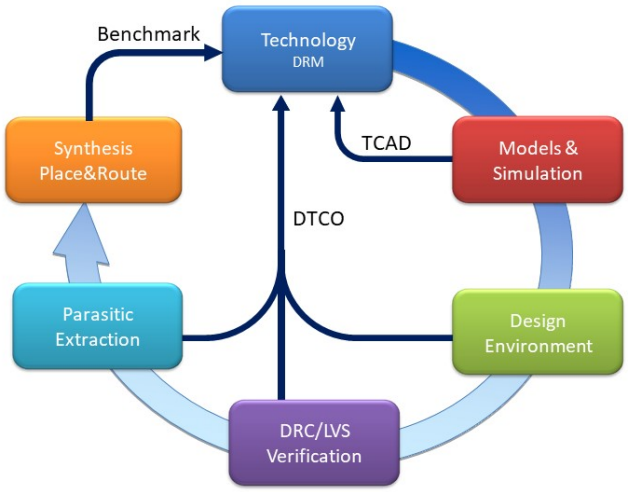

Fig. 1. Validation loop of a PDK from design perspective

TABLE I.
10NM FD-SOI TECHNOLOGICAL FEATURES

CPP (nm)	68
Channel (nm)	5.5 (Si NMOS, SiGe PMOS)
BOX (nm)	20
Lg (nm)	20
Strain channel	SSOI or local strain
Gate	Gate first
Dual metal gate	Al/La dipoles
Gate patterning	SADP
Spacer	Low-k
In-situ doped source/drain	SiGe-B (PMOS), Si-P (NMOS)
Crossing RX contact	Anti-Punch-Through (APT) layer

As part of the FAMES Open Access calls [1], this 10nm FD-SOI pathfinding PDK can already be downloaded for digital design evaluation. It contains a complete Design Rules Manual (DRM) with Front-End Of Line, Middle Of Line and Back-End-Of-Line description, Eldo transistor electrical simulation models, Virtuoso environment for schematic and layout with single gate oxide transistor pcells, Calibre DRC and LVS decks, Star-RCXT parasitic extraction flow, technology files for DC-Compiler digital synthesis and Innovus Place&Route as well as 16 standard cell libraries with various Vt, poly bias and process options for a total count of around 1000 logic gates.

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REFERENCES

[1] https://fames-pilot-line.eu/open-access/