TSRI Platform for Advanced Packaging and Silicon Photonics

Ecosystem for Industry–Academia–Research Collaboration

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I. Introduction

The recent rapid growth of AI applications has emerged as a major catalyst for the entire semiconductor industry. While global semiconductor revenue was previously projected to hit $1 trillion by 2030, the latest forecasts indicate that the market could reach this milestone as early as this year. However, ensuring the sustainable development of AI hinges critically on achieving high energy efficiency. There are two primary avenues to achieving energy-efficient AI: (1) continuing transistor scaling and lowering bias voltage to minimize power consumption; and (2) utilizing advanced packaging and silicon photonics Co-Packaged Optics (CPO) to minimize data transmission power loss.

For an extended period, global advanced packaging capacity has been severely supply-constrained, making it difficult for academia, research institutes, and startups to access cutting-edge packaging resources. To address this, the Taiwan Semiconductor Research Institute (TSRI) under the National Institutes of Applied Research (NIAR) has established the "Chip-Level Advanced Packaging R&D Platform". Leveraging national-level scientific research capabilities, this platform fills a critical gap in the semiconductor innovation ecosystem.

Regarding the Silicon Photonics CPO platform, TSRI has established an end-to-end technological platform. Utilizing the imec silicon photonics process, we have developed device models including Micro-ring modulators (MRM), photo-detectors, lasers, and optical paths. Furthermore, we have developed an integrated design and simulation flow with high-speed electrical transceiver EICs, completed the co-packaged optoelectronic integrated design under a 2.5D architecture, and concurrently driven the development of Co-Packaged Optics technology alongside international collaborations.

The core concepts of TSRI's services are an open, one-stop integrated resource-sharing platform and industry–academia–research collaboration. Based on well-established hardware infrastructure and software platforms, domestic and international research teams are able to share resources in semiconductor manufacturing, packaging and testing, IC design, silicon intellectual property (IP), and system integration. These shared resources in TSRI help shorten technology development and validation cycles, lower the barriers for universities and research institutions to engage in advanced semiconductor research, and support industry in the early-stage validation of emerging technologies and prototype systems.

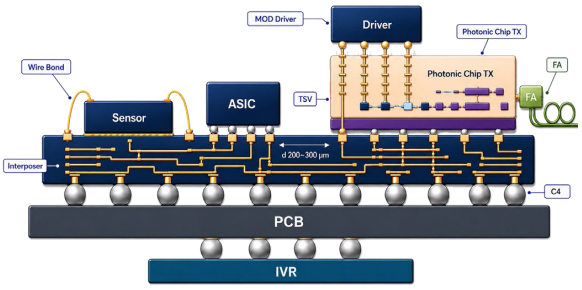

Fig. 1. Illustration of the advanced package platform in TSRI

II. TSRI Platform for Research Collaboration

A. Advanced Packaging Platform

The TSRI platform for advanced packaging, as illustrated in Fig. 1. In this platform, the heterogeneous integration of dies from different sources can be implemented.

- **High-Density Interconnects**: Successfully achieved a chip-level 50 µm pitch high-density interconnect with a yield approaching 90%.
- **Substrate-less CoCoB Architecture**: This Chip-on-Chip-on-Board (CoCoB) packaging architecture removes the substrate to shorten the signal transmission paths, boosting integration density and system performance. Besides cost reduction, this approach also enables die-level bonding, that enables the supports for academic research and startups to conduct highly flexible, low-cost heterogeneous integration.
- **Highly Flexible Integration**: This technology efficiently integrates computing processors, memory, and various sensors, including environmental and biomedical sensors, to build smart, multi-sensing micro-physical entities and Edge AI chip modules. This expands their impact across smart devices, healthcare, and IoT applications.

B. Silicon Photonics CPO Platform

TSRI has established a one-stop platform for silicon photonics CPO, from design, simulation, fabrication, packaging to verification, as illustrated in Fig. 2.

- **Optical & Electrical Co-simulation and Design**: We not only provides the comprehensive simulation and design software, but also provide the reference designs, based on world-leading foundries such as imec, TSMC, STMicro-electronics, and Ligentec.
- **Co-package Optics**: The 2.5D CPO platform integrates PIC and EIC using TSV and silicon-interposer, with micro-bump co-packaging and array fiber interfaces. The III-V sources, such as InP lasers, LNO modulators, and SOAs, can also be directly transferred onto silicon photonic wafers.
- **High speed Opto-electronic Measurement**: TSRI is equipped with an advanced probe station with optical–electrical interfaces, O- and C-band lasers and detectors, and a 110 GHz four-port VNA for high-speed opto-electronic measurements. Using a 224 Gbps PAM4 setup with PPG, AWG, DSO, and RTO instruments, this platform supports complete data transmission testing up to 110 GHz.

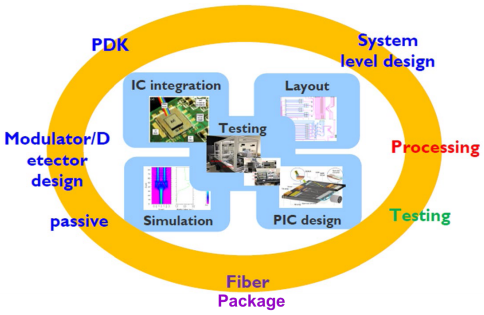

Fig. 2. Illustration of the silicon photonics CPO platform in TSRI