Broadening Participation in Open-Source Integrated Circuit Design and Fabrication Through IEEE Activities

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EXTENDED ABSTRACT

Even though the semiconductor industry is expanding rapidly, access to realistic chip design and fabrication environments remains uneven across institutions, countries, and stages of professional development. Although integrated circuit design is central to modern electronics, participation is limited by the high cost of commercial electronic design automation tools, the complexity of advanced design flows, the shortage of faculty trained in application-specific integrated circuit (ASIC) methodologies, and the cost of fabrication itself. Consequently, many students study analog, digital, or mixed-signal IC theory without ever completing the path from concept to silicon and measurement, which limits their preparation for the workforce.

Open-source process design kits, community-developed electronic design automation (EDA) flows, and accessible prototyping programs are reshaping this landscape. Beyond the release of open PDKs such as Sky130A, GF180MCU-D, and IHP-SG13G2, a broader ecosystem has emerged that combines design infrastructure, training, mentoring, collaboration, and pathways to fabrication. IEEE has become a key institutional actor in this transition through coordinated activities across the Electron Devices Society (EDS), the Solid-State Circuits Society (SSCS), and the Circuits and Systems Society (CASS), helping transform open-source silicon into a scalable platform for education and professional development.

For example, the SSCS PICO Open-Source Chipathon provides a recurring framework for collaborative design, mentoring, and tapeout-oriented activities. The program received 61 submissions in 2021 and 54 in 2022. Later editions expanded to include themes such as analog test macros, analog layout automation, digital building blocks, MOSbius-style educational chips, and AI-assisted analog automation. In 2025, the Chipathon offered free silicon through GlobalFoundries' 180 nm GF180MCU-D technology, with all designs remaining open source. This is especially significant because fabrication costs are often the most difficult barrier for students and small research groups to overcome.

Other IEEE initiatives broaden this impact across regions and communities. LatinPractice, supported by EDS and later expanded into the global ChipPractice program, has already reached about 1,500 participants. These programs were created to attract new generations to chip design and establish career pathways into the semiconductor sector. They support local bootcamps that combine semiconductor and microelectronics theory with hands-on laboratory activities linking theory and experimentation. Meanwhile, UNIC-CASS has focused on increasing access in low- and middle-income regions with limited opportunities by combining open-source tools and open PDKs with tapeout-oriented mentoring and training. More recently, the IEEE Division I Open Silicon Initiative expanded fabrication access through financial support from EDS, SSCS, CASS, the IEEE Nanotechnology Council, and the Council on Electronic Design Automation (CEDA). Its bootcamp campaign for the first quarter of 2026 was designed for 212 leaders and 1,875 participants. As of April 28, 2026, the initiative had already reported 22 workshops in 17 countries, with 648 participants, 60 designs, and 20 PCBs. Its support model is particularly important because it reduces or fully covers fabrication-related costs by providing design tiles, shipping, PCBs, and Tiny Tapeout support.

These initiatives have broad educational, economic, and strategic significance. They provide a pathway from introductory training to publishable, testable, and shareable silicon, while reducing or eliminating tapeout costs that would otherwise prevent many universities, especially those in developing regions, from participating. They also strengthen the semiconductor workforce pipeline by giving students hands-on experience in design, verification, fabrication, and post-silicon testing. For the open-source silicon ecosystem to mature, access must be defined by more than the availability of open PDKs; it must also include funding, mentoring, fabrication sponsorship, test hardware, and opportunities for dissemination. IEEE activities demonstrate that this integrated model is feasible, scalable, and increasingly global.