

Considerations on the Design of Resilient 2.5-3D Heterogeneous, Multilayer Interposer Systems for Chip Lifecycle Management

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SUMMARY

Technology scaling, which made electronics accessible and affordable for almost everyone on the globe, has advanced integrated circuit (IC) and electronics since the sixties. Nevertheless, it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry.

This tutorial addresses the background mechanisms impacting resilience of ICs and shows how on-chip lifecycle management (OCLM) closes the loop when combined effects are unknown or untestable. Shrinking nodes and stacking heterogeneous dies do open many new failure modes (thermal, EMI, aging, SEU, process variation, PDN/noise coupling, electromigration, cross-talk, TSV/interposer faults) and many combined effects simply cannot be exhaustively predicted before deployment.

This tutorial discusses such failure modes and proposes mitigation solutions. Such techniques are based on the massive deployment of on-chip cross-layer sensors that are placed in strategic points of the chiplets and interposer, a data wrapper interface & management hub that is responsible to process and store the collected data from the sensors in a way to create an in-mission history of events, and on-chip analytics. The sensors can monitor from aging, power-supply noise activity and transient faults in memory elements up to system-level transactions in system bus, processor cores and memory IPs, from dies to the interposer level. IEEE and IEC standards are used to support data monitoring and collection processes.

The analytics engine can be implemented based on simple/straightforward data structures such as LUT and CAM, or be based on advanced Machine Learning/Artificial Intelligence (ML/AI) algorithms such as DyNN. ML is used to predict in-field system reliability according to predefined values. The ultimate goal is to perform on-chip lifecycle management to trade, in-mission mode, power, performance, reliability and lifespan. Concrete examples implemented in FPGAs as well as chips manufactured at IHP will illustrate the tutorial.

Duration of the Talk: appr. 40 minutes.

Target Audience: IC- and system-level designers (engineers and PhD students) working on critical applications such as aerospace, defense & security, automotive.

Short Bio: Fabian Vargas obtained the Ph.D. Degree in Microelectronics from the *Institut National Polytechnique de Grenoble* (INPG), France, in 1995. At present, he is Senior Scientist at IHP - Leibniz Institute for High Performance Microelectronics, Germany, where he works on the design of on-chip sensors and cross-layer resilience for aerospace systems. Vargas has served as Technical Committee Member and Guest-Editor in many IEEE-sponsored conferences and journals. He holds several patents and published over 200 refereed papers. Vargas was researcher of the BR National Science Foundation from 1996 to 2023. He co-founded the IEEE-Computer Society Latin American Test Technology Technical Council (IEEE LA-TTTC) in 1997 and the IEEE Latin American Test Symposium (LATS) in 2000. He received the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of these groups. Vargas is Golden Core Member of the IEEE Computer Society and Senior Member of the IEEE.

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