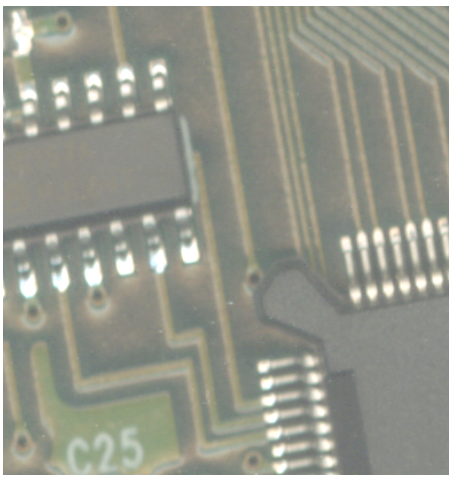
Book of Abstracts of 27th International Conference

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

MIXDES 2020



Łódź, Poland
June 25 – 27, 2020

Organised by:

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

in co-operation with:

Poland Section IEEE - ED & CAS Chapters

Section of Microelectronics & Electron Technology
and Section of Signals, Electronic Circuits & Systems
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee
of International Union of Radio Science – URSI

supported by:

Ministry of Science and Higher Education

Edited by
Andrzej Napieralski

Lodz University of Technology
Department of Microelectronics and Computer Science
ul. Wólczańska 221/223
90-924 Łódź, Poland

Phone: +48 42 631 26 45
Fax: +48 42 638 03 27
E-mail: napier@dmcs.pl
Web: http://www.mixdes.org

Dofinansowano z programu „Doskonała nauka” Ministra Nauki i Szkolnictwa Wyższego.

Printed by
Department of Microelectronics and Computer Science, Lodz University of Technology
ul. Wólczańska 221/223, 90-924 Łódź, Poland

Preface

Since 26 years the MIXDES Conference is a forum devoted to recent advances in micro- and nanoelectronics design methods, modelling, simulation, testing and manufacturing technology in diverse areas including embedded systems, MEMS, sensors, actuators, power devices and biomedical applications.

Due to the coronavirus (COVID-19) pandemic, the Scientific and Organising Committees have decided this year to hold a virtual conference. We are extremely disappointed that we will not meet in person but we hope, that despite this, the presentations and discussions will be efficient and fruitful.

The program of the conference consists of three days of sessions starting each day with invited talks. The following invited talks will be presented:

- *Maximizing the Efficiency of CMOS Front-illuminated Solar cell for Self-powered IoT Sensor Applications*
  Poki Chen (National Taiwan University of Science and Technology, Taiwan)
- *Miniaturized Sensors for Planetary Applications*
  Mina Rais-Zadeh (NASA Jet Propulsion Laboratory, California Institute of Technology, USA)
- *Semiconducting Oxide Electronics for Newly Emerging Applications*
  Arokia Nathan (Cambridge Touch Technologies, Cambridge, UK)
- *Sensor Design Made by Bosch*
  Mike Schwarz (Robert Bosch GmbH, Germany)
- *The Qucs/QucsStudio and Qucs-S Graphical User Interface: An Evolving "White-Board" for Compact Device Modelling and Circuit Simulation in the Current Era*
  Mike Brinson (London Metropolitan University, UK)

The program of MIXDES 2020 also includes 2 special sessions:

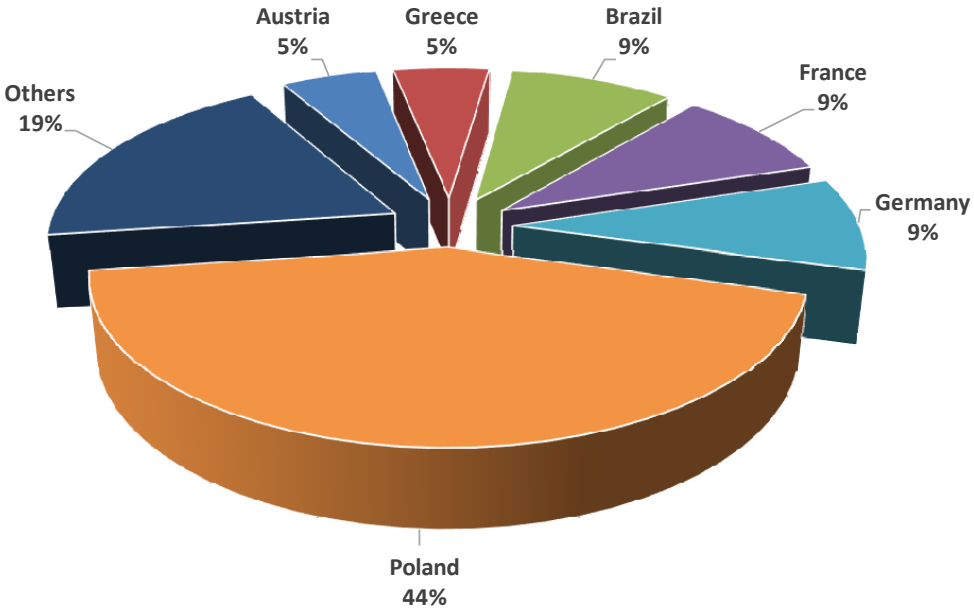
- *Compact Modeling Support for Micro and Nanoelectronic System Development*
  organised by D. Tomaszewski (Institute of Electron Technology, Poland) and W. Grabiński (GMC, Switzerland)
- *Fusion Diagnostics I&C Workshop*
  organised by S. Simrock (ITER, France) and D. Makowski (Lodz University of Technology, Poland)

In addition to the technical sessions, opportunities for the conference attendees will be (free of charge) EDS Distinguished Lecturer Mini-Colloquium: “Semiconductor-based sensors - technology, modeling, applications", organized by ED Poland Chapter with collaboration of Institute of Electron Technology, Warsaw, Poland. It will takes place June 27, 2020.

Number of accepted papers and authors by country

Country	Number of		Country	Number of		Country	Number of	
	papers	co-authors		papers	co-authors		papers	co-authors
Austria	2	7	Iran	1	3	Slovakia	1	2
Brazil	2	12	Italy	1	2	Switzerland	0	1
Czech Republic	0	1	Lithuania	1	2	Taiwan	1	1
Egypt	0	1	Peru	1	3	UK	3	2
France	2	12	Poland	27	58	USA	1	3
Germany	4	12	Portugal	1	2	**Total:**	**50**	**133**
Greece	1	7	Saudi Arabia	1	2			

Number of Authors by Country



All regular papers were reviewed and selected from submissions from 19 countries. The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing contributed papers.

We hope that you are safe and healthy and remain so, and we will meet together next year in Wrocław, June 24-26, 2021.

Łódź, June 2020

Andrzej NAPIERALSKI
Department of Microelectronics and Computer Science
Lodz University of Technology, Poland
General Chairman of MIXDES 2020

International Programme Committee

Prof.	M. Bucher	Technical University of Crete, Greece
Prof.	J. Cabestany	Universitat Politecnica de Catalunya, Spain
Prof.	J. Collet	LAAS - CNRS, Toulouse, France
Prof.	A. Dąbrowski	Poznan University of Technology, Poland
Prof.	G. De Mey	University of Ghent, Belgium **(Vice-Chairman)**
Prof.	J. Deen	McMaster University, Canada
Prof.	M.H. Fino	Universidade Nova de Lisboa, Portugal
Dr.	D. Foty	Gilgamesh Associates, USA
Prof.	L. Golonka	Wrocław University of Science and Technology, Poland
Prof.	K. Górecki	pGdynia Maritime University, Poland
Dr.	W. Grabiński	GMC, Switzerland
Prof.	P. Gryboś	AGH University of Science and Technology, Poland
Prof.	V. Hahanov	Kharkiv National University of Radioelectronics, Ukraine
Prof.	A. Handkiewicz	Poznan University of Technology, Poland
Prof.	A. Hatzopoulos	Aristotle University of Thessaloniki, Greece
Prof.	S. Hausman	Lodz University of Technology, Poland
Dr.	G. Jabłoński	Lodz University of Technology, Poland
Prof.	A. Jakubowski	Warsaw University of Technology, Poland
Prof.	A. Kos	AGH University of Science and Technology, Poland
Prof.	W. Kuźmicz	Warsaw University of Technology, Poland
Prof.	C. Lallement	Strasbourg University, France
Prof.	M. Lobur	State University Lviv, Ukraine
Dr.	M.M. Louerat	Université Pierre et Marie Curie, Paris, France
Prof.	T. Łuba	Warsaw University of Technology, Poland
Prof.	B. Macukow	Warsaw University of Technology, Poland
Prof.	J. Madrenas	Universitat Politecnica de Catalunya, Spain
Dr.	D. Makowski	Lodz University of Technology, Poland
Prof.	A. Martinez	LAAS - CNRS, Toulouse, France **(Honorary Chairman)**
Prof.	A. Materka	Lodz University of Technology, Poland
Prof.	W. Mathis	Leibniz University of Hannover, Germany
Prof.	J.M. Moreno	Universitat Politecnica de Catalunya, Spain
Dr.	M. Napieralska	Lodz University of Technology, Poland
Prof.	A. Napieralski	Lodz University of Technology, Poland **(General Chairman)**
Prof.	J. Nishizawa	Semiconductor Research Institute, Japan
Dr.	J.L. Noullet	INSA de Toulouse, France
Prof.	L. Opalski	Warsaw University of Technology, Poland
Prof.	A. Pfitzner	Warsaw University of Technology, Poland **(Programme Chairman)**
Prof.	E. Piętka	Silesian University of Technology, Poland
Prof.	W. Pleskacz	Warsaw University of Technology, Poland
Dr.	B.F. Romanowicz	Nano Science and Technology Institute, USA
Prof.	J.A. Rubio	Universitat Politecnica de Catalunya, Spain
Prof.	A. Rybarczyk	Poznan University of Technology, Poland
Dr.	J.-M. Sallese	Swiss Federal Institute of Technology, Switzerland
Prof.	D. Sankowski	Lodz University of Technology, Poland
Dr.	M. Schwarz	Robert Bosch GmbH, Germany
Prof.	N. Stojadinović	University of Niš, Serbia
Prof.	T. Szmuc	AGH University of Science and Technology, Poland
Dr.	P. Śniatała	Poznań University of Technology, Poland
Prof.	M. Tadeusiewicz	Lodz University of Technology, Poland
Dr.	D. Tomaszewski	Institute of Electron Technology, Warsaw, Poland
Dr.	P. Tounsi	INSA de Toulouse, France
Dr.	M. Turowski	Alphacore, Inc.,USA
Prof.	R. Ubar	Tallinn Technical University, Estonia
Prof.	G. Wachutka	Technische Universitaet Muenchen, Germany
Prof.	K. Wawryn	Technical University of Koszalin, Poland
Prof.	B. Więcek	Lodz University of Technology, Poland
Prof.	S. Yoshitomi	Toshiba Corporation, Japan
Prof.	J. Zarębski	Gdynia Maritime University, Poland
Prof.	M. Zubert	Lodz University of Technology, Poland

Organising Committee

Prof.	A. Napieralski	(Chairman)
Dr.	M. Orlikowski	(Secretary)
Dr.	M. Napieralska	(Vice-Chairman)
Dr.	G. Jabłoński	Department of Microelectronics and Computer Science, Lodz University of Technology, Poland
Prof.	W. Kuźmicz	Institute of Micro- and Optoelectronics, Warsaw University of Technology, Poland

Table of Contents

6 Power Electronics

7 Signal Processing

8 Embedded Systems

MIXDES 2020 Programme

MIXDES 2020 Timetable

Day 1	Thursday, June 25th, 2020	
	ROOM A	ROOM B
08:50	Conference Opening	
09:00	Plenary Session I	
10:00	Session 1 (Part 1)	Session 7
11:15	Break	
11:30	Poster Session	

Day 2	Friday, June 26th, 2020		
	ROOM A	ROOM B	ROOM C
09:00	Plenary Session II		
10:00	Session 1 (Part 2)	Special Session I	Special Session II (Part 1)
11:30	Break		
12:00	Session 1 (Part 3) & 4	Session 3	Special Session II (Part 2)

Day 3	Saturday, June 27th, 2020		
	ROOM A	ROOM B	ROOM C
08:30	Plenary Session III		
09:30	Break		
10:00	Session 8 (Part 1)	Session 2	IEEE ED Poland MQ (Part 1)
11:30	Break		
12:00	Session 8 (Part 2)	Session 5 & 6	IEEE ED Poland MQ (Part 2)

The MIXDES 2020 Conference sessions are organized using Microsoft Teams platform. We recommend you to install MS Teams application on your computer. It is also possible to connect using MS Teams web application, but note that not all browsers are compatible.

Here are the links for on-line MIXDES 2020 Microsoft Teams sessions for each room valid for all conference days:

ROOM A

ROOM B

ROOM C

For testing purposes we have prepared a test meeting, where we can assist you with testing your connection. Every working day 9:00-11:00 CET till the conference and during the first day conference sessions, we will keep the test meeting opened. You can connect to it, and our colleagues will help you with testing your voice/video connection and screen presentation from your computer. For other hours, please contact us via email (mixdes2020@dmcs.p.lodz.pl).

TEST MEETING

MIXDES 2020 Schedule

Day 1: June 25th 2020 (Thursday)

Time	Room A
08:50	**Conference Opening** Chairman: Prof. A. Pfitzner
09:00	**Plenary Session I** Chairman: Prof. A. Pfitzner *Maximizing the Efficiency of CMOS Front-illuminated Solar cell for Self-powered IoT Sensor Applications* P. Chen (National Taiwan Univ. of Science and Techn., Taiwan)
10:00	**Session 1 (Part 1)**: Design of Integrated Circuits and Microsystems Chairman: Prof. A. Pfitzner *A Capacitive Feedback 80 dBOhm 1.1 GHz CMOS Transimpedance Amplifier with Improved Biasing* A. Romanova, V. Barzdenas (Vilnius Gediminas Tech. Univ., Lithuania) *A Survey on the Application of Parametric Amplification in Next Generation Digital RF Transceivers* L.M. Pires, J.P. Oliveira (Univ. Nova de Lisboa, Portugal) *A W-band SiGe BiCMOS Transmitter Based on K-band Wideband VCO for Radar Applications* M. Kucharski, M. Widlok, R. Piesiewicz (SIRC Sp. z o.o., Poland)
11:15	***Break***
11:30	**Poster Session** Chairman: Prof. W. Pleskacz *A New Architecture of Thermometer to Binary Decoder in a Low-Power 6-bit 1.5GS/s Flash ADC* M. Keyhanazar, A. Kalami (Islamic Azad Univ., Urmia Branch, Iran), A. Amini (Sina Bioelectronics Company, Iran) *Low Hardware Complexity Filters for On-Chip Algorithm Used in Air Pollution Sensors for Dense Urban Areas in Smart Cities* Z. Długosz, M. Rajewski (UTP Univ. of Science and Techn., Poland), M. Banach (Poznan Univ. of Techn., Poland), T. Talaśka, R. Długosz (UTP Univ. of Science and Techn., Poland) *On Applications of Fractional Derivatives in Circuit Theory* J. Gulgowski (Univ. Gdansk, Poland), T. Stefanski (Gdansk Univ. of Techn., Poland), D. Trofimowicz (SpaceForest Ltd., Poland) *Simulation of Signal Propagation Along Fractional Order Transmission Lines* T. Stefanski (Gdansk Univ. of Techn., Poland), D. Trofimowicz (SpaceForest Ltd., Poland), J. Gulgowski (Univ. Gdansk, Poland) *Combining Epsilon-similar Fuzzy Rules for Efficient Classification of Cardiotocographic Signals* M. Jezewski, R. Czabanski, J.M. Leski (Silesian Univ. of Techn., Gliwice, Poland), A. Matonia (Łukasiewicz Research Network - Institute of Med. Techn. and Equipm., Poland), R. Martinek (VSB - Tech. Univ. of Ostrava, Czech Republic) *Modified Particle Swarm Optimization Algorithm Facilitating Its Hardware Implementation* M. Rajewski, Z. Długosz, R. Długosz, T. Talaśka (UTP Univ. of Science and Techn., Poland) *Indoor Precise Infrared Navigation* P. Marzec, A. Kos (AGH Univ. of Science and Techn., Poland)

Time	Room B
10:00	**Session 7**: Signal Processing Chairman: Prof. P. Gryboś *Fusion of Position Adjustment from Vision System and Wheels Odometry for Mobile Robot in Autonomous Driving* J. Zwierzchowski (Lodz Univ. of Techn., Poland), D. Pietrala (Kielce Univ. of Techn., Poland), J. Napieralski (Lodz Univ. of Techn., Poland) *Marker Detection Algorithm for the Navigation of a Mobile Robot* A. Annusewicz (Kielce Univ. of Techn., Poland), J. Zwierzchowski (Lodz Univ. of Techn., Poland) *Testing Stability of Digital Filters Using Multimodal Particle Swarm Optimization with Phase Analysis* D. Trofimowicz (SpaceForest Ltd., Poland), T. Stefanski (Gdansk Univ. of Techn., Poland)

Day 2: June 26th 2020 (Friday)

Time	Room A
09:00	**Plenary Session II** Chairman: Prof. W. Kuźmicz *Sensor Design Made by Bosch* M. Schwarz (Robert Bosch GmbH, Germany) *The Qucs/QucsStudio and Qucs-S Graphical User Interface: An Evolving "White-Board" for Compact Device Modeling and Circuit Simulation in the Current Era* M. Brinson (London Metropolitan Univ., UK)
10:00	**Session 1 (Part 2)**: Design of Integrated Circuits and Microsystems Chairman: Prof. M. Zubert *Active Feedbacks Comparative Analysis for Charge Sensitive Amplifiers Designed in CMOS 40 nm* G. Węgrzyn, R. Kłeczek, P. Kmon (AGH Univ. of Science and Techn., Poland) *ASIC Architecture and Implementation of RED Scheduler for Mixed-Criticality Real-Time Systems* L. Kohutka, V. Stopjaková (Slovak Univ. of Techn. in Bratislava, Slovakia) *Low Power Preamplifier for Biomedical Signal Digitization* N. ALjehani (King Saud Univ., Saudi Arabia), M. Abbas (King Saud Univ., Saudi Arabia and Assiut University, Egypt) *Multichannel Programmable Readout IC for Photodiodes Array* P. Pieńczuk, C. Kołaciński, A. Szymański, P. Janus, K. Kucharski, D. Obrębski, M. Zbieć, M. Jakubowski (Łukasiewicz Research Network - Institute of Electron Techn., Poland)
11:30	***Break***
12:00	**Session 1 (Part 3) & Session 4**: Microelectronics Technology and Packaging & Design of Integrated Circuits and Microsystems Chairman: Dr. P. Śniatała *Challenges in Performance Improvement of Silicon Systems on Chip in Advanced Nanoelectronics Technology Nodes* A. Malinowski (Globalfoundries, Germany), S.K. Mishra (Globalfoundries, USA) *Recessed and P-GaN Regrowth Gate Development for Normally-off AlGaN/GaN HEMTs* C. Haloui (LAAS-CNRS and CEA-Tech, France), G. Toulon (EXAGAN, France), J. Tasselli (LAAS-CNRS, France), Y. Cordier, E. Frayssinet (CRHEA-CNRS, France), K. Isoird, F. Morancho (LAAS-CNRS, France), M. Gavelle (CEA-Tech, France) *CMOS Interface for Capacitive Sensors with Custom Fully-Differential Amplifiers* M. Jankowski, P. Zając, P. Amrozik, M. Szermer (Lodz Univ. of Techn., Poland) *Comparative Analysis of Power Consumption of Parallel Prefix Adders* I. Brzozowski (AGH Univ. of Science and Techn., Poland) *Relocatable Partial Bitstreams for Overlay Architectures atop FPGAs* Z. Mudza (Lodz Univ. of Techn., Poland)

Time	Room B
10:00	**Special Session I**: Compact Modeling Support for Micro and Nanoelectronic System Development Chairmen: Dr. D. Tomaszewski and Dr. W. Grabiński *Compact Model For Continuous Microfluidic Mixer* A. Bonament, A. Prel (ICube, France), J.-M. Sallese (EPFL, Switzerland), M. Madec, C. Lallement (ICube, France) *Impact of Dynamic Trapping on High Frequency Organic Field-Effect Transistors* M. Mueller, S. Donnhäuser, S. Mothes, A. Pacheco-Sanchez, K. Haase, S. C. B Mannsfeld, M. Claus (Tech. Univ. Dresden, Germany) *Parameter Extraction for a Simplified EKV-model in a 28nm FDSOI Technology* K. Bajer, S. Paul, D. Peters-Drolshagen (Univ. Bremen, Germany) *Qucs-S/QucsStudio/Octave Schematic Synthesis Tools for Device and Circuit Parameter Extraction from Measured Characteristics* M. Brinson (London Metropolitan Univ., UK)
11:30	***Break***
12:00	**Session 3**: Analysis and Modelling of ICs and Microsystems Chairman: Dr. D. Tomaszewski *A Process, Voltage and Temperature Dependent Modeling Methodology for Industrial Requirements* I. Sejc, R. Kappel (ams AG, Austria) *Capacitance Deviation Caused by Mechanical Deformation of MEMS Inertial Structure* J. Nazdrowicz, A. Stawiński, A. Napieralski (Lodz Univ. of Techn., Poland) *Noise Resistance Estimation for a GaN JFET Using Small Signal Measurements for an X-band LNA* E. Karagianni (Hellenic Naval Academy, Greece), C. Lessi (National Tech. Univ. Athens, Greece), C. Vazouras (Hellenic Naval Academy, Greece), A. Panagopoulos (National Tech. Univ. Athens, Greece), G. Deligeorgis, G. Stavrinidis, A. Kostopoulos (Foundation for Research and Techn. Hellas, Greece) *Subban Structure and Ballistic Conductance of a Molybdenum Disulfide Nanoribbon in Topological 1T' Phase: A k.p Study* V. Sverdlov, A.-M. El-Sayed, S. Selberherr (Tech. Univ. Wien, Austria)

Time	Room C
10:00	**Special Session II (Part 1)**: Fusion Diagnostics I&C Workshop Chairman: Dr. S. Simrock
11:30	***Break***
12:00	**Special Session II (Part 2)**: Fusion Diagnostics I&C Workshop Chairman: Dr. D. Makowski

Day 3: June 27th 2020 (Saturday)

Time	Room A
08:30	**Plenary Session III** Chairman: Prof. W . Kuźmicz *Miniaturized Sensors for Planetary Applications* M. Rais-Zadeh (NASA Jet Propulsion Lab., California Institute of Techn., USA) *Semiconducting Oxide Electronics for Newly Emerging Applications* A. Nathan (Cambridge Touch Technologies, Cambridge, UK)
09:30	***Break***
10:00	**Session 8 (Part 1)**: Embedded Systems Chairman: Dr. D. Makowski *Consistency Preserving Development of Embedded Systems Using AADL* T. Szmuc, W. Szmuc (AGH Univ. of Science and Techn., Poland) *Rigorous Development of Embedded Systems Supported by Formal Tools* T. Szmuc, W. Szmuc (AGH Univ. of Science and Techn., Poland) *Linux Kernel Driver for External Analog-to-Digital and Digital-to-Analog Converters* P. Skrzypiec, Z. Marszałek (AGH Univ. of Science and Techn., Poland) *Multipoint Wireless Humidity and Temperature Monitoring Network for HVAC Systems Validation* M. Zbieć, D. Obrębski (Sieć Badawcza Łukasiewicz - Instytut Technologii Elektronowej, Poland)
11:30	***Break***
12:00	**Session 8 (Part 2)**: Embedded Systems Chairman: Dr. D. Makowski *Performance Constraints of Machine Learning on Embedded Devices* Ł. Grzymkowski, T. Stefanski (Gdansk Univ. of Techn., Poland) *Sensor Fusion Algorithm Implementation on Microchip PIC Microcontroller* S. Salas, C. Valdez, K. Lau (Univ. Peruana de Ciencias Aplicadas, Peru), M.H. Amini (Florida International University, USA), M. Kropidłowski, P. Śniatała (Poznan Univ. of Techn., Poland) *A Database Proposal for an Application Involving Industrial Networks for Industry 4.0 Concepts* A. Lugli, E. Neto, J.P. Henriques, M.T. de Carvalho Silva, N. Dias Pereira (Inatel, Brazil), T.C. Pimenta (UNIFEI, Brazil) *Virtualization of an Aluminum Cans Production Line Using Virtual Reality* L. Sales de Oliveira Almeida, A. Baratella Lugli (Inatel, Brazil), T. Cleber Pimenta (UNIFEI, Brazil), M.V. Cirino e Silva, J.P. Carvalho Henriques, R. Paranaiba Mesquita (Inatel, Brazil)

Time	Room B
10:00	**Session 2**: Thermal Issues in Microelectronics Chairman: Prof. M. Zubert *Comparison of Set-ups Dedicated to Measure Thermal Parameters of Power LEDs* K. Górecki, P. Ptak (Gdynia Maritime Univ., Poland), M. Janicki (Lodz Univ. of Techn., Poland) *Investigations Properties of Selected Methods of Measurements of Thermal Parameters of the IGBT* K. Górecki, P. Górecki (Gdynia Maritime Univ., Poland) *Thermal Characterization of Electronic Components Using Single-detector IR Measurement and 3D Heat Transfer Modelling* M. Kopeć, B. Więcek (Lodz Univ. of Techn., Poland)
11:30	***Break***
12:00	**Session 5 & 6**: Testing and Reliability & Power Electronics Chairman: Prof. M. Zubert *A Human Immunity Inspired Intrusion Detection System to Search for Infections in an Operating System* P. Widulinski, K. Wawryn (Koszalin Univ. of Techn., Poland) *The Application of NIR Spectrometer for Average Temperature Measurement in Optical Fibers Based on Spontaneous Raman Scattering for DTS Applications* I.S.M. Shatarah, B. Więcek (Lodz Univ. of Techn., Poland) *1MHz Gate Driver in Power Technology for Fast Switching Applications* R. Di Lorenzo, A. Baschirotto (Univ. Milan - Bicocca, Italy), A. Pidutti, P. Del Croce (Infineon, Austria) *An Influence of the Operation Mode of a LED Lamp of the HUE Type on Its Electrical and Optical Parameters* P. Ptak, K. Górecki, J. Heleniak (Gdynia Maritime Univ., Poland)

Time	Room C
10:00	**IEEE ED Poland MQ (Part 1)** *Ultralow Power, High-Resolution Sensor Interfaces* A. Nathan (Cambridge Touch Technologies, UK) *Sensor Design – From Prototype to Series* M. Schwarz (Robert Bosch GmbH, Germany)
11:30	***Break***
12:00	**IEEE ED Poland MQ (Part 2)** *Compact Modeling and Parameter Extraction for Oxide and Organic Thin Film Transistors (TFTs) from 150K to 350K* B. Iñíguez (Univ. Rovira i Virgili, Spain) *Nanometrology Using MEMS/NEMS Devices* T. Gotszalk (Wroclaw Univ. of Techn., Poland) *Phase Change Electro-optical Devices for Space Applications* M. Rais-Zadeh (California Institute of Techn., USA)

General Invited Papers

Maximizing the Efficiency of CMOS Front-Illuminated Solar Cell for Self-powered IoT Sensor Applications

Poki Chen
Department of Electronic and Computer Engineering
National Taiwan University of Science and Technology
Taipei, Taiwan
Email: poki@mail.ntust.edu.tw

SUMMARY

Internet of Things (IoT) enables widespread sensing through the deployment of devices called IoT nodes. IoT nodes should be able to sense, process data, and transmit these data wirelessly [1]. Around 50 Billion IoT nodes are expected to be connected by 2020 [2]. These sensor nodes can be powered by an external power supply or by a battery. However, these are not the viable solutions specially for IoT nodes deployed in places where the accessibility is quite limited. The most practical solution in powering up the IoT node is by harvesting the energy from the ambient sources [2]. Among all of the energy harvesting techniques, ambient light source has the best in terms of power density. Also, no special process is required when manufacturing the solar cells with the CMOS circuit on a single chip.

Most of CMOS circuits requires higher voltage than what a single solar cell can produce. A series connection of on-chip solar cells can be used to further increase its voltage. However, due to the series connection of non-identical solar cells, the output current will be limited by the solar cell that has a lower photogenerated current. This will effectively reduce the overall efficiency. For systems that does not require a small device volume, a single cell alongside with a power management unit is a better choice. In order to increase the system's efficiency, the on-chip solar cell's efficiency should be maximized.

Published materials had shown an efficiency improvement for on-chip solar cells by utilizing backside-illuminated solar cells [3]. It reported a maximum efficiency of 33.37% under 980-nm illumination. However, additional processes, such as post substrate thinning and surface antireflection, are required to achieve such efficiency. Moreover, it requires integrated passive devices (IPD) or heterogeneous integration to supply power to the succeeding CMOS chips. The overall cost is simply too high for most of the IoT devices under mass production. The only feasible solution is to integrate a front-illuminated solar cell with all other CMOS circuit to realize a so-called self-powered system.

Conventionally, a front-illuminated on-chip solar cell's layout is only composed of one large N type layer in a P-substrate. However, due to the nature of semiconductors, the concentration of liberated carriers decreases exponentially with depth, making the bottom plate junction less effective in generating current. Instead of heavily relying on the bottom plate junction, side wall junctions are used to improve the solar cell's efficiency. With the sidewall junctions, a part of the depletion region is exposed at the surface, in which the highest concentration of liberated carriers is located. Different structures with high side wall junction density for both triple well and single well is proposed. After measurements, conversion efficiencies were recorded as high as 28.57% and 29.54% for a single cell structure and triple well structure, respectively. Moreover, an N-Well in P-Substrate structure produced an efficiency as high as 31.27%. These prove the effectiveness of the presented structures and layout.

REFERENCES

[1] M. Alioto and M. Shahghasemi, "The Internet of Things on Its Edge: Trends Toward Its Tipping Point," in IEEE Consumer Electronics Magazine, vol. 7, no. 1, pp. 77-87, Jan. 2018, doi: 10.1109/MCE.2017.2755218.

[2] R. A. Kjellby et al., "Self-powered IoT Device based on Energy Harvesting for Remote Applications," 2018 IEEE International Conference on Advanced Networks and Telecommunications Systems (ANTS), Indore, India, 2018, pp. 1-4, doi: 10.1109/ANTS.2018.8710171.

[3] Y. Hung, H. Su, C. Chun, J. Chen, C. Huang and M. Cai, "Enhanced Efficiency in Backside-Illuminated Deep-n-Well-Assisted CMOS Photovoltaic Devices," in IEEE Electron Device Letters, vol. 36, no. 11, pp. 1169-1171, Nov. 2015, doi: 10.1109/LED.2015.2476380.

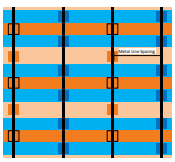


Fig. 1. Layout pattern for single well structure

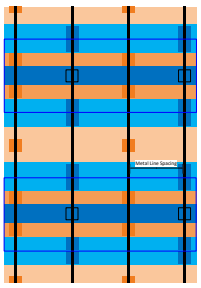


Fig. 2. Layout pattern for triple well structure

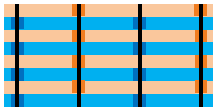


Fig. 3. Layout pattern of N-Well/P-Sub Structure

Sensor Design Made by Bosch

Invited Paper

Mike Schwarz
Robert Bosch GmbH
Email: mike.schwarz@de.bosch.com

***Abstract*—In this paper the sensor design made by Bosch, one of the world's largest supplier of micromechanical sensors in automotive and consumer applications, is briefly introduced. The design is one of the key elements to bridge the different domains between process technology, electronics, system and customers needs. The here presented flow and methodology ensures an integration of all perspectives from prototyping to series production. Examples of typical Sensor/MEMS design including various mechanical and electronical constraints are given.**

***Keywords*—MEMS, micromechnical sensors, design methodology, automotive applications, consumer applications**

INTRODUCTION

The design is one of the key parts within the development process of new sensors. It bridges the physics, e.g. the physical process, process development, electronic circuit(s), ASIC interface and the customer (market) requirements. The need of design, simulation and modeling methodologies is therefore an essential part in the product development cycle. They enable to concentrate on the Key Performance Index (KPI) of sensor and beyond future performance improvements. Furthermore, knowing the design and interaction between the various system components allows for a significant sample phase reduction and the "1st time right" approach. This ensures finally criteria as high functionality, yield and reliability of micromechanical devices in mass production.

To emphasize the reader for the demand of sensor design and parts of its methodologies one notice the penetration of sensors and sensor systems. Sensors are almost everywhere, dominating humans life every minute within electronics and/or sensor interfaces, e.g. for automotive and consumer applications. To give some rough numbers, a car typically contains more than 50 sensors made of Micro Electro Mechanical Systems (MEMS) and a mobile phone between 20-25 sensors [1]. In a few years the global amount of MEMS sensors will reach more than 80 billion [2].

The paper is organized as follows: Section II gives an overview in the design flow and methodologies as influence strength analysis, models, process- and device simulations, multi-domain and mechanical structure simulations, artificial intelligence and big data. Within section III some specific sensor design examples are highlighted using the presented approaches.

The sensor design methodology and flow ensures an integration of all perspectives from prototyping to series production. It is one of the key processes to bridge technology, mechanics, electronics and system and considers various aspects required during the development process.

The methodology is not limited to specific parts of the sensor design. Quite the reverse! The interfaces between the different parts allow for an abstract description which enables the transfer to various domains. It does not matter, if the point of view relies on process, sensor and/or system development or all of them in once.

The here presented sensor design examples incorperating the dicussed and suggested methods, enable and show the potential of the flow advantages. They emphasize the different abstraction level taken into account. Besides, they minimize the development cycles and allow for considering multi dimensional engineering questions.

Besides, the shown examples offer insights into the different aspects and questions during prototyping and/or series production. Depending on the sample phase various methodologies were applied with different abstraction level of the question. This allows for answering the required information in an efficient manner, without taking to much effort in complex simulations and/or models during an early development.

ACKNOWLEDGMENT

The author thank all colleagues at Robert Bosch Automotive Electronics, Engineering Sensor Technology, for their valuable contributions to this work. Special thanks to my colleagues Peter Engelhart, Pascal Gieschke, Stefan Krause, Christian Banzhaf, Bassem Baffoun, Arne Dannenberg, Isolde Simon, Frank Rettig, Friedjof Heuck, Wolfgang Feiler, Alexander Mann, Bastian Schmitt, Matthias Boehringer, and Jochen Franz.

Gefördert durch:

Bundesministerium für Wirtschaft und Energie

IPCEI on Microelectronics

aufgrund eines Beschlusses des Deutschen Bundestages

FUNDING PROVIDED BY THE FEDERAL MINISTRY FOR ECONOMIC AFFAIRS AND ENERGY

REFERENCES

[1] E. Mounier and D. Damianos, *"Status of the MEMS Industry 2019 - Market and Technology Report 2019"*, http://www.yole.fr, Yole Développement, Lyon, France, 2019.

[2] E. Mounier, *"The MEMS market is showing a 17.5% CAGR between 2018 and 2023, strongly supported by current mega trends"*, in Press Releases http://www.yole.fr, Yole Développement, Lyon, France, 2018.

The Qucs/QucsStudio and Qucs-S Graphical User Interface: An Evolving "White-Board" for Compact Device Modeling and Circuit Simulation in the Current Era

Invited Paper

Mike Brinson
Centre for Communications Technology
London Metropolitan University
UK
Email: mbrin72043@yahoo.co.uk

Extended Abstract

It is over fifty years since the industrial standard SPICE 2g6 [1] and 3f5 simulators [2] were first released as tools for integrated circuit design. Originally, these were developed as applications for main frame computers. Today the high performance Personal Computer (PC) has become the work horse for compact modeling and circuit simulation, which in turn has encouraged the development of a range of new commercial and Free Open Source Software (FOSS) circuit simulators similar to, or derived from, the Berkeley SPICE FORTRAN (SPICE 2g6) or C (SPICE 3f5) code. The move from centralized main frame computers to individual PC work station has had a profound effect on the analysis/design capabilities and simulation output data processing tools available to the compact modeling and circuit simulation communities. This paper outlines the evolution, over a period of roughly fifteen years, of the "Quite universal circuit simulator" (Qucs) modeling and simulation facilities [3], placing particular emphasis on the evolution from "SPICE text-in netlist input and simulation text-out output data" to highly interactive PC "White-Board" controlled compact device modeling, circuit schematic drawing, circuit simulation and output data visualization.

Illustrated in Fig. 1 is a block diagram that shows pictorially the links between Qucs and the "forked" QucsStudio [4] and Qucs-S [5] circuit simulators. In this figure the vertical arrows signify modeling and simulation information flow, culminating in entries displayed on a PC Graphical User Interface (GUI) "White-Board" window. Other GUI background information also indicates additional features, like for example where SPICE netlists apply. Throughout this paper a series of compact device modeling, circuit design/simulation and data visualization examples based on a tunnel diode compact model are presented. These have been chosen to demonstrate the QucsStudio and Qucs-S PC "White-Board" features that exemplify, without complex detail, the application of this innovative approach to compact modeling and circuit simulation.

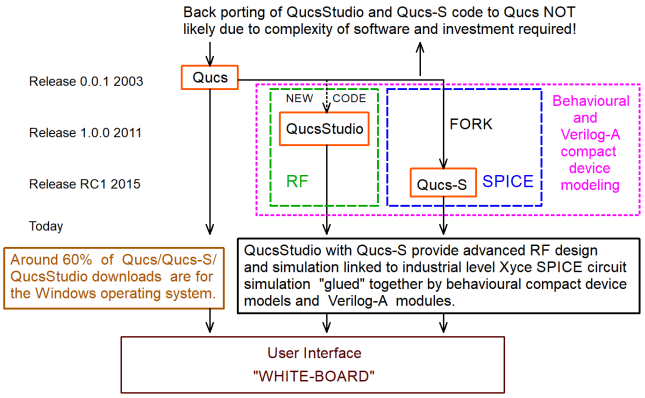


Fig. 1. A block diagram illustrating links between Qucs, QucsStudio, Qucs-S and a common GUI "White-Board".

References

[1] A.R. Newton, D. O. Pederson and A Sangiovanni-Vincentelli, "SPICE Version 2g User's Guide", Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA, 1981.

[2] B. Johnson, T. Quarles, A.R. Newton, D. O. Pederson and A Sangiovanni-Vincentelli, "SPICE3 Version 3f User's Manual", Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA, 1992.

[3] M. Margraf et al. Qucs (Quite Universal Circuit Simulator). Version 0.0.19, 2020. Available from http://qucs.sourceforge.net/index.html. [Accessed May 2020].

[4] M. Margraf, "QucsStudio Version 2.5.7. Available from http://dd6um.darc.de/ QucsStudio/qucsstudio.html, 2018, [Accessed May 2020].

[5] V. Kusnetsov and M. Brinson, "Qucs-S: Qucs with SPICE". Version 0.0.22. Available from https://ra3xdh.github.io/, 2020. [Accessed January 2020].

Compact Modeling Support for Micro and Nanoelectronic System Development

Compact Model for Continuous Microfluidic Mixer

Alexi Bonament[1], Alexis Prel[1], Jean-Michel Sallese[2], Morgan Madec[1], Christophe Lallement[1]
[1]Laboratory of Engineer Sciences, Computer Science and Imagine (ICube),
UMR 7357 (Université de Strasbourg / Centre National de Recherche Scientifique), Strasbourg, France
[2]STI-IEL-Electronics Laboratory,
Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland

Extended Abstract

Over the past decade, lab-on-chips have established themselves as a reference technology for high-quality high-throughput analysis in several fields like environment and healthcare. These lab-on-chips are mainly composed of a microfluidic system to drive fluids, bio-chemical reactions, electronic transducers and driving and processing electronic circuits. The design of such a system is a tricky challenge, especially if we aim at merging all of this domain early in the design process. Up to now, lab-on-chip designers lack a computer-aided design tool encompassing microfluidic, biochemistry and electronics. Designers might use multi-physical simulators to study a small part of the system but such an approach cannot be used at the scale of the complete device due to computation power limitation. For that purpose, we investigated techniques that enable the simulation of microfluidic channels within an electronic circuit simulation environment. Previous work has already shown analogies that can be exploited to simulate microfluidic channels as electronic equivalent circuits. The main assumption of this study is that designed channels are long enough to have homogeneous fluids at their output. This not always the case for small lab-on-chips and not always what we want to have. In this paper, a new modeling approach based on an analytic compact model is described. The technique consists of a translating of partial differential equations into time-dependent ordinary differential equations by using Fourier's series and a time-displacement conversion. Our compact model takes as inputs the flow rates and the concentrations of each fluid that are mixed and returns the flow rate and the concentration profiles at the output of the channel. It depends also on some physical parameters (e.g. diffusion coefficient) and mixing channel geometry. To validate our model, we compare simulation results with reference results obtained by solving the initial partial differential equation with COMSOL. Comparisons made on several use cases show that the model gives a good estimation of the concentration profile, with an error of less than 2% compared to the finite element simulator.

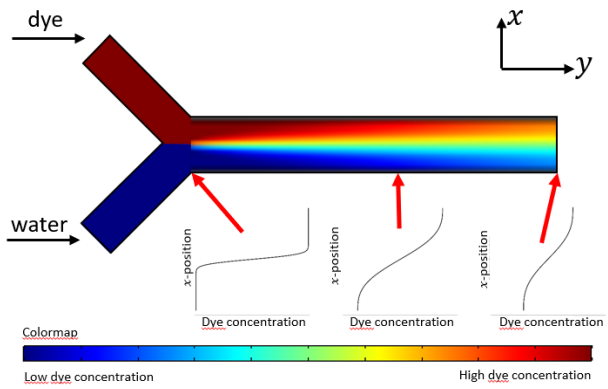


Figure 1. Schematic of a typical concentration distribution within a microchannel without a specific mixing element. The graphs below show the concentration distribution as a function of the coordinate normal to the channel wall, y, at several channel sections.

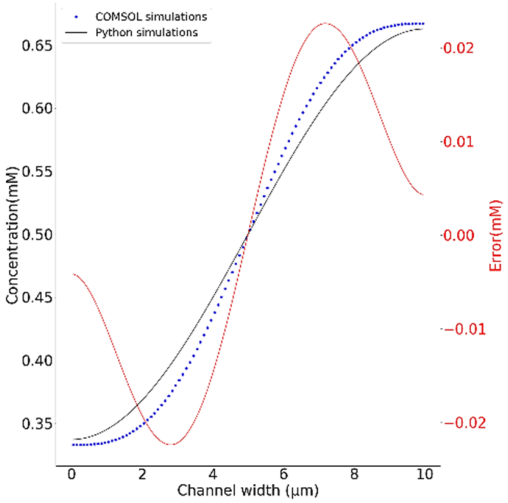


Figure 2. Transversal slice at the end of the channel. Differences obtain with our python simulation vs COMSOL simulation

Impact of Dynamic Trapping on High Frequency Organic Field-Effect Transistors

Markus Mueller[1], Shabnam Donnhäuser[1], Sven Mothes[1], Anibal Pacheco-Sanchez[1],
Katherina Haase[2], Stefan C. B Mannsfeld[2], Martin Claus[2]
[1]Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, Germany
[2]Center for Advancing Electronics Dresden, Technische Universität Dresden, Germany
Email: markus.mueller3@tu-dresden.de, Shabnam.Donnhaeuser@tu-dresden.de

Extended Abstract

Although organic semiconductor technology has made huge progress in the last years, the high frequency (HF) performance of OFETs is still not sufficient for applications such as Radio-frequency identification (RFID) tags [1].

The limitation of the device performance can be attributed to, among other things, the existence of trap states in the semiconductor. In this paper, high-frequency non-quasi-static effects related to dynamic trapping based on a theoretical framework, TCAD simulations and experimental data have been studied.

The dynamics of the trapped carrier is calculated based on the trapped carrier continuity equation [2],

$$\frac{\partial p_\mathrm{t}}{\partial t} = \tau_\mathrm{c} p n_\mathrm{t} - \tau_\mathrm{e} p_\mathrm{t}. \qquad (1)$$

Here, τ_c is the capture rate of holes and τ_e is the emission rate of trapped holes. Obviously, trap charging and discharging only happens for low enough frequencies.

Carriers in trap states do not contribute to the drain current, however their charging and discharging decreases the current gain H_{21} due to their impact on the device electrostatics. Furthermore, the gate capacitance is increased. Based on TCAD simulations it is shown that, as soon as the frequency of the AC signal is so fast that traps can not "follow" the signal anymore, the current gain increases and the gate capacitance decreases, see Fig. 1. This causes an increase of the transit frequency. Hence, the high frequency performance as predicted by conventional low frequency/DC methods is lower than what can actually be expected from a trap affected device. This claim is substantiated by low-frequency measurements of trap affected OFETs, as shown in Fig. 2.

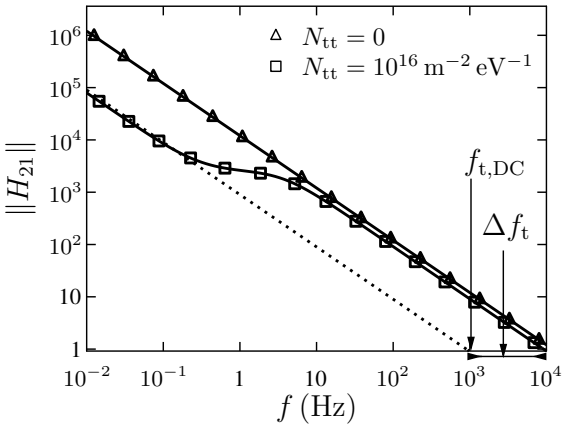


Fig. 1. Current gain H_{21} for a trap affected and a trap free OFET at $V_\mathrm{GS} = -1.5\,\mathrm{V}$ and $V_\mathrm{DS} = -1\,\mathrm{V}$.

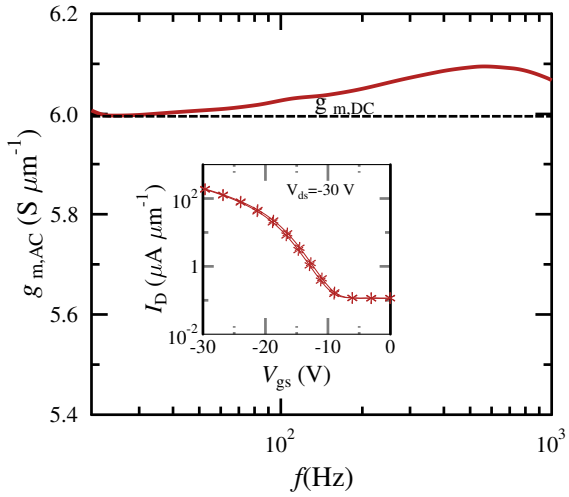


Fig. 2. Frequency dependent transconductance $g_{\mathrm{m,AC}}$ of a fabricated OFET Device with high gain at $V_\mathrm{DS} = -50\,\mathrm{V}$ and $V_\mathrm{GS} = -50\,\mathrm{V}$. The inset figures show transfer characteristics of device with forward-backward sweep.

References

[1] R. Rotzoll, S. Mohapatra, V. Olariu, R. Wenz, M. Grigas, K. Dimmler, O. Shchekin, and A. Dodabalapur, "Radio frequency rectifiers based on organic thin-film transistors," *Applied Physics Letters*, vol. 88, no. 12, p. 123502, mar 2006.

[2] C.-T. Sah, "The equivalent circuit model in solid-state electronics—part i: The single energy level defect centers," *Proceedings of the IEEE*, vol. 55, no. 5, pp. 654–671, 1967.

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Parameter Extraction for a Simplified EKV-model in a 28nm FDSOI Technology

Konstantin Bajer, Steffen Paul, Dagmar Peters-Drolshagen
Institute of Electrodynamics and Microelectronics (ITEM.me)
University of Bremen, Bremen, Germany, +49(0)421/218-62539
Email: {bajer, peters, steffen.paul}@me.uni-bremen.de

***Abstract*—The g_m/I_D methodology is applicable for the circuit design in advanced nanometer technologies. This work proposes a systematic parameter extraction process for a simplified EKV-model with only three model parameters which is applicable to all CMOS technologies. The extraction procedure relies only on the drain current for a sweep of the gate voltage without the need of additional extraction simulations in SPICE or parameters from the model card. Therefore, it is independent from the applied technology or the compact model of the SPICE simulation. For devices with short channel lengths, three variations of the EKV model were evaluated which consider velocity saturation. The resulting model provides good results compared to the SPICE simulation over the complete operation region of the technology for long and short channel devices while keeping simplicity for fast tool-based circuit design procedures and hand calculations.**

***Keywords*—Transistor Modeling. Parameter Extraction, Design Process, EKV, MOSFET, FDSOI, Nanometer Technology.**

I. Introduction

The g_m/I_D design methodology can be applied in deep submicron or nanoscale bulk, single- and double-gate FDSOI and FinFET CMOS technologies. In this work, a simplified EKV model is used which is suitable for hand calculations. This model uses only the subthreshold slope n, the technology specific current I_{spec} and λ_c to model velocity saturation. The approach in this work uses only this database to extract the model parameter without the need for an additional SPICE simulation or parameters from the SPICE model card and is based on the slope of the g_m/I_D curve. This makes it possible to adapt this method to other technologies and to already existing databases.

II. Parameter Extraction

Simplified expressions are presented for the Enz-Krummenacher-Vittoz (EKV) model which cover weak inversion (WI), strong inversion (SI) and/or velocity saturation (VSAT). The extraction procedure is based on g_m/I_D curves from SPICE simulations, where V_{DS} is swept for each curve, as shown in Fig. 1.

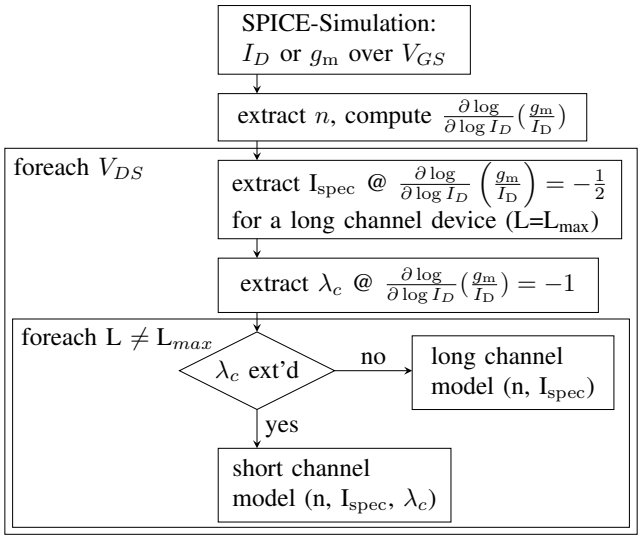


Fig. 1. Parameter extraction procedure from the SPICE database.

III. Conclusion

This paper proposes a systematic parameter extraction for a simplified EKV-model with only three model parameters and applies it to a 28nm FDSOI technology as an example. Compared to other approaches, this work evaluates the slope of the g_m/I_D curve. The algorithm determines the extraction points automatically from the database and whether the velocity saturation has to be considered or the long channel model with only two model parameters is sufficient. In case of the 28nm FDSOI technology for moderate and high V_{DS} and large L, the technology current I_{sp} and the subthreshold slope n are sufficient for the model. For the velocity saturation λ_c three different model approaches were compared in order to improve the model accuracy. The FDSOI can be modelled with the WI+VSAT model with a mean absolute relative error slightly above 0.2 down to 0.05, depending on the transistor dimension and the drain-to-source voltage. In addition to that, two other models are presented, which are capable to model the same operation and design space with less performance. Nevertheless, this extraction procedure can easily be applied to other CMOS technologies i.e. bulk, FinFET and is independent from the used SPICE simulation model. Furthermore, it can be easily automated and applied to already existing databases from tool based g_m/I_D design procedures without the need of additional SPICE simulation for measurements. While this resulting model is very simple and can be used for hand calculations, it is fairly accurate over the complete design space of the technology for a first design approach even for nanometre scale feature sizes of the MOSFET and low voltage designs.

Qucs-S/QucsStudio/Octave Schematic Synthesis Tools for Device and Circuit Parameter Extraction from Measured Characteristics

Mike Brinson
Centre for Communications Technology
London Metropolitan University
UK
Email: mbrin72043@yahoo.co.uk

Extended Abstract

The extraction of device parameters and circuit component values from d.c., a.c., and transient measurements are significant steps in establishing the validity of device and circuit simulation models. One of the most important practical techniques used for this purpose relies on the comparison of measured and simulated output data where each dependent data set has a common independent axis selected from signal frequency (in the a.c., S, Z and Y domains) or time (in the transient domain) or swept parameter values (in all domains). The extraction process proceeds by overlaying simulation output data on top of measured data, varying user selected device parameters, or component values, then re-simulating the device/circuit under test until the two data sets line-up within a specified error limit. The Qucs-S/QucsStudio Free Open Source Software (FOSS) circuit simulators [1][2] allow individual or groups of parameters to be varied by "manual slider tuning" (QucsStudio) or by computer controlled optimization employing objective target functions (Qucs-S and QucsStudio). This paper introduces a groundbreaking parameter extraction technique which links measured and simulated output data via Qucs-S/QucsStudio test bench schematics. To ensure that the independent X axis of the measured and simulated data have the same range and number of data points simulation is controlled by icons synthesized from the measured X scale data. The primary task of these icons is to set up and instantiate simulation while simultaneously ensuring that the independent axis of the measured and simulation output data are aligned automatically during parameter extraction. An overview of this process is shown diagrammatically in Fig.1. To illustrate the procedure data from a study of the admittance of a forward biased semiconductor pn junction diode is introduced, it's model parameters extracted, analyzed and commented on. In this example the pn junction is represented by a non-linear Verilog-A module that models diode inductance generated by conductivity modulation and frequency dependent minority carrier lifetime at high forward d.c. bias currents [3][4][5].

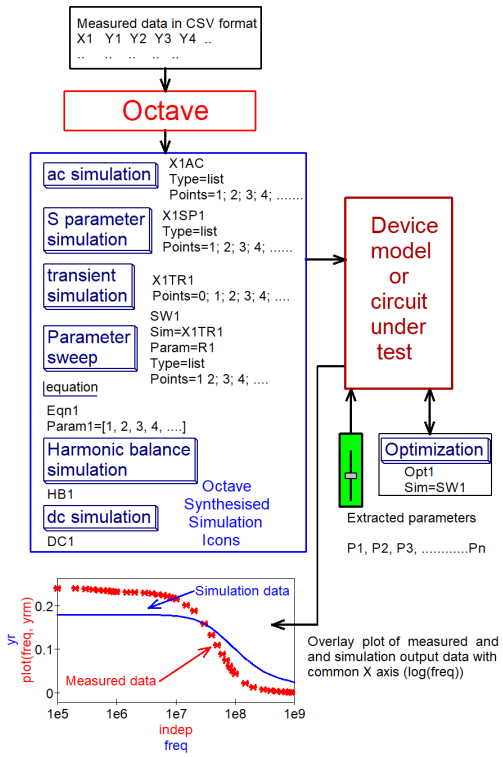


Fig. 1. A block diagram illustrating the fundamental stages for reading measured data, building extended independent and dependent variable lists and synthesizing sets of simulation control icons.

References

[1] V. Kusnetsov and M. Brinson, "Qucs-S: Qucs with SPICE". Version 0.0.22, https://ra3xdh.github.io/, 2020. [Accessed January 2020].
[2] M. Margraf, "QucsStudio Version 2.5.7, http://dd6um.darc.de/ QucsStudio/qucsstudio.html, 2018, [Accessed January 2020].
[3] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors", 1949, Bell System Technical Journal, pp. 435-489.
[4] A.A Barna and D. Horelick, "A Simple Diode Model Including Conductivity Modulation", IEEE Transactions on Circuit Theory, Vol. CT-18, No. 2, 1971, pp. 233-240.
[5] L. Ladany, " An analysis of inertial inductance in a junction diode", IRE Trans. Electron Devices, Vol. ED-7, 1960, pp. 303-310.

Design of Integrated Circuits and Microsystems

A Capacitive Feedback 80 dBΩ 1.1 GHz CMOS Transimpedance Amplifier with Improved Biasing

Agata Romanova[1], Vaidotas Barzdenas[1,2]
[1]Department of Computer Science and Communications Technologies
Vilnius Gediminas Technical University, Vilnius, Lithuania
[2]Micro and Nanoelectronic Systems Design and Research Laboratory
Vilnius Gediminas Technical University, Vilnius, Lithuania
{agata.romanova,vaidotas.barzdenas}@vgtu.lt

Extended Abstract

Constantly growing data rates in communication systems had led to a wide adoption of optical fibers as the core technology for data transmission. This has also triggered an increase in demand for the related maintenance instruments such as Optical Time-Domain Reflectometers (OTDR). Here the front-end Transimpedance Amplifier (TIA) is the most critical part as its performance often limits the overall sensitivity and the noise level of the OTDR instrument. At the same time, strict OTDR noise requirements make it difficult to employ classical shunt-feedback and feed-forward TIA topologies and novel solutions are sought.

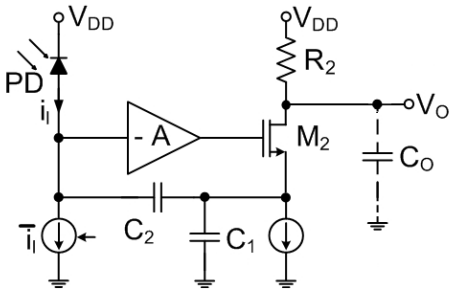


Fig. 1. Capacitive feedback TIA.

The work presents the design of an area-efficient low-noise high-performance CMOS TIA for OTDR using a capacitive feedback approach as shown in Fig. 1 [1]. Here the voltage across C_1 is sensed by C_2 and is returned as a proportional current to the input with the gain for low frequencies [2]:

$$R_T = \left(1 + \frac{C_1}{C_2}\right) R_2. \quad (1)$$

Although the expression above provides an important insight into the underlying principles of the proposed topology, it can hardly serve as the basis for the real circuit design as it significantly overestimates of the gain/bandwidth when compared to realistic circuit implementation under relevant CMOS technological constraints.

In this work we propose a more accurate design methodology based on explicit modeling of the biasing circuits and decoupling capacitor and modifications to the reference design are suggested including circuits for PMOS-based biasing and DC current elimination. The circuit was designed and optimized for standard TSMC 0.18 µm process with the total chip area 130 µm × 70 µm (without connection pads). The simulation results for R_T are shown in Fig. 2. The proposed low-noise solution employs a single-stage CS as a core amplifier and shows a gain of 83/80 dBΩ with the bandwidth reaching 1.1 GHz and average input-referred noise current density below 1.8 pA/$\sqrt{\text{Hz}}$ in the presence of a 0.7 pF total input capacitance. The total power consumption is around 21 mW while running at 1.8 V power supply.

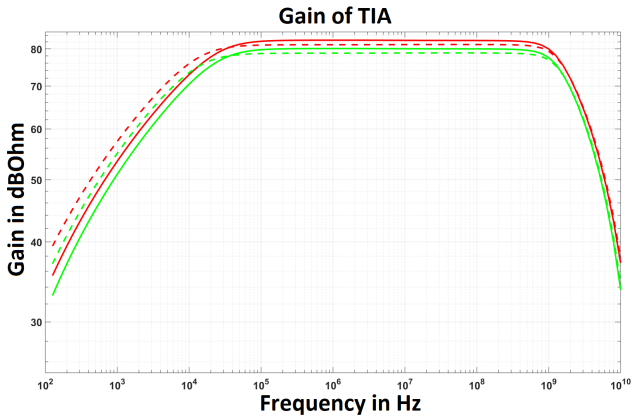


Fig. 2. Simulation results for the transimpedance gain before (red line) and after the output buffer (green line): dashed line - original design with resistive biasing, solid line - optimized bias circuit.

The suggested TIA design demonstrates no ripple in the pass-band and is a viable candidate for low-cost OTDR instruments, where its significant performance margin makes the approach also suitable for other low-noise applications.

References

[1] B. Razavi, "A 622 Mb/s 4.5 pA/$\sqrt{(Hz)}$ CMOS transimpedance amplifier [for optical receiver front-end]," in *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)*, Feb 2000, pp. 162–163.

[2] S. Shahdoost, A. Medi, and N. Saniei, "Design of low-noise transimpedance amplifiers with capacitive feedback," *Analog Integrated Circuits and Signal Processing*, vol. 86, no. 2, pp. 233–240, 2016.

A New Architecture of Thermometer to Binary Decoder in a Low-Power 6-bit 1.5GS/s Flash ADC

Mohammad Keyhanazar, Arash Kalami
Department of Electrical Engineering
Urmia Branch, Islamic Azad University
Urmia, Iran
m.keyhanazar@gmail.com, a.kalami@iaurmia.ac.ir

Abdollah Amini
Sina Bioelectronics Company (SBC)
Roshd Center, Urmia Branch, Islamic Azad University
Urmia, Iran
amini7908@gmail.com

ABSTRACT

This paper introduces a new structure of thermometer to binary decoder utilizing combination of two conventional approach and modify them in a low-power 6-bit flash analog to digital converter (ADC). Considering advantages of each method to form the presented decoder can leads to minimum possible power consumption which is a critical parameter in all converters especially in flash ADCs. Moreover, in the high-resolution flash ADCs, the decoder structure will be simpler compared to conventional ones and decreases the amount of power dissipation as well. Simulation results through HSPICE software level 49 parameters in 0.18µm standard CMOS technology parameters, prove the precise operation and the great improvements. The 6-bit converter achieves sampling rate of 1.5 GS/s, and precision of 5.10 effective number of bits (ENOB). The proposed ADC works with 1.8V power supply and it has the power consumption of 4.57mW and the figure of merit (FOM) is 0.047 pJ/conversion-step. Hence, this architecture would be dedicated to communication transceivers and data acquisition systems where area and energy efficiency are paramount.

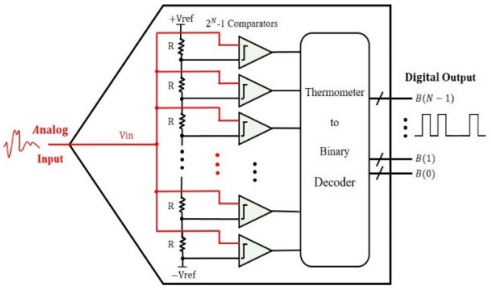


Fig. 1. Block diagram of Flash ADC

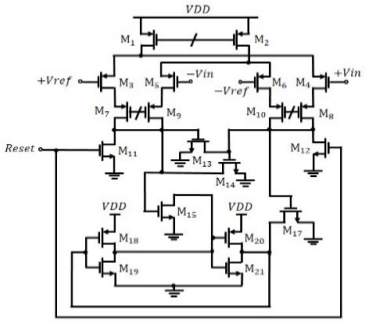


Fig. 2. The comparator circuit

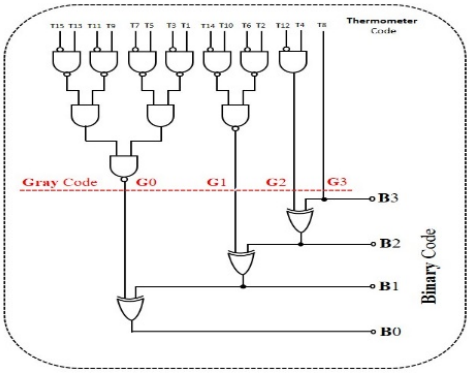


Fig. 3. Schematic of a simple 4-bit decoder

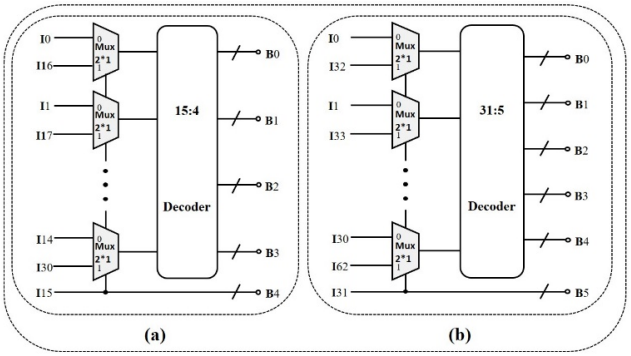


Fig. 4. a) Schematic of a simple 5-bit decoder, b) The proposed 6-bit decoder

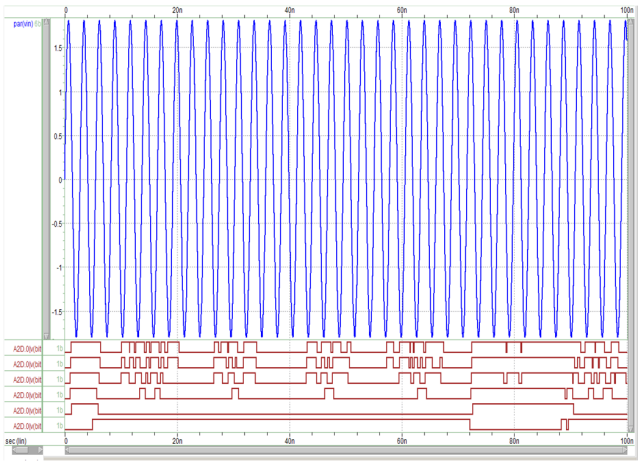


Fig. 5. Digital outputs of ADC for sinus output

A Survey on the Application of Parametric Amplification in Next Generation Digital RF Transceivers

Luís Miguel Pires[1,2], João P. Oliveira[1,2]
[1]Centre for Technologies and Systems (CTS) - UNINOVA
[2]Department of Electrical Engineering (DEE)
Universidade Nova de Lisboa (UNL)
Campus FCT/UNL, 2829-516, Caparica, Portugal
l.pires@campus.fct.unl.pt, jpao@fct.unl.pt

***Abstract*—The accelerating growth in mobile networks for data communication, covering a diversity of applications, has originated a high demand not only for low-power devices but also for low-cost System on Chip (SoC). An example of this is the next generation 5G, which is under intense development intending to reach an effective ubiquitous connectivity. CMOS technology offers the best trade-off between costs versus performance and facilitates the co-integration of digital-analog. However, integrating analog RF in recent technology nodes remains a challenge, which has pushed the research towards innovative techniques. One of these techniques is the parametric signal conversion, which can offer high speed and low-noise operation. This paper presents a survey on the application of this technique in modern heterodyne receivers.**

Keywords*—Parametric Amplification; Next Generation Digital RF Receivers; 5G; RF Front-End; Heterodyne RF Transceiver; Mixer-First; CMOS; Beamforming Receiver;** ***Introduction

I. Using Parametric Amplification in 5G RF Transceivers

The application requirements for higher data rage in mobile communications is driving the 5G development to support larger capacity. Considering the high occupancy of the radio spectrum up to 6 GHz, one of the most promising evolution is the utilization of the mmWave range, i.e., 28 GHz frequency that can offer larger bandwidth channel, when comparing with the current 4G standard.

For higher frequency range, namely for mmWave, a heterodyne topology can combine a mixer-first approach with a software defined radio architecture. The main issue, however, with a passive mixer-first receiver front-end is its fairly high noise figure. The challenge is then to minimize the noise figure of the following blocks, which will imply spending more current, decreasing the on-resistance of the mixer, while keeping the input impedance well matched with the input antenna.

This work was financially supported by FCT – Fundação para as Ciências e Tecnologia in the scope of the Investigation Unit CTS - Centro de Tecnologias e Sistemas, under the reference UIDB/00066/2020 within the project foRESTER PCIF/SSI/0102/2017.

An alternative, for the implementation of a heterodyne architecture for a 5G compatible transceiver, is the use of parametric amplification along the signal processing chain. This can be achieved in both time continuous time and discrete time, as shown in Fig. 1, which can be integrated in a single chip. In a first step, a 28 GHz RF frequency applied to a parametric based downconverter, in continuous time, can be translated to a first intermediate frequency. A second mixing step, to bring down to baseband or low-IF, can be implemented using a discrete-time parametric based downconverter.

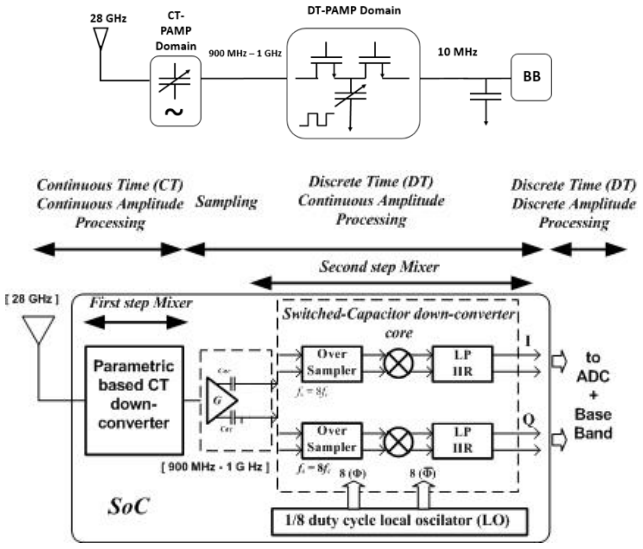


Fig. 1. Conceptual SoC for the RF front-end transceiver, using parametric amplification in both continuous and discrete time domains.

In this paper, an overview about reactance-based signal amplification and conversion, as well as their system integration targeting modern digital transceivers, is provided.

A W-band SiGe BiCMOS Transmitter Based on K-band Wideband VCO for Radar Applications

Maciej Kucharski, Michał Widlok, Radosław Piesiewicz
SIRC Sp. z o.o. ul. Starowiejska 41-43, 81-363 Gdynia, Poland
Emails: m.kucharski@si-research.eu, m.widlok@si-research.eu, r.piesiewicz@si-research.eu

Extended Abstract

This paper presents an 86-97 GHz transmitter (TX) using a wideband voltage-controlled oscillator (VCO) operating in 21.5-26 GHz range and frequency quadrupler (FQ) fabricated in SiGe BiCMOS technology (Fig. 1). The VCO implements a self-buffered common-collector Colpitts topology with binaryweighted varactor ladder for low VCO gain (K_{VCO}) and wide tuning range. Use of high-Q passive components and low-noise heterojunction bipolar transistors (HBT) results in worst-case phase noise of -92.8 dBc/Hz at 1MHz offset from the carrier. The VCO is loaded by a low-loss transformer that splitts the signal between frequency prescaling and multiplying blocks. The prescaler comprise three divide-by-two circuits (DTC) based on D flip-flops (D-FF) providing adequate feedback signal for an external phase-locked loop (PLL). The multiplying section consists of two cascaded Gilbert-cell frequency doublers driving a W-band power amplifier (PA).

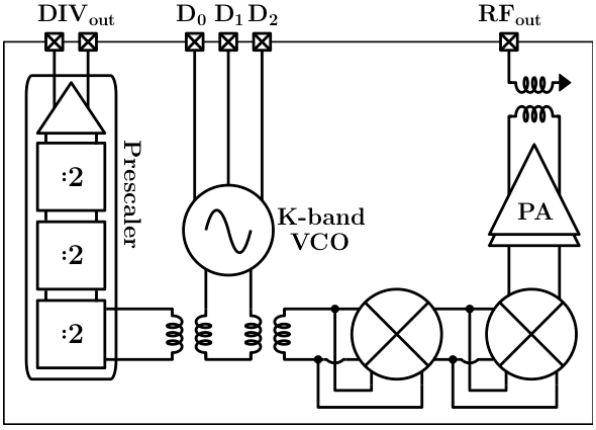


Fig. 1. Block diagram of W-band transmitter.

The TX was manufactured using SG13S process from IHP. It offers heterojunction bipolar transistors (HBT) with f_T / f_{MAX}=240/330 GHz for RF circuits and CMOS devices for efficient control and digital processing. In order to reliably measure TX output power and the phase noise a dedicated PCB containing ADF4158 PLL was designed to stabilize LO signal and eliminate drift effects. The chip board contains the TX IC as a bare die mounted on the PCB.

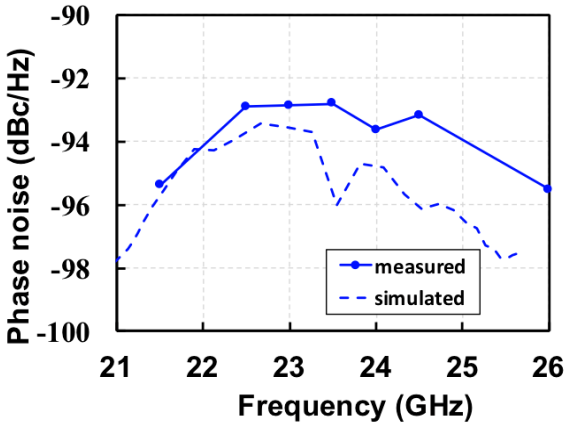


Fig. 2. VCO phase noise at 1MHz offset from the carrier.

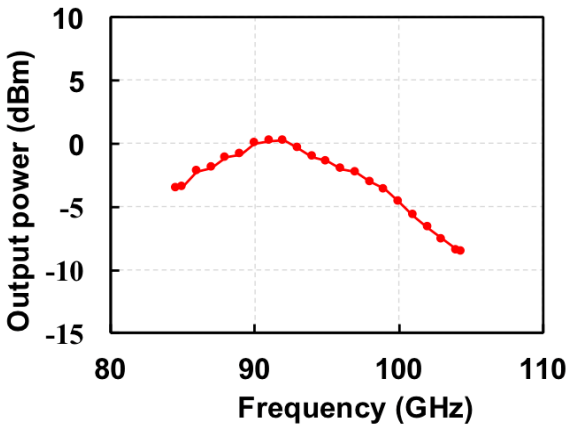


Fig. 3. Measured TX output power versus frequency.

Fig. 2 presents VCO phase noise (PN) at 1 MHz offset from the carrier. The measured PN varies from -95.5 to - 92.8 dBc/Hz reaching highest value in the middle of the VCO tuning range due to the largest VCO gain and resulting AMto-PM noise conversion. Fig. 3 presents measured output power of the complete TX circuit. It achieves 0.2 dBm output power at 92 GHz and more than -2.8 dBm in 86-97 GHz range consuming 60mA from 3.3V supply. The chip occupies 0.755mm^2 silicon area.

ASIC Architecture and Implementation of RED Scheduler for Mixed-Criticality Real-Time Systems

Lukáš Kohútka, Viera Stopjaková
Institute of Electronics and Photonics
Slovak University of Technology in Bratislava
Bratislava, Slovakia
lukas.kohutka@stuba.sk

***Abstract*—This paper presents a new ASIC design of a coprocessor that performs process scheduling for embedded mixed-criticality real-time systems consisting of processes of various criticality and various real-time attributes. The proposed solution is implementing Robust Earliest Deadline (RED) algorithm and previously developed hardware architectures used for scheduling of real-time processes. Thanks to the on-chip implementation of the scheduler in a form of a coprocessor, the scheduler operations can be completed in two clock cycles regardless of the process amount within the system contains. The proposed scheduler was verified by simulations that applied millions of random inputs. Chip area costs are evaluated by synthesis into an ASIC using 28 nm process by TSMC. Two versions of real-time process schedulers were compared: EDF scheduler designed for hard real-time processes only and the proposed RED scheduler. The RED algorithm handles variations of process execution times better, achieves higher CPU utilization and can be used for scheduling of hard real-time, soft real-time and non-real-time processes combined within one system that is not possible using the other scheduling algorithms.**

***Keywords*—scheduling, mixed-criticality, ASIC, RED.**

EXTENDED ABSTRACT

Mixed-criticality is an active research field, as reflected in the review by Burns and Davis. Mixed-criticality is resulting from the global trend in microelectronics that lies in increasing integration of growing number of components on chip belonging to safety-critical domain. Until not so long time, process isolation was required within safety-critical certification to imply performing of critical processes in a separated hardware. Due to the process isolation, RT systems were under-utilized and based on the pessimistic analysis of worst-case execution time for each process. As average execution time is generally significantly smaller than the worst-case time, CPU resources are usually reserved much more than it is really needed for execution of RT processes. Mixed-criticality RT systems can contain any combination of critical and/or non-critical processes in the same platform without complete isolation of the processes as it is considered to be too inefficient (e.g. using hypervisors). Non-isolation is recommended as a demanding and efficient way to improve CPU utilization, which is achieved by executing low-priority and non-critical processes within slack time that becomes available whenever high-priority and high-critical processes are finished sooner than it was predicted according to worst-case execution time. This is happening relatively frequently in real-world applications. The problem is that safety-critical processes and best-effort processes have usually conflicting requirements, being an important research challenge.

We proposed a new process scheduler that performs RED scheduling algorithm and is implemented on chip. The proposed scheduler is suitable for robust mixed-criticality RT systems due to the ability to distinguish between various types of processes, including their priority and deadlines. The proposed solution used an approach of reusing and extending of existing EDF schedulers. The Ready Queue as well as the Reject Queue is implemented using an existing sorting architecture called Shift Registers. Both queues perform an operation of process insertion or process removal in constant time regardless of number of processes used in the system. The RED algorithm extended the EDF algorithm with two features: rejection of process and reclaiming of process reclaiming. These features are combined with a possibility to use various types of processes and various criticality levels. The RED scheduler correctly and efficiently handles any combination of safety-critical hard RT processes, high-priority soft RT processes, medium-priority soft RT processes, low-priority soft RT processes and non-RT processes. This means that all safety-critical hard RT processes meet their deadlines, and as many as possible soft RT processes meet their deadlines, considering the priority within the soft RT processes as well. Therefore, the proposed RED scheduler is very suitable for mixed-criticality RT systems. The RED scheduler is providing 1024 priority levels for the non-RT processes and 4 criticality levels for the RT processes. The proposed solution is consuming higher, but still acceptable resource costs, which are scaling still linearly with growing maximum number of processes. If we compare the proposed solution to existing solutions implemented in software, the ASIC implementation is able to execute instructions in constant time and with dramatically higher throughput. Thanks to that, the system using the proposed RED scheduler would be much more efficient and deterministic, resulting in lower amount of processes missing their deadlines, especially if they are high-criticality processes. The ASIC-implemented scheduler causes CPUs to waste minimum possible time for scheduling and to focus only on execution of the processes.

ACKNOWLEDGEMENT

This work was supported in part by the Ministry of Education, Science, Research and Sport of the Slovak Republic under grant VEGA 1/0905/17, and ECSEL JU under project PROGRESSUS (876868).

Active Feedbacks Comparative Analysis for Charge Sensitive Amplifiers Designed in CMOS 40 nm

Grzegorz Wegrzyn, Rafal Kleczek, Piotr Kmon
Faculty of Electrical Engineering, Automatics, Computer Science and Electronics
AGH University of Science and Technology, Krakow, Poland
grzesweg@student.agh.edu.pl

***Abstract*—In this paper we present a comparative analysis of active feedback circuits dedicated to charge sensitive amplifiers (CSA) used in X-ray imaging systems. This work is motivated by the fact there are many papers discussing advantages and disadvantages of using particular CSA feedback but none of them are realized in the same process which is very crucial. The presented design, prototype recording channels fabrication employing two the most competing solutions, and their further measurement results may therefore help one in choosing the most suitable feedback for a particular application. The presented circuits are designed in CMOS 40 nm process and are compared in terms of noise contribution, power consumption, area occupation, ability to minimize detectors leakage current, and also CSA stability. Index Terms—X-ray imaging, active feedback circuit, CMOS, sensor, energy measurement, charge sensitive amplifier.**

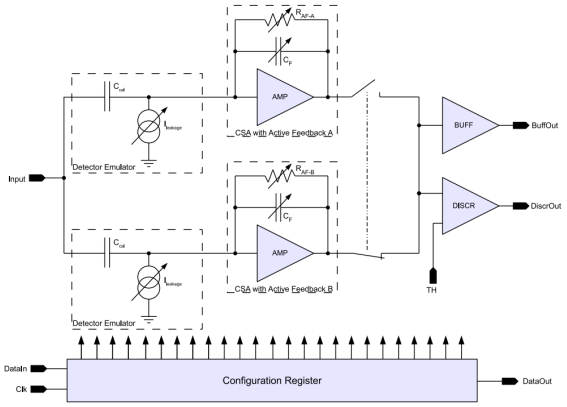
***Keywords*—X-ray imaging, active feedback circuit, CMOS, sensor, energy measurement, charge sensitive amplifier.**

I. Introduction

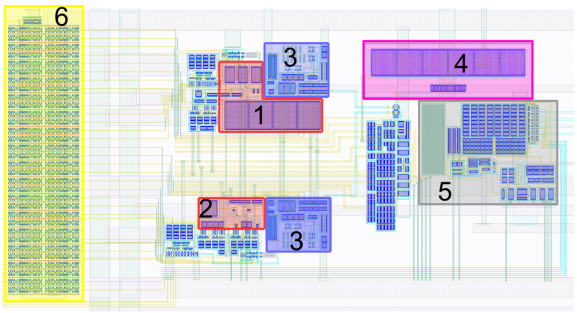
In this paper we present a comparative analysis of two active feedback circuits. The first is a commonly used solution named Krummenacher circuit [1] while the second feedback is an approach presented in [2] and being a very attractive counterpart. The feedback circuits are compared in terms of noise contribution, power consumption, area occupation, detectors leakage current compensation, and CSA stability. Two prototype recording channels were both designed in the CMOS 40 nm process and sent for fabrication. The paper is organized as follows. In the Section II we provide CSA feedbacks description while in the Section III a prototype recording channels design is shown. The Section IV provides post-layout simulation results of designed circuits and finally conclusions are provided.

TABLE I,
ACTIVE FEEDBACKS PARAMETERS SUMMARY

Parameter	Unit	AF-A		AF-B	
Pulse width	μs	0.2	1.5	0.2	1.5
Power consumption	nW	15	4	22	5
ENC_{AF}/ENC_{TOT}	–	0.61	0.60	0.52	0.5
ENC_{TOT}	e^-	101	100	78	72
Phase margin	deg	54	55	53	55
Occupied area	μm^2	160		50	



a)



1 – AF-A 3 – CSA 5 – Discriminator
2 – AF-B 4 – Output Buffer 6 – Configuration Register

b)

Fig. 1 Active feedbacks prototype recording channels schematic idea a) and designed circuit layout view b).

Acknowledgment

The presented work has been supported by the National Science Center, Poland under Contract No. UMO2016/23/D/ST7/00488.

References

[1] F. Krummenacher, "Pixel detectors with local intelligence: an ic designer point of view," Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 305, no. 3, pp. 527 – 532, 1991.

[2] P. Kmon, G. Deptuch, F. Fahim, P. Grybos, P. Maj, R. Szczygieł, and T. Zimmerman, "Active feedback with leakage current compensation for charge sensitive amplifier used in hybrid pixel detector," IEEE Trans. Nucl. Sci., p. 1, 2019.

CMOS Interface for Capacitive Sensors with Custom Fully-Differential Amplifiers

Mariusz Jankowski, Piotr Zając, Piotr Amrozik, Michał Szermer
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
jankowsk@dmcs.pl

Extended Abstract

In many applications it is crucial to design reliable and efficient analog readout circuits for micro-electromechanical (MEMS) capacitive sensors. In this paper, we describe the switched-capacitor, open-loop, capacitive-sensing readout circuit, which was designed and manufactured in 0.18 µm technology. Non-standard application of a fully differential amplifier structure is also presented. The post-layout simulation results are described to show the proper operation of the circuit. They show that with the proper symmetrical design of the differential signal path the output offset voltage can be kept at acceptable level.

Intelligent systems for detection and monitoring of balance disorders have recently gained a lot of interest [1]. The most popular solutions are based on multiple sensing devices that are put on patient's body and allow continuous tracking of the patient's movement [2]. The data from sensors is wirelessly transmitted to the central database and can be subsequently used for diagnosis by a human doctor or artificial intelligence.

Such a system is currently being developed within the frame of "InnoReh" (Innovative Rehabilitation) project [3]. One of the crucial parts of the sensing device is the capacitive MEMS accelerometer with analog sensing interface. Several parts of the system have already been described in literature [4][5]. In this paper, we concentrate on custom solutions used for the design of the analog readout circuit (ARC), which is a switched-capacitor, open-loop interface circuit. Its main goal is to convert the MEMS capacitance to a digital signal. The block diagram of the ARC is shown in Fig. 1 and essentials of the corresponding layout are presented in Fig. 2.

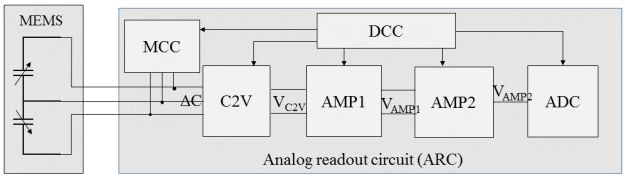


Fig. 1. Block diagram of the designed readout circuit

The readout circuit for capacitive sensors has been designed and manufactured. Although the analog blocks are based on designs found in literature, the important novelty presented in this paper is their combination and application of a low-voltage positive feedback op-amp topology as cross-current control. The post-layout simulations prove that the circuit operates correctly and emphasize the importance of symmetry in the design of the differential parts of the circuit to reduce the impact of parasitics. With a carefully realized symmetrical design we were able to reduce the output offset voltage to an acceptable value of 0.3 V.

Tests of the manufactured and already received MEMS and ASIC structures will prove correctness of presented design principles and solutions.

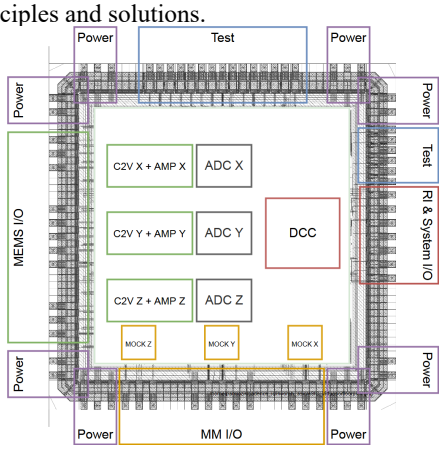


Fig. 5. Essentials of the designed chip layout manufactured in 0.18 µm technology process.

Acknowledgment

The presented research is supported by the project STRATEGMED 2/266299/19NCBR/2016 funded by The National Centre for Research and Development in Poland.

References

[1] D. Basta, M. Rossi-Izquierdo, A. Soto-Varela, et al. "Mobile posturography: posturographic analysis of daily-life mobility", Otol Neurotol, 34 (2013), pp. 288-297.

[2] L. Chiari., "Wearable systems with minimal set-up for monitoring and training of balance and mobility," 2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, Boston, MA, 2011, pp. 5828-5832.

[3] M. Jankowski, M. Szermer and P. Amrozik, „Concept of an Electronic Device Dedicated to Imbalance Disorders Monitoring," 15th International Conference The Experience of Designing and Application of CAD Systems in Microelectronics (CADSM), Lviv, 2019, pp. 1-4.

[4] M. Szermer, P. Amrozik, P. Zając, C. Maj and A. Napieralski, „Capacitive MEMS accelerometer with open-loop switched-capacitor readout circuit," International Journal of Microelectronics and Computer Science, 2017, vol. 8, no 4, p. 139-145

[5] P. Zając, M. Szermer, P. Amrozik, C. Maj, G. Jabłoński, „Coupled Electro-mechanical Simulation of Capacitive MEMS Accelerometer for Determining Optimal Parameters of Readout Circuit," 20th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EUROSIME), Hannover, 2019, pp. 399-403.

Comparative Analysis of Power Consumption of Parallel Prefix Adders

Ireneusz Brzozowski
AGH University of Science and Technology
Department of Electronics
Krakow, Poland
ireneusz.brzozowski@agh.edu.pl

***Abstract*—This paper presents results and conclusions derived from simulations of tens structures of Parallel Prefix Adders considering over a dozen activity scenarios of input vector changes. Based on extended power model of static CMOS gates accurate analysis is done, thanks to the fact, that the model take into consideration changes of input vectors, not only switching activity of signals. Various structures of PG tree have been examined: regular, non-regular, with grey cells only, with both grey and black and with higher valency cells. Obtained results shows that some structures are better for some kind of summed data, but general remarks for adders design can be derived.**

***Keywords*—power consumption, low-power design, parallel prefix adders,integrated circuits, CMOS technology**

I. Introduction

Power consumption is still important issue in design of integrated circuits. But achievement of reduction needs more effort, detailed analysis and specialist tools. It is not enough to take into consideration general conditions of a circuit work. Efficient reduction of power consumption needs to individual consideration of work conditions of designed circuit. Arithmetic circuits play very important role because they are essential part of microcontrollers and other data processing systems. In many cases, they work with specific and known data. So some properties of the data can be well defined. And there is a temptation to design circuits especially for specific kind of data. One of the fastest adders are Parallel Prefix Adders (PPA), are well described in many papers. Addition can be described as three-step operation: precomputation (G_i, P_i), **prefix calculation** (PG tree), and postcomputation (S_i). The second step is the main point of our interests in the context of power consumption. Additionally, extended power model used in this work, thanks to taking into account probability of input vector changes is independent of spatial and temporal correlation between inputs signals, gives more accurate results and allows to deepened analysis of adders power consumption.

II. Tests

Using building blocks specially prepared as much as possible PG-trees of adders were created, because realization of this part gives many possibilities. At the beginning only 4-, 5- and 6-bit circuits were considered. According to theory of PPA dashed diagrams represent structure of PG blocks (Fig. 1). Using specially prepared software in Matlab environment 100 PG trees with 28 distributions of input vectors changes were simulated. Results, equivalent capacitance, which represent consumed energy, are collected in colored tables (e.g. Table I).

III. Results

Analyzing numbers collected in tables some conclusions for adders design can be derived. It is seen that some realizations are better for some distributions of input vector changes. In many cases the Ripple Carry Adder (sum4b_3p7) is the best realization. But the second one is usually only a few percent worse than RCA, about 1 or 2 %. Use of black cells, number of levels and valency of cells are analyzed in context of power consumption.

IV. Conclusions

In the paper comparison of power consumption of PPA under advanced analysis were presented. Only propagation-generation tree was considered. Analyzed structures are shown as diagrams and results are collected in colored tables. Structures of adders in aspect of kind of summed data should be taken into consideration during design for low power.

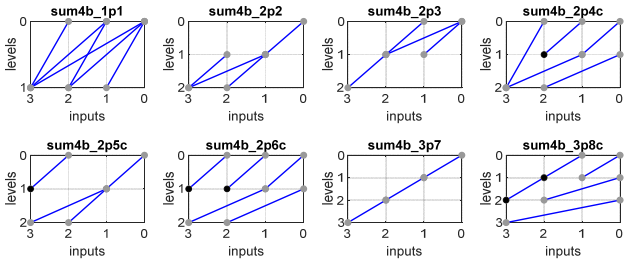


Fig. 1. Diagrams of PG blocks for 4-bit parallel prefix adder.

TABLE I.
Total equivalent capacitance of PG tree [fF] for 4-bit adders (frag.)

Adder Name	Distribution Name											
	unif.	*ser1*	*ser3*	*ser4*	*ser9*	*ser11*	*ser12*	*sin1*	*sin3*	*sin5*	*sin11*	*sin12*
sum4b_1p1	19.0	18.7	*10.9*	10.9	19.1	14.8	18.7	8.2	4.8	7.4	6.7	10.2
sum4b_2p2	16.8	16.1	*10.9*	11.0	16.8	*12.9*	16.4	6.7	3.8	5.6	5.2	8.7
sum4b_2p3c	16.7	15.0	10.9	10.9	16.4	13.4	16.3	6.7	4.1	6.1	5.3	8.8
sum4b_2p4c	24.2	23.5	**15.3**	**15.4**	24.4	19.8	24.0	**9.3**	5.5	8.3	7.4	**12.2**
sum4b_2p5c	22.4	19.9	10.9	*10.9*	22.1	15.4	20.0	7.3	4.1	6.2	5.6	9.2
sum4b_2p6c	**28.3**	**25.7**	13.6	13.7	**28.2**	20.9	25.9	9.0	5.4	8.2	7.2	11.6
sum4b_3p7	*16.4*	*14.7*	11.7	11.8	*16.0*	13.0	*15.9*	*6.2*	*3.7*	*5.5*	*4.8*	*8.5*
sum4b_3p8c	28.2	23.7	13.7	13.7	27.8	**21.2**	**26.4**	9.0	**5.7**	**8.6**	**7.4**	11.9

This work has been supported by AGH University of Science and Technology under subvention funds (no. 16.16.230.434).

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Low Hardware Complexity Filters for On-Chip Algorithm Used in Air Pollution Sensors for Dense Urban Areas in Smart Cities

Zofia Długosz[1], Michał Rajewski[1], Marzena Banach[2], Tomasz Talaśka [1], Rafał Długosz[1]
[1] UTP University of Science and Technology
Faculty of Telecommunication, Computer Science and Electrical Engineering
ul. Kaliskiego 7, 85-796, Bydgoszcz, Poland
[2] Poznan University of Technology
Institute of Architecture and Spatial Planning
Nieszawska 13C, 61-021 Poznań, Poland
E-mail: zosia.dlugosz@gmail.com, michalrajon@gmail.com, marzena.banach@put.poznan.pl,
tomasz.talaska@gmail.com, rafal.dlugosz@gmail.com

***Abstract*—The paper presents a method of transistor level implementation of a reconfigurable filter for the application in the algorithm responsible for processing air pollution data. The assumption of the proposed solutions is the realization of the algorithm that uses such filters directly in the wireless sensor, along with other components of such devices. Thanks to this, the amount of data exchanged between the sensors and the base station can be reduced. In the proposed filter structure, a special emphasis was placed on reducing the hardware complexity of the filter. The objective is to reduce the chip area of the overall device. The filter features a modular reconfigurable structure, which allows to achieve different filter orders, with almost linear increase in the hardware complexity. Target application of the proposed solution is in wireless sensors networks (WSN) that consist of large numbers of devices distributed, e.g. in dense urban areas in cities.**

***Keywords*—Air pollution sensors; Air pollution data processing; Filters; Edge computing**

I. Introduction

Air pollution belongs to one of the key problems in cities today. According to the United States Environmental Protection Agency, various types of air pollutants, especially those designated as particulate matter $\mathrm{PM}_{2.5}$ and PM_{10} (smog), are hazardous to human health [1]. This applies especially to the particles with diameters below 2.5 μm, as their size allows them to enter the human blood directly. Prevention of the described problems is one of the basic assumptions and ecological goals of theoreticians of the, so-called, smart cities.

This problem may be observed through more and more popular networks of air pollution sensors. Such networks allow to create air pollution maps showing the levels of pollution in cities, with a relatively frequent update of current situation.

Pollution levels depend heavily transportation in cities, on weather conditions, insolation level, wind strength and direction, season of the year, etc. A factor that also substantially impacts the course of the air pollution over time in cities is the structure of urban development, as urban density and height of buildings have an impact on ventilation abilities.

Pedestrians and cyclists belong to the group of people, moving in an urban space, that is particularly exposed to pollutions. Usually they move around the city without any cover. Considering this, we believe that maps with higher spatial resolution are needed than those currently offered. These maps should be also updated more frequently. This would allow the mentioned users of the cities to plan their routes in such a way to avoid the most polluted areas.

The described problem may be addressed through the development of air pollution monitoring systems based on wireless sensor network (WSN) composed of miniaturized, low power devices densely distributed in the urban environment. The idea is to enable the monitoring at the level even of particular streets. More dense maps require a large number of sensors, which should be substantially cheaper than devices available today. They should also allow for an easy installation in the urban infrastructure of the cities. This may be achieved by eliminating the need for an external power supply.

Low power operation and the ability to achieve compact sizes requires the optimization of particular circuit components of the sensors. The purpose of this work is to contribute to the development of such solutions. It is a continuation of our earlier work presented in [2]. Here, we focus specifically on filters, which are one of the main components of the previously proposed algorithm responsible for analysis of recorded data.

References

[1] United States Environmental Protection Agency, „Particulate Matter (PM) Basics", https://www.epa.gov/pm-pollution/particulate-matter-pm-basics. (access 2020.02.17)
[2] Banach, M., Długosz, R., Pauk, J., Talaśka, T. "Hardware Efficient Solutions for Wireless Air Pollution Sensors Dedicated to Dense Urban Areas". *Remote Sensing*, Vol. 12, Issue 776, 2020.

Low Power Preamplifier for Biomedical Signal Digitization

Nawaf ALjehani[1], Mohamed Abbas[1,2]
[1] EE Department, College of Engineering, King Saud University, Kingdom of Saudi Arabia
[2] EE Department, Faculty of Engineering, Assiut University, Egypt
mohabbas@ksu.edu.sa
437105870@student.ksu.edu.sa

SUMMARY

This paper presents a low power, low noise preamplifier stage with simple common mode desensitization circuit for dynamic comparators. The target application of the proposed circuit is analog to digital converter for biomedical applications. Adopting TSMC 0.18µm technology, the proposed circuit (as shown in Figure 1) is designed to work in weak inversion using gm/ID design methodology. The simulation results (as shown in Figure 2) show that the preamplifier stage consumes less than 32nW using power supply of 0.75V. The input referred noise is 17µV, DC gain of 43.15dB and unity gain frequency of 300 kHz.

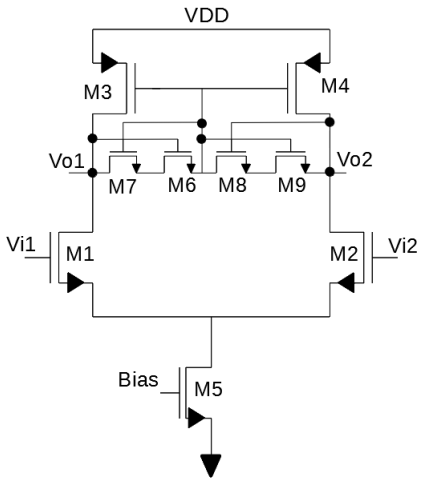


Figure 1. Proposed preamplifier circuit

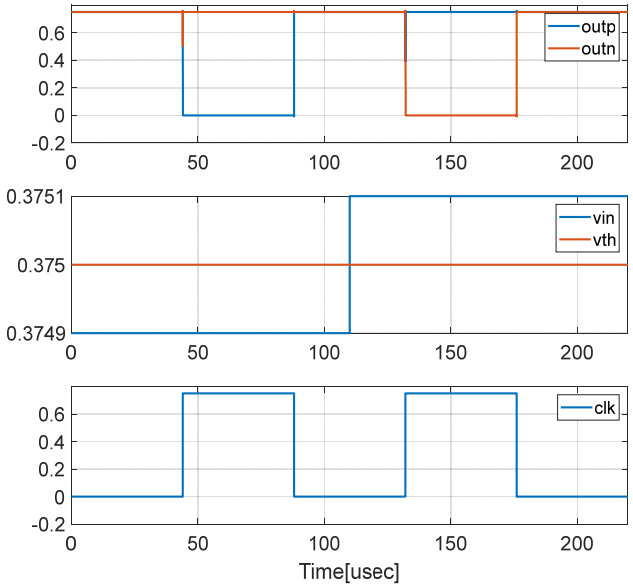


Figure 2. Sample simulation of outputs, inputs and control clock of the comparator

Multichannel Programmable Readout IC for Photodiodes Array

Paweł Pieńczuk, Cezary Kołaciński, Andrzej Szymański, Paweł Janus,
Krzysztof Kucharski, Dariusz Obrębski, Michał Zbieć, Mariusz Jakubowski
Sieć Badawcza Łukasiewicz — Instytut Technologii Elektronowej
Warsaw, Poland
E-mails: pawel.pienczuk@ite.waw.pl, ckolacin@ite.waw.pl, aszym@ite.waw.pl, janus@ite.waw.pl,
kucharsk@ite.waw.pl, zbiec@ite.waw.pl, obrebski@ite.waw.pl, mariusz.jakubowski@ite.waw.pl

***Abstract*—This paper describes the design of the 17-channel readout integrated circuit targeted to front-end operation for photodiodes array. Proposed system contains an analog front-end electronics digitally configured using built-in Serial Peripheral Interface. Each signal channel has been designed for one particular set of photodiodes. Chip was designed and fabricated utilizing CMOS 0.18 μm technology and occupies area of 4960 μm x 1525 μm. Total current consumption is expected to be less than 33 mW (with 3.3 V supply).**

***Keywords*—CMOS, ParCour, photodiodes, readout.**

Extended Abstract

Under the ParCour project, the established consortium develops a new particle counting technique, with an aim of cost and mobility. A new measurement apparatus will be based on a LED light source, additional optical systems, an unique photodiodes (PDs) array and a designed integrated circuit for readout.

PDs array is organized as a ring structure consisting 17 sections with different sizes and position. The central PD is used for calibration. The remaining 16 sections form 120° arcs. This structure has been manufactured in Łukasiewicz-ITE CMOS-based technology. PDs array has been assembled in a PLCC32 package.

Designed readout chip features 17 analog input ports, 17 analog output ports, SPI Interface and several diagnostic and auxiliary ports. Analog blocks consists of 17 separate channels, one for each PDs section. Developed front-end circuit converts input current signals into output voltage signals. Digital interface configures analog block parameters. It is comprised of calibration registers which can be accessed via the Serial Peripheral Interface (SPI) bus. Power-on Reset (PoR) block reset registers at every power-up event. Presented IC contains built-in bandgap reference (BGR) source, providing reference voltage. Dedicated diagnostic ports were added to observe several internal signals. Both analog and digital domains are separated in order to minimize the noise and distortion effects.

Single signal path is composed of two amplification blocks: a transimpedance amplifier (TIA) and a voltage amplifier (buffer). Offset of these two stages can be controlled by 4-bit configuration port (within a limited range). It is realized by turning on and off transistor connected in parellel and matched to the input differential pair. Effectively, the size of input differential amplifier is changed. Gain is controlled by configurable feedback loop resistor. 4-bit input port adjusts the gain by adding or removing particular resistors. Channel 0., dedicated to the central PD, has slightly different structure, due to smallest capacitance and largest output current.

The digital part provides calibration for entire readout IC by 3 4-bit registers per each channel. The first register configures the TIA gain, the second and third one provide voltage offset adjustment of the TIA and the buffer, respectively. At start-up, all the registers are reset by the PoR block.

Configuration process is realized with the SPI protocol and 2-byte data frame. Each configuration word addresses particular register in specific channel and passes 4-bit value in 11 least-significant bits. Last 5 bits are ignored. Proper configuration of all internal registers lasts for $17 \cdot 16 \cdot 3 = 816$ cycles.

Total current consumption has been estimated at 10 mA for the complete chip (at 3.3 V power supply). Structure was fabricated in UMC CMOS 180nm technology, occupies area of 4960 μm x 1525 μm and is equipped with 57 I/O pads.

Test environment, including printed-circuit board (PCB), auxiliaries and dedicated software, was developed. Problem of low current AC stimuli was solved using two types of analog optocouplers. At the moment (end of February) fabricated chips are under characterization. Eventually, the integration of whole particle counting system will be executed. The project can be extended by adding analog-to-digital converter (ADC) and processing auxiliaries, in purpose of minimization and mobility.

Acknowledgment

The presented experiments were supported by the Poland-Berlin-Brandenburg Project no. 2/POLBER-3/2018 Parcour — "Particle counter".

Relocatable Partial Bitstreams For Virtual Overlay Architectures atop Field-Programmable Gate Arrays

Zbigniew Mudza
Department of Microelectronics and Computer Science,
Lodz University of Technology
Lodz, Poland

EXTENDED ABSTRACT

FPGA usage in systems that require frequent changes of functionality is very limited due to long development cycle and reconfiguration time. An intermediate virtual architecture overlay with individually reconfigurable modules can be used to address both these issues. Simplified platform independent high-level abstraction architecture models provided by overlays are convenient for software developers and can be easily migrated between different FPGA devices. Partial reconfiguration can be used to reprogram individual modules independently from the rest of the system, which reduce reconfiguration time dramatically.

Generally, each partition (an individually reconfigurable module instance) uses its own set of configuration data bitstreams defining multiple variants of possible functionality. The static part of the system remains uses global bitstream and remain unchanged during the system operation. Homogeneous reconfigurable modules could potentially use common configuration data, which would reduce required program memory storage space. In the case of Xilinx 7 Series FPGA devices, a bitstream can be relocated to a different partition provided that source and destination partitions represent the same functionality and their floorplanning (spatial distribution of assigned resources and ports location) is compatible.

An overlay can be designed in the way that functionally equivalent modules are assigned to compatible partitions, despite no relocatability support in the design workflow tools (Vivado Design Suite in the case of Xilinx 7 series). In order to achieve the desired partition floorplanning design constraints for placement and routing needs to be applied to force the automated tools to preserve the compatibility of partitions during the implementation process. Additionally, global connections must be prevented from using feed-through connections crossing the partitions, as those nets could be disconnected in case of relocation.

The proposed methodology can be summarized in a form of the following consecutive steps:

- Logical synthesis of the overlay architecture with black-box reconfigurable modules (RM).
- Module assignment to partitions of identical spatial resource distribution.
- Isolation interspace insertion between static and reconfigurable partitions.
- Reference partition selection and static-to-reference connection area restriction.
- Isolation Design Flow implementation of the reference partition.
- Partitions constraining based on extracted tool-generated placement and routing properties of the reference partition.
- Isolation Design Flow implementation of the entire overlay with empty RM partitions.
- Overlay design checkpoint export.
- Implementation of desired RM functionality using Partial Reconfiguration Flow
- Partial bitstream generation
- Bitstream relocation - Frame Address Register offset and CRC value updates.

The proposed methodology was used to generate relocatable bitstreams for proof-of-concept design targeting Artix-7 XC7A200T. For a group of partitions identical bitstreams were obtained using relocation and independent implementation with full partition constraining. However, individual inconsistencies were found in some other partitions and are currently examined.

REFERENCES

[1] Jain A. K,. Maskell D. L., Fahmy S. A., "*Are Coarse-Grained Overlays Ready for GeneralPurpose Application Acceleration on FPGAs?*", IEEE International Symposium on Dependable Autonomic and Secure Computing (DASC), 2016

[2] Oomen R., Nguyen T., Kumar A., Corporaal H., "*An automated technique to generate relocatable partial bitstreams for Xilinx FPGAs"*, 25th International Conference on Field Programable Logic and Applications, 2015

[3] Rettkowski J., Friesen K., Gohringer D., "*RePaBit: Automated Generation of Relocatable Partial Bitstreams for Xilinx Zynq FPGAs"*, International Conference on Reconfigurable Computing and FPGAs (ReConFig), 2016

[4] Xilinx, Hallet E., "Isolation Desing Flow For Xilinx 7 Series FPGAs or Zynq-700 AP SoCs (Vivado Tools)", 2016

[5] Xilinx, "Vivado Design Suite User Guide Partial Reconfiguration", UG909 (v2018.3), 2018

[6] Xilinx, "7 Series FPGAs Configuration User Guide", UG470 (v1.13.1), 2018

[7] Xilinx, "Vivado Design Suite User Guide Implementation", UG904 (v2019.2), 2019

[8] Xilinx, "Vivado Design Suite User Guide Using Constraints", UG903 (v2018.1), 20118

Thermal Issues in Microelectronics

Comparison of Set-ups Dedicated to Measure Thermal Parameters of Power LEDs

Krzysztof Górecki, Przemysław Ptak
Department of Marine Electronics
Gdynia Maritime University, Gdynia, Poland
k.gorecki@we.umg.edu.pl, p.ptak@we.umg.edu.pl

Marcin Janicki
Department of Microelectronics and Computer Science
Łódź University of Technology, Łódź, Poland
janicki@dmcs.pl

EXTENDED ABSTRACT

Power Light Emitting Diodes (LEDs) are basic components of modern lighting systems. The operating parameters of these devices strongly depend on temperature. The transient thermal behaviour of LEDs can be fully characterised by their thermal impedance $Z_{th}(t)$. Thermal parameters of these devices depend not only on the operating point, but also on the specific cooling conditions. Hence, the proper characterization of LED thermal properties normally requires numerous measurements of their thermal responses carried out in various conditions.

The method of measuring the thermal impedance of power LEDs is described in the JEDEC standard, which contains also the description of the measurement set-ups. The commercially available transient thermal tester T3Ster® complying with the standard is available at the Department of Microelectronics and Computer Science (DMCS) of Łódź University of Technology, Poland. The standard system includes also the Master software implementing the Network Identification by Deconvolution method and offering thermal analysis tools rendering possible the estimation of various parameters of investigated devices, such as the thermal time constant spectra.

However, this piece of equipment is relatively expensive, hence a custom solution was developed in Poland at the Gdynia Maritime University (GMU). This system allows additionally measurements of radiant power emitted by LEDs, what is not possible using the basic version of the standard equipment, but it is indispensable for the proper determination of power LED thermal impedance. The main disadvantage of the new custom solution is that it renders possible measurements only in with free convection cooling conditions.

This custom measurement system also includes a software, called ESTYM, which allows the estimation of thermal time constants. Therefore, the main goal of this paper was not only to compare measurement results obtained for different LEDs with the two measurement systems considered here, but also to provide comprehensive thermal analyses of the thermal time constant spectra computed with the commercial Master and the custom ESTYM software.

This paper presents the results of LED thermal impedance measurements performed for three types of devices at different cooling conditions, with and without a heat sink. An example of such measurements is shown in Fig. 1. The results obtained with the standard system are denoted by the solid lines whereas the ones obtained with the custom system by the dashed ones. As can be seen the results are quite similar and the differences occurring mainly in the transient states might result only from measurement errors. The measurement results were processed further obtaining the time constant spectra, such as the one presented in Fig. 2. Most peaks in the spectra appear in similar locations and they have comparable magnitude, hence proving the correctness of the implemented estimation algorithm,

The analyses presented in this paper demonstrated that both systems yield comparable results. Therefore, it could be stated that the custom hardware solution and the ESTYM software developed at GMU operate correctly rendering possible the measurements of thermal impedance, LED optical power and the evaluation of thermal time constants. An obvious additional advantage of the custom system is that is much cheaper than the standard one.

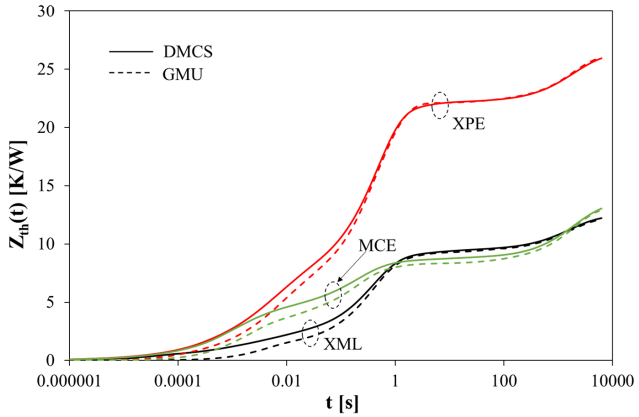


Fig. 1. Comparison of measured thermal impedances.

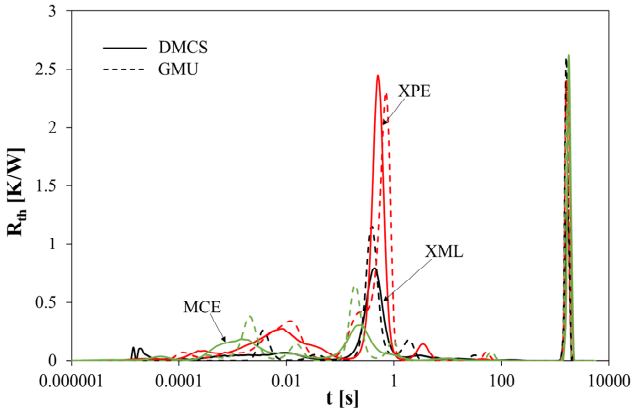


Fig. 2. Comparison of computed thermal time constant spectra.

Investigations Properties of Selected Methods of Measurements of Thermal Parameters of the IGBT

Krzysztof Górecki, Paweł Górecki
Department of Marine Electronics
Gdynia Maritime University
Gdynia, Poland
k.gorecki@we.umg.edu.pl, p.gorecki@we.umg.edu.pl

EXTENDED ABSTRACT

IGBTs are used in many electronic and power electronics circuits. Their properties strongly depend on temperature. Internal temperature T_j of the considered transistor exceeds ambient temperature T_a as a result of self-heating phenomena.

In order to estimate an increase of internal temperature of the semiconductor device over ambient temperature at dissipation of power of the fixed value in this device, thermal parameters are used. These parameters are transient thermal impedance $Z_{th}(t)$ and thermal resistance R_{th}. These parameters characterise efficiency of removal of heat generated in the examined semiconductor device to the surrounding and their values depend on cooling conditions of this device. Reliable determination of these parameters demands performance of suitable measurements.

The considered thermal parameters are measured with the use of suitable definitional formulas. Particularly, thermal resistance is described by the dependence of the form

$$R_{th} = \frac{T_j - T_a}{P} \tag{1}$$

where P is power dissipated in the tested device.

Values of temperature T_a and power P can be measured in an easy way, whereas the value of temperature T_j cannot be measured directly. The value of this temperature is measured indirectly with the use of optical or electric methods. Optical methods make it possible to measure temperature of the semiconductor structure only in the case of laboratory semiconductor devices without the case, whereas for commercially made devices with cases optical methods make it possible only to measure the case temperature T_C.

In turn, indirect electric methods allow determining internal temperature of the device basing on measurements of the value of the selected electric parameter univocally dependent on temperature - a thermo-sensitive parameter. In the literature possibilities of the use of different thermo-sensitive parameters to measure internal temperature of different semiconductor devices are considered. In the case of IGBTs voltage between the gate and the emitter of the transistor operating in the active range, voltage between the collector and the emitter on the switched-on transistor or voltage on the forward biased anti-parallel diode are used.

In the paper influence of the method of measurements on thermal resistance of the IGBT is analysed. The indirect electrical and optical methods are considered. In the electrical method, in turn two thermo-sensitive parameters: gate-source voltage V_{GE} and voltage V_D on the forward biased anti-parallel diode are used.

On the basis of the obtained results it is stated that thermometric characteristics $V_{GE}(T)$ are non-linear and can be approximated with big accuracy by a square function. In turn, thermometric characteristics $V_D(T)$ are practically linear. The slope of the characteristic $V_{GE}(T)$ is even twice higher than the slope of the characteristic $V_D(T)$. This means that with the use of voltage V_{GE} it is possible to obtain a smaller value of the measurement error of thermal resistance than with the use of voltage V_D.

It is also shown that the measuring error of thermal resistance determined with the use of the method of the complete differential is a decreasing function of an excess of internal temperature over ambient temperature. If this increase attains 100 K, the measuring error of thermal resistance with the electric method does not exceed 4%. This error is higher for the optical method due to occurrence of thermal resistance between the semiconductor structure and the case.

The obtained results of measurements of thermal resistance of the considered transistor show that with the use of the indirect electrical method the difference between values of the considered parameter obtained with the use of voltages V_{GE} and V_D as thermo-sensitive parameters is observed. Due to the fact that the diode is the separate semiconductor structure situated in the common case with the transistor and power is dissipated in the transistor its temperature is lower than for the IGBT. Values of thermal resistance obtained with the use of these thermo-sensitive parameters do not differ between each other more than about 5%. This difference is only imperceptibly higher than the estimated error of measurements. In turn, the value of this parameter obtained by means of the optical method is underestimated by about 10%. It is proper also to notice that the measured dependences of thermal resistance on power are decreasing functions and a drop in the value of this parameter in the considered range of changes of power reaches even 25%.

The obtained results show that the use of the optical method of measurements can cause indeed understating of the value of thermal resistance. The results of measurements of this parameter with the use of the electrical method and one of the considered thermo-sensitive parameters do not differ from each other.

Thermal Characterization of Electronic Components Using Single-detector IR Measurement and 3D Heat Transfer Modelling

Michał Kopeć, Bogusław Więcek
Institute of Electronics
Lodz University of Technology
Lodz, Poland
michal.kopec@edu.p.lodz.pl, boguslaw.wiecek@p.lodz.pl

EXTENDED ABSTRACT

Thermal impedance concept is still used in electronics for thermal testing and management both in production and exploitation. There are standard procedures and methodology of measuring thermal impedance in practice. This methodology has the fundamental limits. It can be effectively applied only for devices with dominant one dimensional heat transfer. In addition, in practice, a Device Under Test (DUT) can only be powered by the approximated Heaviside step function excitation, what can lead to the erroneous results, especially in the high frequency range of the thermal impedance. Another main engineering problems in such measurements is to evaluate temperature in the heat source, what is impossible in the general case. Moreover, the overall methodology is based on the inverse thermal problem solution, which is by definition, ill-conditioned. In the existing commercially available apparatus, temperature is measured using a contact method.

In this research presented this paper, a novel methodology of thermal impedance measurement by temperature monitoring out of the heat source in a power transistor is presented. A low-cost Infra-Red (IR) head is used to register evolution of temperature after step-function powering. A dedicated power generator has been developed to synchronize temperature recording with power dissipation in a device. Simultaneously, the 3D FEM thermal model of a DUT was elaborated to calculate the step-function temperature response vs. time on the outer surface of the transistor's case. Modelling was realized using the Comsol environment. Fitting of temperature rise by changing thermal parameters of a DUT, obtained from measurement and simulation was then made using optimization procedure. Next, the thermal impedance, in the form of the Nyquist plot was numerically calculated using the Filon integration. In addition, converting the Nyquist plot given as the frequency-series, into the analytical rational transfer function (Zth) was performed. It is the crucial step of the proposed methodology. Finally, in order to estimate the discrete thermal time constant distribution, the Foster network approximation was calculated. The proposed methodology of thermal analysis of power devices is presented in Fig. 1.

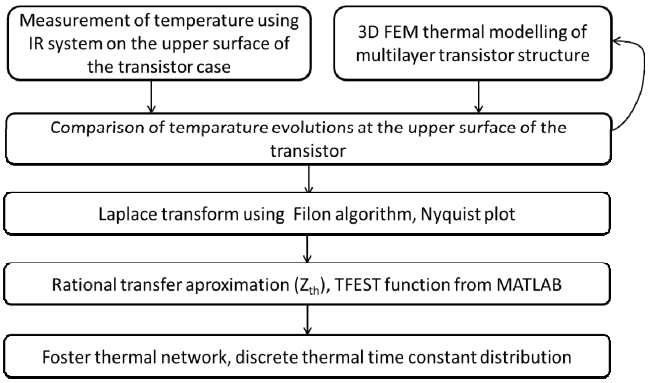


Fig. 1. The algorithm of the proposed method thermal characterization of power devices using IR measurement

The developed measurement setup enables precise placement of a tested object under the IR system. It consists of single-detector IR head, developed electronic controller, z-axis moveable stand and x-y micrometer table. The important function of the developed controller is the precise synchronization of temperature measurement and power dissipation in a DUT. Software of the developed controller enables setting of sampling period Ts, acquisition time t_M and dissipated power P_D in a DUT.

In this paper, the application of IR temperature measurement on the surface of a power device and 3D thermal simulation are presented to estimate the thermal impedance. The simulation model was developed using COMSOL Multiphysics software. The Heat Transfer in Solids interface of the Heat Transfer Module was used to carry out time dependent analysis. The low-cost IR single-detector system was developed to measure the temperature synchronously with the power dissipated in a DUT using step-function excitation. The example of measurement and comparison of results obtained from the new low-cost and commercially available systems are presented showing the acceptable accordance.

Analysis and Modelling of ICs and Microsystems

A Process, Voltage and Temperature Dependent Modeling Methodology for Industrial Requirements

Ivan Sejc, Robert Kappel
ams AG
Premstaetten, Austria
ivan.sejc@ams.com, robert.kappel@ams.com

EXTENDED ABSTRACT

Time efficient and accurate design verification is a key procedure in an industrial environment. In order to achieve both, a behavioral modeling can be used instead of more complex SPICE model options. This, however, requires a significant model complexity. This paper proposes a PVT and Monte Carlo modeling methodology based on the generation of polynomial equations with Matlab environment. The methodology is divided in three main steps as shown in the figure 1.

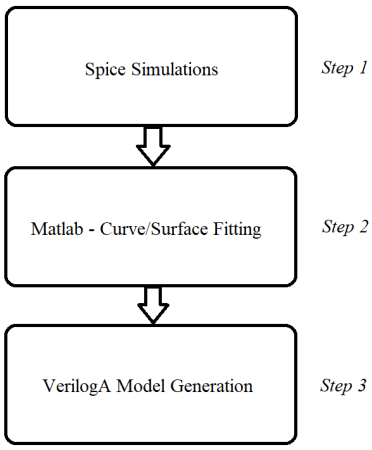


Figure 1. Modeling flow

The first step is to perform all the necessary SPICE simulations to obtain the output parameter *y* as a function of required input variables e.g. temperature, supply voltage or process corner. The output data are then saved as a *.csv* file and prepared for post-processing. In the case of MC simulations, Gaussian distribution of the parameter *y* is obtained. The mean value and standard deviation are extracted from the simulation. The second step of the modeling methodology is generation of all the necessary mathematical equations in order to describe the behavior of the output *y* by using Matlab Curve and Surface Fitting toolbox, since it provides relatively fast and user-friendly approach. The third step is generation of a VerilogA model based on the derived equations in step 2. The output parameter quantity, either voltage or current can be simply considered as a function *y(T, VDD, process corner)*. The overall methodology is tested on the example of bandgap reference voltage circuit where reference voltage V_{ref} is an output parameter as shown in the figure 2.

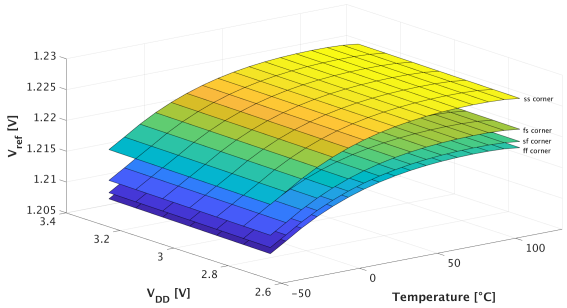


Figure 2. V_{ref} as function of temperature and supply voltage V_{DD} and process corner

The simulation proved a significant difference in simulation time between behavioral and SPICE models. The simulation time of the behavioral model is almost 20 times shorter in the case of transient simulation than the SPICE model. The simulation time of the behavioral model shows almost 6 times improvement compared to SPICE based model during Monte Carlo simulation.

Capacitance Deviation Caused by Mechanical Deformation of MEMS Inertial Structure

Jacek Nazdrowicz, Adam Stawiński, Andrzej Napieralski
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
jnazdrowicz@dmcs.pl, astawinski@dmcs.pl, napier@dmcs.pl

EXTENDED ABSTRACT

Authors presents a very important problem of estimation capacitance structures used in MEMS sensors. The importance comes from the fact that during operation, inertial sensors deform under influence of external forces. The result of the problem is visible in capacitance deviations what directly may be seen in accuracy sensor measurement.

The MEMS comb capacitors consist of numbers of parallel electrodes. Capacitance estimation in a perfect situation (when all electrodes are in parallel) is very easy. These are just parallelly connected single capacitors and calculation of capacitance may be performed with use popular formula:

$$C_{comb} = \sum_{i=1}^{n} C_i = n\varepsilon\frac{A}{d}$$

The above formula assumes, that dimensions of all electrode fingers are the same and distances between stationary and movable electrodes are constant.

However, in case of solid inertial MEMS devices like sensors (where many details are combined with and these details are very susceptible to deformation), any displacement from equilibrium state, anchors, combination with springs potentially causes unnecessary structure stresses and deformations. Moreover, the source of these deformations may come also from other external sources like temperature. Those mentioned above factors influence on capacitance measurements and in turn, accuracy of sensors.

We see in fig. 1, that particular electrode location and orientation changes and it is in fact caused by supporting beam deformation. Each finger is oriented with different angle from the original position, therefore, it is crucial to calculate capacitance separately.

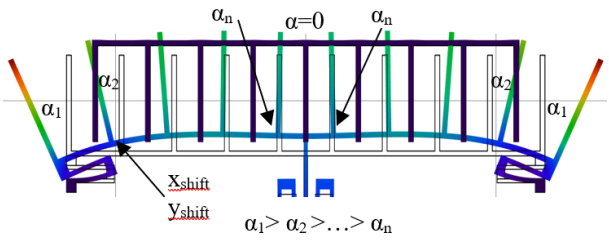


Fig. 1. Different angles of electrodes caused by structure deformation.

Particular capacitances C_1 and C_2 in dependency of angle are presented in fig. 2 and 3. The stronger dependency on angle is in case of C_1 and it is strongly nonlinear. For angle close to maximum value capacitance drastically grows. Fig. 2. shows that capacitance C_1 grows exponentially as electrode angle grows from $1*10^{-14}$ to $6.5*10^{-14}$ F – thus, the growth is more than 6 times.

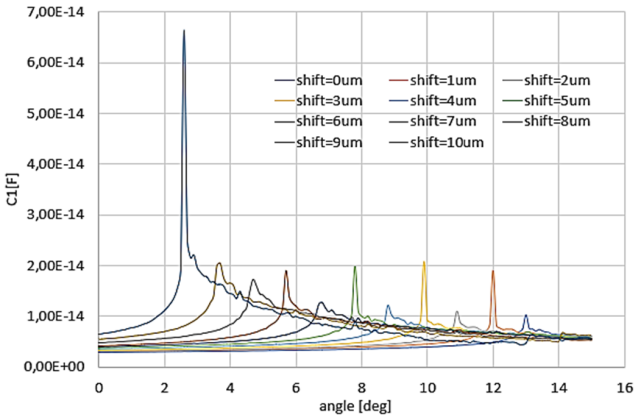


Fig. 2. C_1 capacitance dependency on angle for different electrode shift caused temperature expansion.

In fig. 3. It can be seen that C_2 decreases for each shift along with angle growth, however the capacitance difference between particular values decreases along with angle grows. Consequently capacitance difference plot has the same shape like C_1 (fig. 2) but it is shifted along with capacitance axis.

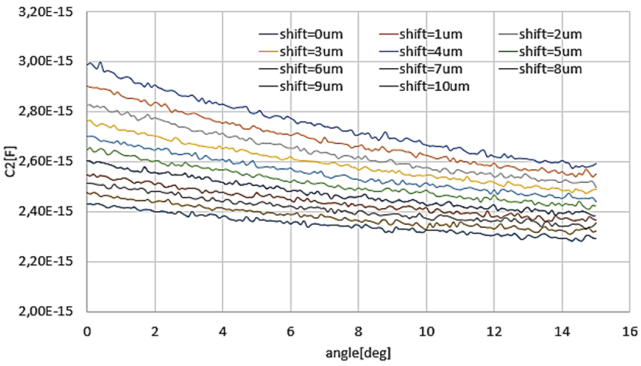


Fig. 3. C_2 capacitance dependency on angle for different electrode shift caused temperature expansion.

Noise Resistance Estimation for a GaN JFET Using Small Signal Measurements for an X-band LNA

Evangelia A. Karagianni[1], Christina C. Lessi[2], Christos N. Vazouras[1], Athanasios D. Panagopoulos[2], George Deligeorgis[3], George Stavrinidis[3], Athanasios Kostopoulos[3]

[1]Hellenic Naval Academy
Piraeus, Greece

[2]National Technical University of Athens
Athens, Greece

[3]Foundation for Research and Technology Hellas
Creta, Greece

{evka, chvazour}@hna.gr, chrislessiee@gmail.com, thpanag@ece.ntua.gr, {deligeo, gstav, kosto}@physics.uoc.gr

Extended Abstract

Gallium Nitride technology is entering dynamically in the area of manufacturing integrated circuits. In this paper the design of a Low Noise Amplifier is presented. The transistor that is used is a bilateral, conditionally stable transistor and it has been built at the Foundation for Research and Technology Hellas. It is measured in order to get the Scattering parameters and the Noise Figure. The Noise Figure is additionally calculated, together with the noise resistance and the error between the calculated and the measured values is estimated for a single stage amplifier. The Rn is calculated and the error inserted to the NF is less than 0.4% at the operating frequency. Once the error between the original NF measured and the calculated one is acceptable, we proceed to the LNA design.

For the first stage of the LNA the transistor is polarized with VGS at 2.5Volts, VDS at 15Volts and drain-source current at 32mA. The transistor is conditionally stable and bilateral. The maximum gain is 10.79 dB at 10GHz. A method to deal with the problem of oscillations is accomplished through a coil at the source, with the aim of eliminating parasitic capacities increase gain. After connecting the proper matching circuits to the input and output of the first stage, the circuit of Figure 1 is obtained, with the results as shown in Figure 2. The LNA is stable at frequencies from 5 to 15GHz. The maximum gain is 6.94 dB at 10GHz and the NF is 3.2dB, almost 6% higher than the minimum of the transistor. Regarding the design of the inductors, they must consist of as many coils as possible in order to avoid coupling between adjacent coils in the layout. However, the initial design that has taken place has taken into account to some extent coupling between adjacent coils to avoid problems with the amplifier layout.

This design is ambitious and full of challenges, as it seems to be necessary to use the stability resistor, which worsens the transistor noise characteristics. This design give a NF=3.2 dB and a maximum gain approximately 7 dB. As the design is successful, the amplifier will be manufactured and measured.

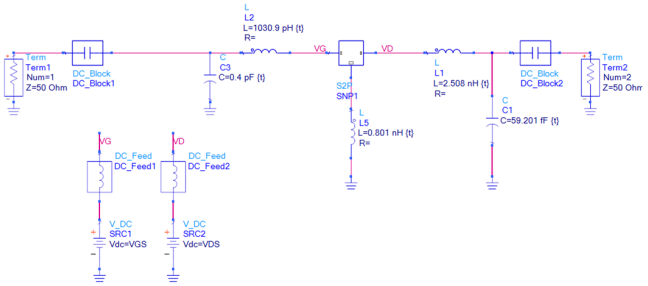


Fig. 1. Simulated circuit with the optimized matching circuits for the input and output, with the use of ADS (Advanced Design System)

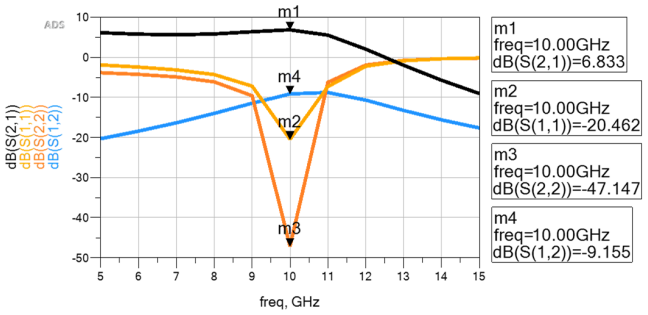


Fig. 2. Simulated results for the LNA's S-paremeters with the use of ADS

This research has been co-financed by the European Union and Greek national funds through the Operational Program Competitiveness, Entrepreneurship and Innovation, under the call RESEARCH – CREATE – INNOVATE (project code: T1EDK-00329) and Hellenic Navy, Hellenic Ministry of Defence.

On Applications of Fractional Derivatives in Circuit Theory

Jacek Gulgowski
University of Gdansk
80-308 Gdansk, Poland
Email: jacek.gulgowski@mat.ug.edu.pl

Tomasz P. Stefański
Gdansk University of Technology
80-233 Gdansk, Poland
Email: tomasz.stefanski@pg.edu.pl

Damian Trofimowicz
SpaceForest Ltd.
81-451 Gdynia, Poland
Email: d.trofimowicz@gmail.com

EXTENDED ABSTRACT

The fractional-order (FO) calculus is a branch of mathematics investigating formulations of the derivative operator D^α with the order α being a real number ($\alpha \in \mathbb{R}$). Hence, the FO derivative operator D^α is a generalization of the standard integer-order (IO) concept of the n-fold differentiation D^n where n is an integer number ($n \in \mathbb{Z}$). The FO calculus has been applied in the circuit theory for many years [1]. Reviews of numerous formulations of FO derivatives can be found in classical monographs [2]. Some definitions of FO derivatives are well established and already applied in the circuit theory, whilst some definitions have been introduced recently. Hence, we discuss the applicability of four important derivative definitions, i.e., Riemann-Liouville, Caputo, Grünwald-Letnikov and Marchaud, from the circuit theory point of view. The ambiguity of definitions of the FO derivative, whose properties sometimes exclude them from applications in the circuit theory, is the motivation for our research. Recently, opinions appear that questionize applicability of FO derivatives and models in electrical sciences and engineering [3]–[5]. Such a discussion in literature suggests that the proposed analysis of properties of FO derivatives is currently necessary.

In our opinion, the FO derivative employed in the circuit theory must satisfy the following properties:

1) *Identity*
$$D^0 f(t) = f(t). \tag{1}$$
2) *Compatibility with IO Derivative*
$$D^\alpha f(t) = \frac{d^\alpha}{dt^\alpha} f(t), \qquad \alpha \in \mathbb{N}. \tag{2}$$
3) *Compatibility with IO Integral*
$$D^{-\alpha} f(t) = \int \cdots \int f(t) d^\alpha t, \qquad \alpha \in \mathbb{N}. \tag{3}$$
4) *Linearity*
$$D^\alpha (af(t) + bg(t)) = aD^\alpha f(t) + bD^\alpha g(t). \tag{4}$$
5) *Semigroup Property (also called the index law)*
$$D^\alpha D^\beta f(t) = D^\beta D^\alpha f(t) = D^{\alpha+\beta} f(t), \quad \alpha, \beta \in \mathbb{R}. \tag{5}$$
As it is noticed in [4], the condition (5) may not be satisfied for widely applied definitions of FO derivative.
6) *Trigonometric Functions Invariance*
$$D^\alpha e^{j\omega t} = (j\omega)^\alpha e^{j\omega t} \tag{6}$$
where $j = \sqrt{-1}$. This property is a generalization of the fundamental formula taken from the IO calculus. It is required for the representation of signals in the phasor analysis of circuits.
7) *Constant Function Derivative*
$$D^\alpha C = 0 \tag{7}$$
where $C = Const$. This property results from the trigonometric functions invariance because one obtains (7) from (6) for $\omega = 0$.

The circuit analysis can be executed in either time or frequency domain. The solutions obtained in both domains should be equivalent which means that results of time- and frequency-domain circuit analyses should be related by the Fourier transform. The properties (1)–(7) are required when using the classical methods of the circuit theory. In the paper, we demonstrate inconsistencies which can arise when the semigroup property is not valid for the FO derivative. Out of four of the most popular approaches considered in this paper, only two of them are looking at the entire time-history of an input function and are appropriate choices for the circuit theory. The Riemann-Liouville and Caputo derivatives with finite base point have a limited applicability, whereas the Grünwald-Letnikov and Marchaud definitions (which are actually equivalent) lead to reasonable results.

REFERENCES

[1] M. D. Ortigueira, "An introduction to the fractional continuous-time linear systems: the 21st century systems," *IEEE Circuits Syst. Mag.*, vol. 8, no. 3, pp. 19–26, 2008.
[2] S. G. Samko, A. A. Kilbas, and O. I. Marichev, *Fractional Integrals and Derivatives: Theory and Applications*. Gordon and Breach, New York, 1993.
[3] R. Sikora and S. Pawłowski, "Fractional derivatives and the laws of electrical engineering," *COMPEL*, vol. 37, no. 4, pp. 1384–1391, 2018.
[4] R. Sikora and S. Pawłowski, "On certain aspects of application of fractional derivatives in the electromagnetism," *Przeglad Elektrotechniczny*, vol. 94, no. 1, pp. 101–104, 2018.
[5] K. J. Latawiec, R. Stanisławski, M. Łukaniszyn, W. Czuczwara, and M. Rydel, "Fractional-order modeling of electric circuits: modern empiricism vs. classical science," in *2017 Progress in Applied Electrical Engineering (PAEE)*, June 2017, pp. 1–4.

Simulation of Signal Propagation Along Fractional-Order Transmission Lines

Tomasz P. Stefański
Gdansk University of Technology
80-233 Gdansk, Poland
Email: tomasz.stefanski@pg.edu.pl

Damian Trofimowicz
SpaceForest Ltd.
81-451 Gdynia, Poland
Email: d.trofimowicz@gmail.com

Jacek Gulgowski
University of Gdansk
80-308 Gdansk, Poland
Email: jacek.gulgowski@mat.ug.edu.pl

Extended Abstract

The fractional-order (FO) modelling of transmission lines demonstrates advantages over classical approach for THz frequencies. The classical integer-order (IO) RLGC model allows for accurate modelling of transmission-line characteristics in a limited frequency range, because a conductor exhibits both frequency and spatial dispersion for high frequencies [1], [2]. Therefore, the dispersion and non-quasi-static effects cannot be accurately modelled by the classical model of the transmission line with IO elements. As a result, causality problems can appear in time-domain simulations employing the classical model. Fortunately, the FO RLGC model of the transmission line can describe these effects also in the THz frequency range and has already been successfully applied in engineering. In [1], [2], a causal and compact FO transmission-line model for THz frequencies is developed for CMOS on-chip conductor. For this model, a good agreement of the characteristic impedance is observed with measurements up to 110 GHz. However, the traditional IO model agrees with measurements only up to 10 GHz. These results clearly demonstrate advantages of the FO transmission-line modelling based on the time-fractional telegraph equations.

In mathematical literature, this type of equations has already been analysed. In [3]–[6], the time-fractional telegraph equation without the term linear in unknown function is considered with the use of both analytical and numerical methods on either bounded and unbounded domains. In [7], [8], the forcing term is introduced as well. The time-fractional telegraph equation with orders α and β of fractional differentiation ranging from zero to two is considered in [9], [10]. Furthermore, several numerical methods of simulation of the FO transmission lines have been recently proposed [11]–[14]. These methods are based on numerical computations of the inverse Laplace transformation. Significant analytical preprocessing on the complex s-plane is therefore required before these methods can be applied. Hence, we decided to propose the fast and efficient algorithm of the FO transmission-line simulation which is already successfully applied for simulations of the wave propagation in media described by FO models. It employs computations in the frequency domain, i.e., an analytical excitation is transformed to the frequency domain, multiplications with phase factors are executed, and finally the result is transformed back to the time domain. This algorithm involves elementary functions only and the fast Fourier transformation, hence, computations are numerically efficient and accurate. However, applicability of the method is limited by the sampling theorem. Numerical results are presented allowing for the evaluation of the method.

References

[1] Y. Shang, W. Fei, and H. Yu, "A fractional-order rlgc model for terahertz transmission line," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2013, pp. 1–3.
[2] Y. Shang, H. Yu, and W. Fei, "Design and analysis of cmos-based terahertz integrated circuits by causal fractional-order rlgc transmission line model," *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol. 3, no. 3, pp. 355–366, 2013.
[3] R. C. Cascaval, E. C. Eckstein, C. L. Frota, and J. A. Goldstein, "Fractional telegraph equations," *J. Math. Anal. Appl.*, vol. 276, no. 1, pp. 145–159, 2002.
[4] J. Chen, F. Liu, and V. Anh, "Analytical solution for the time-fractional telegraph equation by the method of separating variables," *J. Math. Anal. Appl.*, vol. 338, no. 2, pp. 1364–1377, 2008.
[5] S. Momani, "Analytic and approximate solutions of the space- and time-fractional telegraph equations," *Appl. Math. Comput.*, vol. 170, no. 2, pp. 1126–1134, 2005.
[6] E. Orsingher and L. Beghin, "Time-fractional telegraph equations and telegraph processes with brownian time," *Probab. Theory Relat. Fields*, vol. 128, no. 1, pp. 141–160, 2004.
[7] F. Huang, "Analytical solution for the time-fractional telegraph equation," *J. Appl. Math.*, p. 890158, 2009.
[8] W. Jiang and Y. Lin, "Representation of exact solution for the time-fractional telegraph equation in the reproducing kernel space," *Comm. Nonlinear Sci. Numer. Simulat.*, vol. 16, no. 9, pp. 3639–3645, 2011.
[9] T. M. Atanackovic, S. Pilipovic, and D. Zorica, "A diffusion wave equation with two fractional derivatives of different order," *J. Phys. A Math. Theor.*, vol. 40, no. 20, pp. 5319–5333, 2007.
[10] S.-q. Zhang, "Solution of semi-boundless mixed problem for time-fractional telegraph equation," *Acta Math. Appl. Sin.*, vol. 23, no. 4, pp. 611–618, 2007.
[11] S. M. Cvetićanin, D. Zorica, and M. R. Rapaić, "Generalized time-fractional telegrapher's equation in transmission line modeling," *Nonlinear Dyn.*, vol. 88, no. 2, pp. 1453–1472, 2017.
[12] S. M. Cvetićanin, D. Zorica, and M. R. Rapaić, "Frequency characteristics of two topologies representing fractional order transmission line model," *Circuits, Syst. Signal Process.*, vol. 39, no. 1, pp. 456–473, 2020.
[13] N. A. R-Smith, A. Kartci, and L. Brancik, "Fractional-order lossy transmission line with skin effect using nilt method," in *2017 40th International Conference on Telecommunications and Signal Processing (TSP)*, July 2017, pp. 730–734.
[14] L. Brancik, A. Kartci, and N. A. R-Smith, "Matlab simulation of transmission lines with skin effect via fractional telegraph equations and nilt," in *2017 27th EAEEIE Annual Conference (EAEEIE)*, June 2017, pp. 1–5.

Subband Structure and Ballistic Conductance of a Molybdenum Disulfide Nanoribbon in Topological 1T' Phase: A k·p Study

Viktor Sverdlov
Christian Doppler Laboratory
for Nonvolatile Magnetoresistive Memory and Logic
at the Insitute for Microelectronics
Technische Universität Wien
Vienna, Austria
sverdlov@iue.tuwien.ac.at

Al-Moatasem Bellah El-Sayed, Siegfried Selberherr
Institute for Microelectronics
Technische Universität Wien
Vienna, Austria
el-sayed@iue.tuwien.ac.at, Selberherr@TUWien.ac.at

Extended Abstract

Edge states in a sheet of MoS_2 in its 1T' phase, a two-dimensional topological insulator [1], propagate without backscattering, and are attractive for designing highly conductive transistor channels. The dispersion of edge states lies within an inverted gap of a topological insulator. By applying a vertical electric field E_z, the inverted gap can be reduced, closed, and opened again as a direct dielectric gap in the "bulk" of the sheet [1]. As no propagating edge states are allowed within the direct gap, the current is dramatically reduced [2].

In order to enhance the on-current through the channel it is beneficiary to have many edges by stacking several narrow nanoribbons. We evaluate the subband structure in a narrow nanoribbon of 1T' molybdenum disulfide by employing an effective **k·p** Hamiltonian [3], [4]. Highly conductive topologically protected edge states whose energies lie within the bulk band gap are investigated. Due to the interaction of the edge modes located at the opposite edges, a small gap in their linear spectrum opens in a narrow nanoribbon (Fig.1, circles)). This gap is shown to sharply increase with the perpendicular out-of-plane electric field, in contrast to the behavior in a wide nanoribbon. The gaps between the electron and hole bulk subbands (Fig.1, diamonds and squares) also increase with the electric field. The increase of the gaps between the subbands leads to a rapid decrease of the ballistic nanoribbon conductance and current with the electric field, which can be used for designing molybdenum disulfide nanoribbon-based current switches.

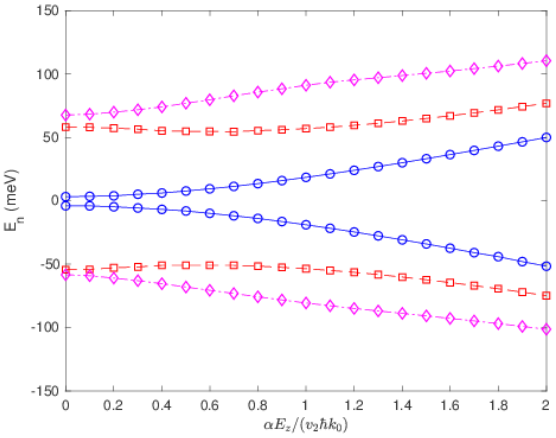


Fig. 1. Dependence of electron (hole) subbands minima (maxima) on the electric field E_z for the first three subbands. In contrast to the bulk case, the gap never closes and keeps increasing with E_z

The increasing gap between the edge-like subbands is reflected in the sharp decrease of the corresponding nanoribbon ballistic conductance shown in Fig.2 (diamonds). Although the edge-like subbands give the leading contribution in the conductance (Fig.2, circles) the role of other subbands shown in Fig.2 by squares is non-negligible. First two electron (hole) bulk-like subbands (Fig.1, diamonds and squares) give similar contributions to the ballistic conductance totaling to 30%. However, all contributions to the total conductance G rapidly decrease as a function of E_z (Fig.2). This makes 1T'-MoS_2 potentially suitable for switching applications.

Acknowledgment

Financial support by the Austrian Federal Ministry for Digital and Economic Affairs and the National Foundation for Research, Technology and Development is gratefully acknowledged.

References

[1] X. Qian et al., Science, vol. 346 (6215), p.1344, 2014.
[2] L. Liu and J. Guo, J.Appl.Phys., vol.118, 124502, 2015.
[3] V. Sverdlov et al., EUROSOI-ULIS 2020, accepted.
[4] V. Sverdlov and S. Selberherr, Phys.Rep., vol.585, p.1, 2015

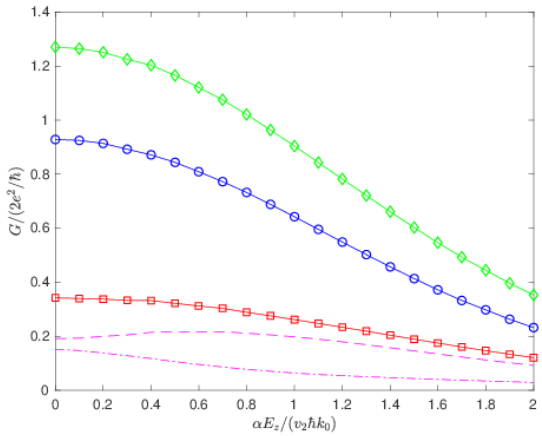


Fig. 2. Ballistic conductance (diamonds) of a 1T'-MoS_2 nanoribbon, with the contributions from the edge-like states (circles), and the remaining bulk-like subbands (squares). Dashed line from subbands shown in Fig.1 by squares; dot-dashed line- from Fig.1 by diamonds.

Microelectronics Technology and Packaging

Challenges in Performance Improvement of Silicon Systems on Chip in Advanced Nanoelectronics Technology Nodes

Arkadiusz Malinowski
Department of Integration and Yield
GLOBALFOUNDRIES
Dresden, Germany
arek.malinowski@globalfoundries.com

Shiv Kumar Mishra
Department of Product Integration
GLOBALFOUNDRIES
Malta, 12020 NY, USA

EXTENDED ABSTRACT

Microprocessor's performance is usually advertised by its maximum frequency (F_{max}) or clock rate i.e. 5 GHz. It means a number of simple operations per second (5 billion simple operations per second in this case). Obviously, the more operations per second, the faster and more efficient microprocessor is. And this is how personal computer (PC) era market was driven – it was all about speed and computing power for high performance (HP) applications. Speed or clock rate of the first microprocessor released to the market in 1971 was 740 kHz. This microprocessor was intended for calculator application. Continuing increase of microprocessor speed and computing power led to explosion of numerous applications. Five decades later microprocessors speed reached 5 GHz and they have enough computing power leading to such wonders as an artificial intelligence, virtual reality and self-driving autonomous cars which were before only in a science fiction domain. However, an increase of a chip speed is very challenging and it comes with a high price.

In the early CMOS technology era scaling and performance improvement were working hand in hand. Firstly, scaling of CMOS technology for following nodes was done by reducing gate length L_g and thinning gate oxide t_{ox} [1]. Later on the carrier mobility μ_n enhancement techniques came into play based on tensile and compressive stress liners as well as on introducing strained silicon (SiGe) in 90 nm technology [2]. Eventually the classical scaling started facing significant challenges and potential roadblocks. A problem became even more critical with the second wave of integrated circuit (IC) manufacturing revolution, namely low power (LP) mobile applications. Now, the power consumption has come into main play and has become the even more critical parameter. The low power chips including 5G and RF application for such devices as mobile phones, laptops, pads, and smartwatches are powered by batteries, therefore the power consumption determines how long those mobile devices can run on a battery. So, the chip behavior, namely its frequency as a function of the power consumption has become a key issue. Especially critical for battery lifetime is the current drawn in quiescent state, so called I_{ddq}. Correlating maximum frequency (F_{max}) with I_{ddq} leakage current is typical approach for the chip performance estimation.

The chip performance is determined by performances of the transistors and of the passive elements in the chip, e.g. parasitic resistances of the access regions and metallization lines at different levels and parasitic capacitances between semiconductor and metal areas. Therefore, improving the chip performance involves improving the transistor intrinsic performance. However, this task is so challenging that eventually such bold and revolutionary step as transistor architecture re-design was required for the first time in 40 years. Since 2011 the era of FinFET has started and dominated CMOS main stream manufacturing. Currently, in mainstream manufacturing are FinFETs with fin pitch 34 nm and gate pitch 54 nm [3]. This allows to stuff as much as 100 million transistors in 1 square millimeter which is unprecedented. Unlikely how it has been before such hyper scaling causes tremendous difficulties for FinFET performance improvement. These difficulties and challenges, which are described in this paper, may actually end the Moore's Law as well as era of microprocessor computing power improvement based on classical silicon technology [4].

REFERENCES

[1] Intel Technology Journal, Vol. 6, Issue 2, May 16, 2002 https://www.intel.com/content/dam/www/public/us/en/documents/research/2002-vol06-iss-2-intel-technology-journal.pdf

[2] T. Ghani et al., "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," IEEE International Electron Devices Meeting 2003, Washington, DC, USA, 2003, pp. 11.6.1-11.6.3.

[3] S. Narasimha et al., "A 7nm CMOS technology platform for mobile and high performance compute application", 2017 IEEE International Electron Devices Meeting (IEDM), DOI: 10.1109/IEDM.2017.8268476

[4] A. Malinowski, J. Chen, S. K. Mishra, S. Samavedam and D. Sohn, "What is Killing Moore's Law? Challenges in Advanced FinFET Technology Integration," 2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems", Rzeszów, Poland, 2019, pp. 46-51.

Recessed and P-GaN Regrowth Gate Development for Normally-off AlGaN/GaN HEMTs

Chaymaa Haloui[1,2], Gaëtan Toulon[3], Josiane Tasselli[1], Yvon Cordier[4], Éric Frayssinet[4], Karine Isoird[1], Frédéric Morancho[1], Mathieu Gavelle[2]
[1]LAAS-CNRS, Toulouse University, CNRS, UPS, Toulouse, France
[2]CEA Tech Occitanie, Toulouse, France
[3]EXAGAN, Toulouse, France
[4]CRHEA-CNRS, Valbonne, France
chaloui@laas.fr

***Abstract*— A new normally-off AlGaN/GaN HEMT structure is proposed. The regrowth of a P-GaN layer on the AlGaN/GaN heterostructure after the gate recess allows the achievement of the enhancement mode. A shift in the threshold voltage to positive values has been proved through simulation results. A precise control of the etch depth for the gate recess is detailed.**

***Keywords*—HEMT; normally-off; AlGaN/GaN; gate recess; RIE; P-GaN regrowth.**

I. Introduction

Thanks to their high breakdown voltage and ultrahigh power density operation, AlGaN/GaN HEMTs stand out as promising candidates for next-generation of high-speed switching devices. While most of the demonstrated AlGaN/GaN HEMTs are inherently normally-on with a negative gate threshold voltage, normally-off mode is strongly demanded to fulfill the requirements of power electronics applications; normally-off devices are inherently secure and suitable for energy converters requiring specifically high system reliability.

In this paper, a new structure of a normally-off AlGaN/GaN HEMT is presented. It combines two approaches: recessed and P-GaN regrowth gate (Fig. 1). The use of a P-GaN layer on the AlGaN/GaN heterostructure under the gate contact region lifts up the band diagram, which causes the depletion of the 2DEG channel, even in the absence of external bias. First, the simulated performance of the new device is described, then an overview of the technological process mandatory to realize such a device is proposed, with a particular focus on the gate recess step.

II. Results

The simulations have been performed with Sentaurus TCAD tools and carried out in two cases: metal on P-GaN (ohmic and Schottky contacts) and gate with insulator for different recess depth and P-GaN doping (Fig. 2). High threshold voltages can be achieved by reducing the thickness of the remaining AlGaN. With the ohmic contact, the threshold voltage is independent on P-GaN doping concentration, contrary to the Schottky one. With the gate insulator structure, the electrical performances depend on the type of insulator and thickness.

Among the realization steps of this device, a critically precise AlGaN etching is necessary. It was achieved by adjusting Cl_2-RIE etching parameters (Fig. 3). The roughness surface after etching was three times higher than the non-etched one but remains acceptable for a RIE mode. Some post-etch residues were found on the etched AlGaN surface and were removed by UV insolating and developing steps.

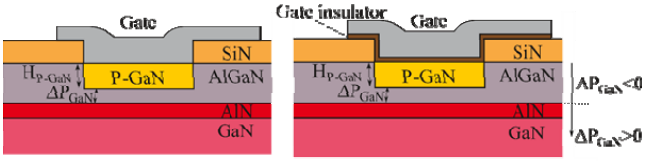


Fig. 1. Gate detail of the proposed structure with metal on P-GaN (left) and with gate insulator on top of P-GaN (right)

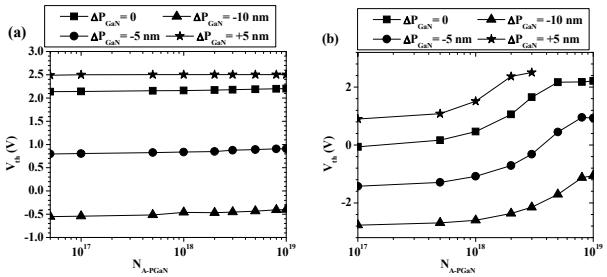


Fig. 2. Threshold voltage as a function of P-GaN doping concentration for different ΔP_{GaN} values when the gate contact is defined ohmic (a) and Schottky (b).

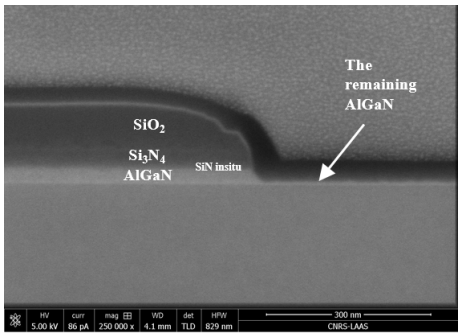


Fig. 3. Picture of FIB cut after the gate recess for RIE AlGaN etching of 35 s.

Testing and Reliability

A Human Immunity Inspired Intrusion Detection System to Search for Infections in an Operating System

Patryk Widulinski, Krzysztof Wawryn
Faculty of Electronics and Computer Science
Koszalin University of Technology
Koszalin, Poland
patryk.widulinski@tu.koszalin.plwawryn@tu.koszalin.pl

I. Introduction

During several decades, Intrusion Detection Systems (IDS) have been developed to protect computer software and computer networks from virus attacks. Many approaches to IDS based on Artificial Immune Systems (AIS) have been presented in the literature. Most of them are focused on anomaly intrusion detection systems and negative selection method to detect infections (anomalies) in the computer software.

In this article, we present an IDS devoted to detection of infections in an operating system. It is based on the negative selection algorithm consisting of two steps, receptor generation and anomaly detection. Receptors are generated randomly and receptors recognizing self patterns of the code sections are discarded. In this way, a set of receptors recognizing nonself patterns only, is created. These receptors are used to search for the infections in the operating system by the anomaly detection algorithm.

II. Our Solution

We propose an AIS-based system which may be used to detect irregularities within compiled computer programs. A diagram of the system is shown in Fig. 1.

The IDS monitors an area prone to infections in the operating system. The monitored area is called the safe container. The safe container houses programs the integrity of which is required.

A. Receptor generation

In order to detect anomalies within the program code, the IDS needs to construct a set with receptors. Receptors are binary strings of length l. If used within specific formulae, they have the ability to recognize nonself code patterns.

B. Anomaly detection

Proposed system detects anomalies in the code sections of programs in the safe container using receptors generated earlier, when the files were in a trusted state.

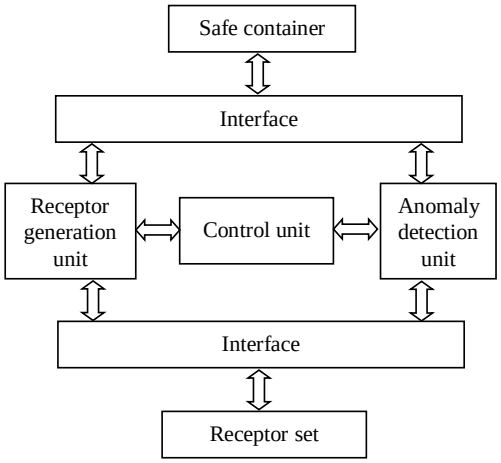


Fig. 1. A diagram of the proposed IDS.

III. Experimental results

Presented algorithms have been tested experimentally. A Windows implementation of the proposed IDS has been written in Microsoft Visual C# 2017. The implementation was tested on the Windows 7 64-bit operating system with an Intel i7-7700K CPU.

IV. Concluding Remarks

In the paper, an intrusion detection system to detect anomalies within an operating system was proposed. The algorithms in the proposed IDS are based on a negative selection algorithm inspired by the human immune system. The IDS detects anomalies within code sections of Win32 PE programs in a specific location on the hard drive. Proposed IDS has been implemented in C# language and tested on a computer running the Windows 7 operating system. During testing, the implemented solution successfully detected infected files. The research may continue with testing the IDS with files of greatly varying code section sizes.

The Application of NIR Spectrometer for Average Temperature Measurement in Optical Fibers Based on Spontaneous Raman Scattering for DTS Applications

Iyad S. M. Shatarah, Bogusław Więcek
Institute of Electronics
Lodz University of Technology
Lodz, Poland
iyad.safwat.shatarah@dokt.p.lodz.pl, boguslaw.wiecek@p.lodz.pl

EXTENDED ABSTRACT

Distributed optical fiber sensors (DOFS) have been implemented in several applications in the past decades. Nowadays DOFS are gaining more attention and are being applied in several new fields. The general principle of DOFS systems is the measurement of the changes along the optical fiber, which in this case is the actual sensor. DOFS systems are based on the measurement and analysis of Rayleigh, Brillouin and Raman scatterings phenomena. Fiber sensors can detect temperature changes, strain and cracks, fire and oil leakage. Distributed temperature sensing (DTS) systems are the type of DOFS systems that is used for temperature measurement.
Light injected in optical fibers scatters in every direction. Backscattered light is often studied in order to obtain information about changes along the optical fiber. A pulse laser with known power and pulse width is used in the optical time domain reflectometry (OTDR) based system, whereas a continuous wave laser is used in the optical frequency domain reflectometry (OFDR) based systems, with a tunable function generator or frequency modulator to set the source frequency. The receiver can be a photodiode (usually an avalanche photodiode), spectrum analyzer or spectrometer. DOFS systems are commonly developed in single – ended, double – ended and loop configurations.

Depending on the wavelength of the scattered light, there are three types of light scattering: Rayleigh, Brillouin and Raman scatterings. DTS systems measure the intensity of Raman Anti-Stokes in order to determine temperature changes due to its high dependency on temperature.

This paper presents the set-up of the DTS system used in the measurements. The laser diode used in this setup has the optical power of 20 mW, and it's operating wavelength is 1550 nm in order to achieve long distance measurements. The backscattered light is typically filtered into Rayleigh, Raman Stokes and Raman Anti-Stokes by using WDM filters. Alternatively, in the set-up presented in this research, the spectrometer NIRQUEST256-2.5 was used in order to observe the backscattered light. The implementation of the spectrometer allows the elimination of WDM filter. Backscattered Rayleigh radiation has a very high intensity and covers a larger range of the wavelength spectrum than theoretically should be, thus WDM filters in most cases are not able to precisely filter the backscattered radiation to pure Raman Stokes and Anti-Stokes components, which leads to incorrect measurements. The author's MATLAB calculation script help avoiding the inability of the WDM filter through choosing the desired range for each the backscattered radiation.

Two sets of measurements were carried out: the first set was for a DTS system with WDM filter implemented in the system, while the second set was for a DTS system without the implementation of the WDM filters. The temperature of the optical fiber was changed and controlled by heating chamber. The author's MATLAB calculation script finds the Raman Anti-Stokes to Raman Stokes ratio in order to obtain much reliable results of temperature impact on the Raman Anti-Stokes intensity. The optical fiber used in this DTS system's experiments is a 1000 m single-mode SMF-28e bare fiber. Preliminary measurements for a 100 m loose tube single-mode fiber have been realized in order to verify the DTS system operation with different optical fiber types.

The DTS system presented in this paper allows obtaining reliable results regarding the impact of temperature on Raman Anti-Stokes intensity. The results presented in this paper show the impact of temperature over two different types of optical fibers: bare optical fiber and loose tube optical fiber. Both optical fibers are single-mode (SMF28-e), however the construction, isolation and protection layers are different, thus the impact of temperature on them is different. This system also helps reducing the costs and the ability to work without a WDM filter. The author's calculation script improves the potentials of achieving more reliable results.

A series of further experiments are planned to be held. Several types of optical fibers will be tested. Moreover, experiments will be extended through the implementation of photodiodes as a receiver for the DTS system. Model, alongside results will soon be published.

Power Electronics

1MHz Gate Driver in Power Technology for Fast Switching Applications

Roberto Di Lorenzo, Andrea Baschirotto
Physics Department "G.Occhialini"
University of Milan - Bicocca
Milan, Italy
r.dilorenzo3@campus.unimib.it

Albino Pidutti, Paolo Del Croce
IFAT DC ATV BP PD ADL
Infineon Technologies
Villach, Austria
Albino.Pidutti@infineon.com

***Abstract*—The demand for low-cost integrated circuits for automotive applications is increasing, while their cost must remain low to maintain product competitiveness. In this scenario, to guarantee DC-DC Buck converters high-efficiency and low cost (in terms of external components) increasing switching frequency is mandatory. The main problems are inherent the parasitic inductances and the parasitic capacitance of power MOSFET. This paper deals with the main critical aspects of increasing such switching frequency and show how to replace the external Schottky Diode with an integrated structure. The case of a high-speed monolithic integrated circuit to control a load current is here proposed. Proper design allows to achieve switching frequency up to 1MHz with 94.4% efficiency.**

***Keywords*—gate driver, DC/DC converter, Buck**

SUMMARY

In this work, all the aspects that arise in the design of a gate driver have been taken into consideration. Among the various aspects to be taken into consideration are the losses due to switching, due to the joule effect, and the speed with which the external capacity is recharged. The gate driver has a wide operating range, with a duty cycle that can vary by 90%.

Fig. 1 shows the main blocks for this paper. Each block must be optimized to avoid the bottleneck, the maximum switching frequency depends not only on the integrated circuit, but also on the parasitic external inductances.

Fig. 2 shows the main contribution that affects the overall efficiency of the system. The power transistor together with the driver require particular attention in order to obtain maximum efficiency up to 94.4%.

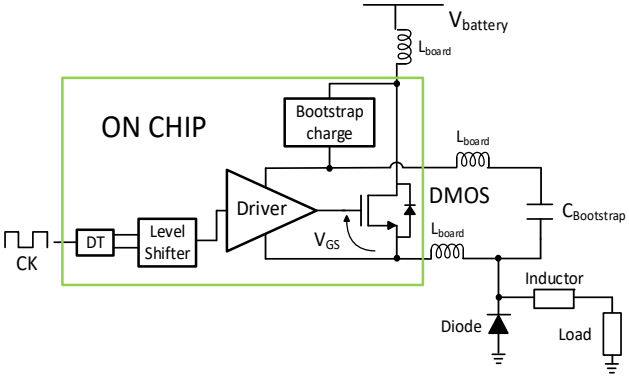


Fig. 1. Block diagram of gate driver

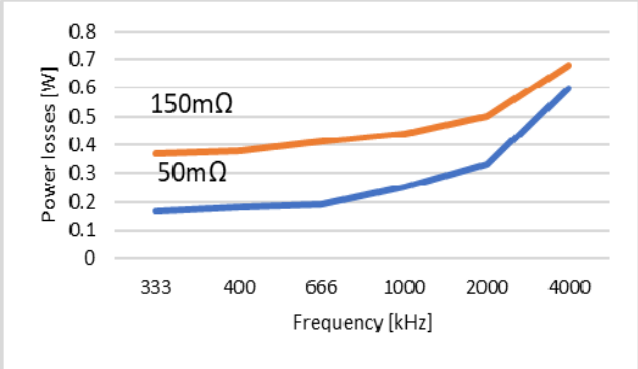


Fig. 2. Power losses on power switch

In the last part of the article the results of the designed device will be presented and will be compared with the products currently on sale on the market.

An Influence of the Operation Mode of a LED Lamp of the HUE Type on Its Electrical and Optical Parameters

Przemysław Ptak, Krzysztof Górecki
Department of Marine Electronics
Gdynia Maritime University, Gdynia, Poland
k.gorecki@we.umg.edu.pl, p.ptak@we.umg.edu.pl

Jakub Heleniak
Faculty of Electrical Engineering
Gdynia Maritime University, Gdynia, Poland
kuba.97-1997@o2.pl

EXTENDED ABSTRACT

Solid-state light sources are commonly used in lighting technique. Both LED lamps emitting white light (lighting of rooms) and LED lamps emitting light of the fixed colour (accent lighting, backlight) are used. LED lamps consist of three components: LED modules emitting light, feeders and the case with a heat-sink.

The important aim in lighting systems is to obtain a desirable colour of the emitted light and its illuminance. Classical LED lamps do not show such functionality and the mentioned above parameters are fixed in the stage of production of these lamps. On the other hand, from the literature it is known that illuminance emitted by power LEDs can be easily regulated by changing the value of current feeding these diodes, and the colour of the emitted light can be regulated using RGB diodes and regulating the value of current flowing through each diode.

Development of solid-state light sources and systems of intelligent lighting of buildings resulted in production of wireless controlled LED lamps which operate using mobile devices. This control is realised with the use of radio waves and such systems as Bluetooth, Wi-Fi or ZigBee. The radio signal is transmitted between the controller and the lamp contains the address of the lamp and the required parameters describing illuminance and the colour of the emitted light.

One of the main advantages of LED lamps is high luminous efficiency which causes that these lamps are characterised by low consumption of electrical energy. Unfortunately, quality of these feeders typically included in such lamps is low and they cause essential noise of current received from the electroenergy network, which can lead to worsening of coefficients characterising quality of electrical energy. To these coefficients belong e.g.: total harmonic distortion THD and the power factor PF.

Philips is one of the main producers of wireless controlled LED lamps, offering among other things LED lamps of the type HUE. The first lamps belonging to this group were introduced to the market in October 2012. They make possible among other things, a change of colour of the emitted light. At present, three generations of HUE lamps are accessible on the market. Such lamps are fully compatible with one othe.

In the paper experimental findings illustrating properties of electrical and optical LED lamps of the type HUE emitting light of selected colours are presented. A manner of regulating useful parameters of the considered lamp is presented and characteristics illustrating relation between values of the fixed optical parameters and the measured values of the emitted luminous flux and spectral characteristics of the examined lamp are shown.

Attention was paid to properties of the system feeding lighting elements of the examined lamp. Influence of both: feeding voltage and colour of the emitted light and illuminance of the lamp on the efficient value of current of the power supply, its waveform, the coefficient of the total harmonic distortion and the power factor is discussed.

Measurements were performed with the use of the authors' measuring set-up. Measurements of the RMS value of the feeding current show that it is an increasing function of the fixed value of illuminance and a decreasing function of feeding voltage. Waveforms of feeding current registered during experimental research confirm strong deformation and they can constitute a proof that in the feeding system a block of the power factor correction was not applied. The performed measurements and calculations of the coefficients THD and PF also show that the examined lamp unfavourably influences quality of energy in the electroenergy network. It is proper to pay attention that values of parameters THD and PF obtained by means of the power analyser accept far less favourable values than in the case of using oscilloscopic measurements and simplified analytic formulas given in the literature. The observed differences result probably from the fact that the waveband, wherein harmonics values of feeding current are measured, is considerably wider in the case of the power analyser. When the oscilloscope is used, fast Fourier transformation taking into account only about 20 harmonics frequencies of the network is realised. Therefore, disturbances of frequency higher than 1 kHz were not taken into account while determining the THD value.

Findings presented in this paper can be useful for designers of lighting systems with LED lamps. It is also proper to take into account in investigations influence of electronic devices on the electroenergy network to make allowance for harmonics of higher order which correspond to current impulses connected with the use of switch-mode power supplies of LED lamps. The objective of further investigations will be a proposal of systemic solutions making it possible to determine the THD and an increase of the PF value characterising waveforms of feeding current of the examined LED lamps.

Signal Processing

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Combining ε-similar Fuzzy Rules for Efficient Classification of Cardiotocographic Signals

Michal Jezewski[1], Robert Czabanski[1], Jacek M. Leski[1], Adam Matonia[2], Radek Martinek[3]
[1]Department of Cybernetics, Nanotechnology and Data Processing
Silesian University of Technology, Gliwice, Poland
[2]Łukasiewicz Research Network – Institute of Medical Technology and Equipment, Zabrze, Poland
[3]VSB – Technical University of Ostrava, Ostrava, Czech Republic
Emails: mjezewski@polsl.pl, rczabanski@polsl.pl, jleski@polsl.pl, adamm@itam.zabrze.pl, radek.martinek@vsb.cz

I. Introduction

CardioTocoGraphic (CTG) monitoring, involving the analysis of fetal heart rate and uterine contractions, is a widely used method to assess fetal state. The visual evaluation of the signals by clinicians is characterized by inter- and intra-observer disagreement, therefore a well-established approach is the automated classification of CTG signals. In case of medical diagnosis support, a very important feature of the classifier is its interpretability, which is ensured by fuzzy rule-based classifiers. However, the extracted rule base may include redundant rules, which reduce interpretability and increase the rule base complexity.

The aim of this study is to introduce a rule base simplification method which is based on ε-insensitive distance between rule premises. The goal is to achieve efficient classification of CTG signals to support assessment of fetal condition using fewer classifier rules. The premises of the initial (not simplified) rule base were found using clustering with pairs of ε-hyperballs procedure ($\mathrm{CPP}^{\varepsilon}_{\mathrm{ST}}$).

II. Rule Base Simplification

The proposed algorithm for simplification of the rule base consists in reducing its size by combining ε_S-similar rules into so-called representative rules. Two rules ith and jth are considered ε_S-similar, if they indicate the same class of objects (have conclusions $y^{(i)}, y^{(j)}$ of the same sign), and the distances between their centers v_{in}, v_{jn} of all N Gaussian functions do not exceed the assumed value of ε_S

$$\underset{\substack{1\le n\le N\\ i\neq j,\ y^{(i)}y^{(j)}>0}}{\forall} \left|v_{in}-v_{jn}\right| \le \varepsilon_S. \tag{1}$$

In the algorithm, the ε_S-similarity is checked for all possible pairs of rules and the ε_S-similar rules are combined into groups. Each group is then represented by the"strongest" (representative) rule. The "strength" of the rule is determined based on its conclusion and activation levels. The algorithm is run separately for both indicated classes.

III. Experiments and Results

A two-stage classification was carried out based on two component classifiers. CTU-UHB benchmark dataset of CTG signals was used in the experiments. Measurement of blood pH in the neonatal umbilical artery was adopted as a reference signal evaluation.

Table I compares the achieved classification performance with the results obtained when using the full (not simplified) rule base (pH threshold set to 7.15). We can conclude that the proposed rule simplification method is beneficial as providing a higher classification quality QI, which was defined as a geometric mean of classification sensitivity (Se) and specificity (Sp). Moreover, the increase in QI is accompanied by a significant increase of Se, which is of particular importance in medical applications. Moreover, the results were obtained with a smaller number of rules (R_1 and R_2) of both component classifiers (in total on average 49.56, compared to 78.00).

TABLE I
Comparison of the rule base simplification ($\mathrm{CPP}^{\varepsilon}_{\mathrm{ST}}$+RBS) with the results obtained using the full rule base ($\mathrm{CPP}^{\varepsilon}_{\mathrm{ST}}$)

	$\mathrm{CPP}^{\varepsilon}_{\mathrm{ST}}$ + RBS	$\mathrm{CPP}^{\varepsilon}_{\mathrm{ST}}$
QI=$\sqrt{\mathrm{Se}*\mathrm{Sp}}$	74.06 (3.28)*)	72.30 (3.84)
Sensitivity (Se)	65.33 (6.08)	57.91 (6.52)
Specificity (Sp)	84.23 (3.82)	90.61 (2.50)
R_1	16.70 (0.84)	40
R_2	32.86 (0.87)	38

*) mean value (std. dev.), #) no. of rules of the first (R_1) and the second (R_2) component classifiers

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Fusion of Position Adjustment from Vision System and Wheels Odometry for Mobile Robot in Autonomous Driving

Jarosław Zwierzchowski*, Dawid Pietrala†, Jan Napieralski*
* Department of Microelectronics and Computer Science, Lodz University of Technology
Wolczanska 221/223, 90-924 Lodz, Poland
† Department of Automation and Robotics, Kielce University of Technology
Al. 1000-lecia P.P. 7, 25-314 Kielce, Poland
Emails: jzwie@dmcs.pl, dpietrala@tu.kielce.pl, jnapier@dmcs.pl

***Abstract*—Autonomous mobile vehicles need advanced systems to determine their exact position in a certain coordinate system. For this purpose, the GPS and the vision system are the most often used. These systems have some disadvantages, and so the GPS signal is unavailable in rooms and may be inaccurate, while the vision system is strongly dependent on the intensity of the recorded light. This work presents a system for determining the position of the robot base on information about the distance travelled coming from each vehicle wheel and the IMU sensor. However, wheels odometry introduces an additive measurement error (rise in every measure cycle). In this work there has been a vision correction system applied, where corrections are calculated by measuring the distance to artificial markers. This system precisely determines such correction. Each of these systems is described in the paper, in particular the vision system. There is also a description of a fusion algorithm of wheels odometry and vision correction system. The presented system was tested on an artificially built test track.**

***Keywords*—autonomous driving, artag, odometry, signals fusion.**

Extended Abstract

The article describes the implementation of algorithms to determine the position and orientation of the mobile robot in a certain coordinate system without the participation of the GPS positioning system. Authors divided described task into two subsystems constantly sending messages to each other via UART bus. The first subsystem consists of programs located in the robot control system and determines the robot's trajectory calculated from vehicle wheels. This is called wheels odometry and it is widely used in the automotive industry. A general discussion of this solution has been described in [1], [2]. Currently, designers of modern solutions to increase the accuracy of determined robot position, very common are using a combination of many independent positioning systems. Therefore, the authors added a second subsystem, that was a vision system. In the literature, a vision system with an implemented SLAM algorithm is the most often described [3]. In this article, the vision system only provided position corrections, and was geared toward finding characteristic landmarks. The problem with landmarks was studied in the paper [5].

To check the correctness of the implemented subsystems, a mobile robot was designed and built. What is more, many tests were performed on the test track. This track was accurately measured and a map was made based on these measurements. Control points and position of graphic markers - ARTags were marked on the map. The experiment assumed that the robot autonomously was able to move from the starting point to the next and subsequent checkpoints with the greatest accuracy. Besides if the robot calculated that a checkpoint was reached the blue lamp mounted on its board stated to flash.

By design, numbers from 0 to 16 are encoded in ARTags. To accurately determine the position of the robot, the vision system needed to recognize three markers. While if two markers had been detected, two robot positions were determined, fortunately one of which could be easily rejected. If one marker was detected, the robot could be located with some accuracy, one was positioned on the circle indicated by the distance between the robot and the marker. To calculate the distance to the markers, a specially designed head with two cameras set under a 20-degree account was used.

The software that interpreted the robot's space was initially tested on a laptop with an Intel Core i7 processor and 32 GB RAM, which at 1024x760 resolution allowed to run the ARTag recognition algorithm at 15 frames per second. The vision system communicated with the robot's main processor via a serial bus and transmitted the numbers of founded markers and the distances to them. Information from the wheel odometry was also transmitted to the main processor. Ultimately, the important step of the whole task was to combine the subsystems described above into one decision-making robot control system, i.e. calculating signals fusion. Tests for the accuracy and speed of vision system were described in [4].

All algorithms regarded to wheels odometry were implemented in C language and are flashed in STM processor. The vision system was written in C++ language.

The article contains many images and descriptions like general block overview of the system, test track experiment, mobile vehicle autonomous drive and others.

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Marker Detection Algorithm for the Navigation of a Mobile Robot

Anna Annusewicz
Kielce University of Technology
Aleja Tysiaclecia Panstwa Polskiego 7, 25-314 Kielce, Poland
Email: aannusewicz@tu.kielce.pl

Jarosław Zwierzchowski
Lodz University of Technology
ul. Żeromskiego 116, 90-924 Łódź, Poland
Email: jzwie@dmcs.pl

I. Vision System

The navigation of mobile robots plays an important role in autonomous movement tasks. This article discusses a vision system for recognizing fiducial markers to autonomous navigate a mobile robot. The vision system was developed for the mobile robot shown in Fig. 1. Its function is to enable accurate robot navigation without using a GPS signal. The position of the robot in space is determined by encoders. The location of the markers in the robot space is known; thus, the recognition of appropriate markers allows for precise navigation of the robot. Using only the odometry method could cause measurement errors resulting, e.g., from wheel slips. The vision system consists of two Logitech HD Pro Webcam C920 cameras and a Nvidia Jetson TX2 module performing digital image processing operations. Cameras are mounted on the sides of the robot in such a way that their frames do not overlap. Fiducial markers of the ARTag type were used to navigate the mobile robot. The vision system was designed to detect markers, recognize their indexes and determine the position of the robot relative to the ARTags.

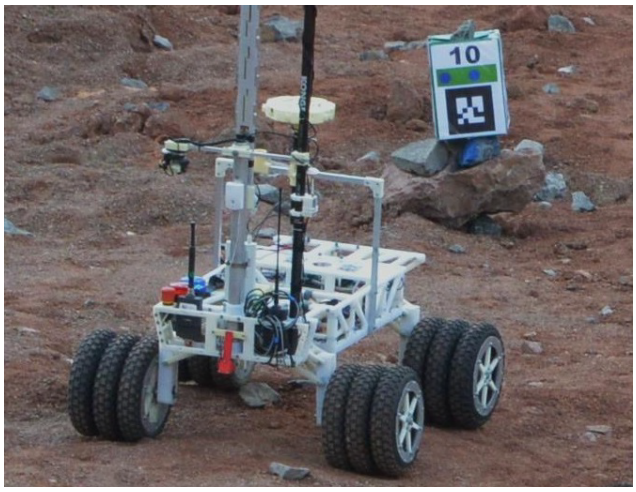


Fig. 1. The mobile robot for which the vision system was developed at a test site.

A. Algorithm for recognizing graphic markers

The algorithm discussed here uses the marker recognition method presented in [1,2]. The algorithm was implemented on the Nvidia module in C++ language using OpenCV and QT libraries. The application performs image processing operations for the two cameras and sends information to the main robot control system using a serial port. The algorithm works in real time and analyzes subsequent frames from both cameras in order to find markers.

II. Analysis of the Vision System Operation

The marker detection algorithm was tested for various camera resolution settings. The tests were carried out for Full HD resolution (1920x1080) and 1024x576. All the detection tests were performed on a marker with 142 mm long side. The calculated distance between the marker and the camera was compared with the distance measured using a measuring tape with an accuracy of 1 mm, which was treated as a reference measurement. The use of higher resolution allowed us to increase the distance to over 5 m (from which the marker could be recognized), while in the low resolution case the maximum distance was over 4 m. The absolute measurement error increased with distance.

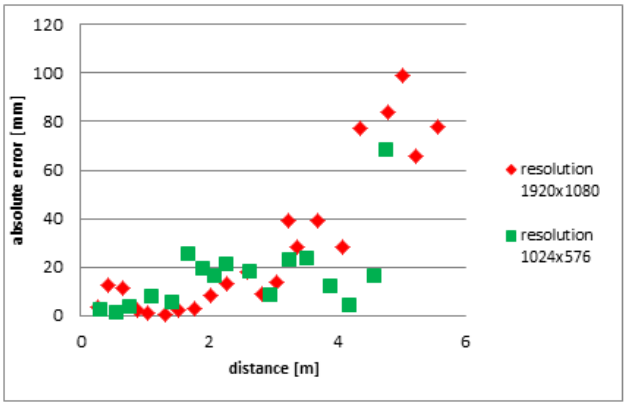


Fig. 2. Absolute error versus the distance between the camera and the marker for measurements performed by the vision system for different resolutions

References

[1] S. Garrido-Jurado, R. Mu˜noz-Salinas, , F.J. Madrid-Cuevas, and M.J. Marin-Jimenez, *Automatic generation and detection of highly reliable fiducial markers under occlusion*, in Pattern Recognition, vol. 47, pp. 2280 - 2292, 2014.

[2] Y. Kim, S. H. Yang, K. W. Yang and N. G. Dagalakis, *Design of MEMS vision tracking system based on a micro fiducial marker*, in Sensors and Actuators A: Physical, vol. 234, pp. 48 - 56, 2015.

Book of Abstracts of the 27th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 25-27, 2020, Łod , Poland

Modified Particle Swarm Optimization Algorithm Facilitating Its Hardware Implementation

Michal Rajewski, Zofia Długosz, Rafal Dlugosz, Tomasz Talaska
UTP University of Science and Technology
Faculty of Telecommunication, Computer Science
and Electrical Engineering
Kaliskiego 7, 85-796
Bydgoszcz, Poland
Email: michalrajon@gmail.com, zosia.dlugosz@gmail.com, rafal.dlugosz@gmail.com, talaska@utp.edu.pl

***Abstract*—This paper presents various modifications and developments in the PSO algorithm. PSO is an algorithm based on the behavior of swarms. In this work we focus mainly on simplifying the algorithm by replacing random number generators, which can be a problem when implementing algorithms in hardware. We investigate how changing the methods for algorithm updates from random to more deterministic approach influences the results. This paper shows whether it is possible to achieve same as random or better results using a simplified algorithm, which uses simple mathematical operations in the algorithm optimization process.**

***Keywords*—Particle Swarm Optimization; Optimization; Deterministic methods; Hardware implementation issues;**

I. Introduction

The PSO algorithm has been a well-known and widely used algorithm for many years, especially useful when searching for the function optimum. The algorithm is modeled on the behavior of clusters of animals such as ants or bees. It consists of searching the "area" of functions by many so-called agents who try to get to the extremum. The strength of the algorithm is the cooperation of agents with each other and them sharing experience regarding existing discoveries. Each agent is based on the knowledge acquired during exploration, taking into account the best value achieved, but also shares its knowledge with the swarm. The algorithm is especially useful when the searched function has many extrema, because in such situation searching the area by only one unit would not bring the desired results, limiting the effect of the operation to finding a local extremum, not a global one.

The way the agents move is similar to how animals move in nature, but there are also some differences. The space in which the agents move is fully abstract, and the movement of individuals is only a simplified mathematical description of what can be found in reality.

Every particle in the swarm is characterized by the following variables:

- position – position of the particle in space,
- velocity – speed at which the particle moves,
- local best – position of found personal local optimum,
- global best – position of current found global optimum.

An important parameter of each particle, which also describes local best and global best, is the fitness function (FF) output value. It determines how far the unit is from the target function optimum.

In the original version of the algorithm, both the initial position and the weight values, by which the position is updated in subsequent iterations, are random values. In this work, the goal was to simplify the algorithm and explore alternative ways to update the algorithm parameters. The scope of work included the analysis of updating units in a more orderly and deterministic manner, i.e. eliminating the element of randomness in the algorithm. Elimination of randomness is also an extremely important issue in the case of hardware implementation, because the hardware implementation of the randomization block is computationally expensive.

The first phase of the PSO algorithm is the initialization of the positions of particular particles in the swarm, X, and their velocities, V. In the conventional approach, the initial values of X parameters are selected randomly.

From the hardware implementation point of view, the drawing operation of the X and the V vectors is relatively complex. For this reason, in our works we investigated various ways of the initialization and their impact on the effectiveness of the optimization process of the swarm.

Another complex operation in the original PSO algorithm is the modification of particle velocity, which is responsible for their movement. In this work we present some modifications of the way how the velocities of particular particles are computed during the optimization process of the swarm. They lead to a simplification of the PSO algorithm when it comes to the hardware implementation. They also allow to increase a control over the changes occurring in subsequent iterations of the optimization process.

One of the main objectives of the carried out investigations is transistor level implementation of the PSO algorithm. For this reason, in the proposed solutions we try to eliminate the randomness of some coefficient appearing in the original algorithm.

The proposed modifications of the conventional PSO algorithm are presented further in the article. The behavior of particular modified versions was verified for three selected functions: the Sphere, Rosenbrock and the Griewank ones, which all offer different complexities.

Testing Stability of Digital Filters Using Multimodal Particle Swarm Optimization with Phase Analysis

Damian Trofimowicz
SpaceForest Ltd.
81-451 Gdynia, Poland
Email: d.trofimowicz@gmail.com

Tomasz P. Stefański
Gdansk University of Technology
80-233 Gdansk, Poland
Email: tomasz.stefanski@pg.edu.pl

Extended Abstract

The stability analysis is an important topic in almost every area of engineering. Most of electronic circuits must be stable to properly operate and execute tasks for which they are designed. It is also vitally important in the digital signal processing. In general, the discrete-time linear time-invariant system is (asymptotically) stable if and only if all zeros of the characteristic equation ($f(z) = 0$) are within the unit circle at the complex z-plane [1]. The direct approach is to find all zeros of the charateristic equation (e.g., a denominator of a transfer function). However, it might be a difficult task because for some systems, e.g., of fractional order [2], the characteristic equation may not be based on a polynomial. Furthermore, the search space for zeros of the characteristic equation of the system is outside the unit circle ($|z| > 1$), hence, it is infinite.

We have already proposed numerical tests [3], [4] allowing for evaluation of the system stability by employing modern techniques of global root finding based on Delaunay's triangulation and discrete Cauchy's argument principle (DCAP). The motivation behind this work is to benchmark a novel stability test based on the multimodal particle swarm optimization with phase analysis (MPSO-WPA) targeting discrete-time systems, especially digital filters. Its main advantage over other methods relies on stochastic space exploration by subsequent swarms, hence, the probability of detection of all zeros is increasing each time swarm positions are updated. The MPSO-WPA method is very general because it allows one to evaluate stability of systems whose characteristic equations are not based on polynomials. The method combines an efficient evolutionary algorithm represented by the particle swarm optimization and the phase analysis of a complex function in the characteristic equation. The method generates randomly distributed particles (i.e., a swarm) within the unit circle on the complex plane and extracts the function phase quadrants in position of each particle. By determining the function phase quadrants, regions of immediate vicinity of unstable zeros, called candidate regions, are detected. In these regions, both real and imaginary parts of the complex function change signs. Then, the candidate regions are explored by subsequently generated swarms. When sizes of the candidate regions are reduced to a value of assumed accuracy, then the occurrence of unstable zero is verified with the use of DCAP. The algorithm is evaluated in four benchmarks for integer- and fractional-order digital filters and systems. The numerical results show that the algorithm is able to evaluate the stability of digital filters very fast even with a small number of particles in subsequent swarms. Furthermore, the proposed method is based on the phase analysis, hence, it is not sensitive to numerical precision issues resulting from the overflow of arithmetic operations. However, MPSO-WPA may not be computationally efficient in stability tests of systems with complicated phase portraits.

To demonstrate efficiency of the developed method, let us consider the fractional-order digital filter, which is represented in the Z-transform domain by the transfer function

$$H(z) = \frac{1}{(\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}})^{\alpha+\beta} + a(\frac{1-z^{-1}}{1+z^{-1}})^{\alpha} + c} \qquad (1)$$

where a and c are the design parameters, α and β are the fractional-order parameters and T is the sampling period. The filter characteristic equation in the w-domain ($w = z^{-1}$) is given by

$$F(w) = s^{(\alpha+\beta)} + as^{\alpha} + c \qquad \text{and} \qquad s = \frac{2(1-w)}{T(1+w)}. \quad (2)$$

The function is tested for $\alpha = \beta = 0.5$, $a = 1$, $c = -1000 + 50j$ and $T = 0.001$. A single zero is found inside the unit circle, i.e., $w = 0.346947 + 0.022324j$. This stability test lasts about 0.16 second for the accuracy set to $\varepsilon = 10^{-5}$. The algorithm executes 9 iterations and generates 600 particles in total. The filter is unstable because zero is found inside the unit circle on the complex w-plane.

References

[1] E. I. Jury, *Theory and Application of the Z-Transform Method*. John Wiley and Sons, 1964.

[2] R. Stanislawski and K. Latawiec, "Stability analysis for discrete-time fractional-order lti state-space systems. part i: New necessary and sufficient conditions for the asymptotic stability," *Bull. Pol. Ac.: Tech.*, vol. 61, pp. 353–361, 2013.

[3] L. Grzymkowski and T. P. Stefanski, "Numerical test for stability evaluation of discrete-time systems," in *2018 23rd International Conference on Methods Models in Automation Robotics (MMAR)*, Aug 2018, pp. 803–808.

[4] L. Grzymkowski and T. P. Stefanski, "A new approach to stability evaluation of digital filters," in *2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES)*, June 2018, pp. 351–354.

Embedded Systems

A Database Proposal for an Application Involving Industrial Networks for Industry 4.0 Concepts

Alexandre Baratella Lugli[1], Egidio Raimundo Neto[1], João Paulo Carvalho Henriques[1], Maria Teresa de Carvalho Silva[1], Nayara Dias Pereira[1], Tales Cleber Pimenta[2]

[1] Department of Industrial Automation
National Institute of Telecommunications (INATEL)
CEP , 37.540-000, Santa Rita do Sapucaí, MG, Brazil

[2] Institute of Engineering System and Information Technology
Federal University of Itajubá (UNIFEI)
CEP 37.500-903, Itajubá, MG, Brazil

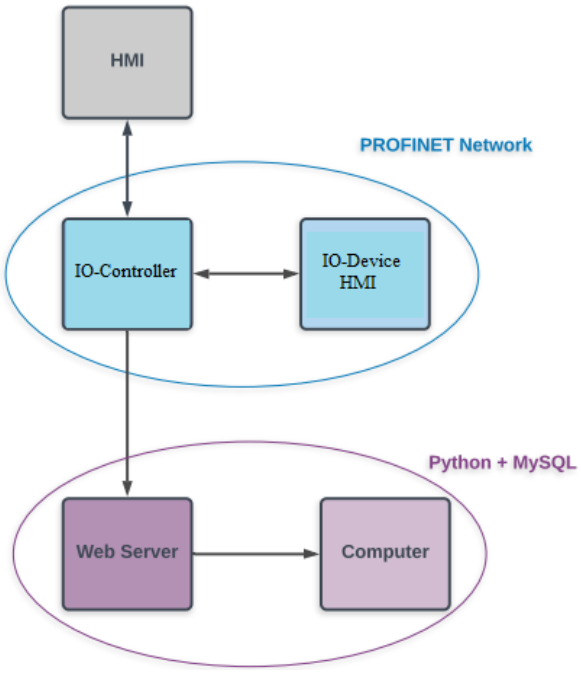
baratella@inatel.br, egidio.neto@inatel.br, joao.paulo@inatel.br, mariateresa@gea.inatel.br, nayaradias@gea.inatel.br
tales@unifei.edu.br

ABSTRACT

This paper proposes to develop an application with the PROFINET network applied in the context of the Industry 4.0. The proposal consists in collect data of an industry application, such as temperature and motor status, for instance, and then, by a tool developed in Python programming language, it is possible to monitor and control the magnitudes of the industrial process. The developed Database was used to monitor the variables in a PROFINET industrial network application.

The purpose of this paper is to develop an application of this communication protocol, where industrial field elements will be able to access information stored in a database. Such application will be built especially for interaction between the PROFINET industrial communication network and the information technology network (IT), in real-time, being able to store the information of the industrial processes, accessed remotely and at any time.

Figure illustrates the general block diagram of the practical application developed in this paper. The program application to store the data was developed in Python language (*PyCharm*) that it stores the information collected through the PROFINET network.



Block diagram of the general project.

Consistency Preserving Development of Embedded Systems Using AADL

Tomasz Szmuc, Wojciech Szmuc
Department of Applied Computer Science
AGH University of Science and Technology
30-059 Kraków, Poland
tsz@agh.edu.pl, wszmuc@agh.edu.pl

EXTENDED ABSTRACT

Embedded systems are hardly depended on their environment, therefore multi-domain modeling is recommended to preserve consistency of application and reduce testing effort in the later phases of the development process. Software of embedded systems is deeply involved in hardware, hence design of software modules should even consider hardware features. Embedded systems in control domain should also care on dynamics of the control object and also time characteristics of sensors, actuators and other devices in the environment.

The necessity of the multi-domain approach is especially visible in the Cyber Physical Systems (CPS) domain. Architecture of these systems is often complicated structure which consists of microcontrolers, networks of sensors (IoT) and usually collections of data stored in nebula or cloud structure. Robot controllers, intelligent cars are other examples of the multi-domain approach. Correctness requirements (logics, time-response, safety, etc.) of Safety-Critical Systems magnifies the need for consistency preserving of modeling during the development.

SysML and AADL (Architecture Analysis and Design Language) are two main languages recommended for development of embedded systems. SysML is an extension of UML profile which adapts this language to embedded applications by additional diagrams: requirement, parametric, block definition and internal block diagrams. Requirement and parametric diagrams support consistency of developed models, while block definition and internal block diagrams are simpler and more precise than general class/object diagrams in UML. The total number of diagrams in SysML is also reduced. Besides these adaptations and extensions, SysML seems to be to heavy for modeling of embedded systems perhaps because of heritage from "baroque" UML. It should be mentioned, however, that SysML is the most popular modeling language in the embedded world. AADL background is quite different. The language was built from scratch but basing on experience in development of real-time and embedded systems. The main AADL building constructs are **process**, **thread**, **subprogram** and **data** for software, and **device**, **processor**, **memory** and **bus** for hardware. The components are integrated in **system** block. The constructs are directly related to the corresponding ones in the embedded engineering space. Additional features dealing with grouping, abstractions and parametrizations support modeling of complex systems.

The goal of the paper is to present parallel modeling and verification path supporting development of AADL projects. The main idea is to apply automatic translation of AADL artifacts into the corresponding Colored Petri Nets (CPN) models. These models may be analyzed using existing tools and provide qualitative feedback to AADL development process. The paper focuses on the translation AADL→ CPN provided by the developed translator, and describes verification lane of the models. An overview of main AADL features is presented to provide a background for the proposed approach.

AADL language reached some maturation in the area of tools supporting modeling and verification. The main tool is Eclipse plugin Osate providing several functions: graphical modeling, latency analysis, constraints checking and safety analysis. Ocarina extends Osate functions by code generation. Both tools are accessible under public license – EPL and GPL correspondingly. There are also commercial solutions AADL Inspector seems to be the most popular.

Systematic design and verification case study is presented in the paper. The study starts with definition of general system structure using AADL textual language. In the first step the description focuses on block structure, i.e. blocks with interfaces and connections. Devices which specify environment of the system are also defined. In the next steps the general structure is refined by definition of internal structures, hardware elements, time parameters and scheduling modes. Verification of time requirements (latency, time for specified paths etc.) are verified for the defined system. The next step is safety analysis which needs previous definition of error levels and error possible flows through architecture. The system designed The above mentioned activities allow to design system structure correct with regard to specified time safety parameters. The system frames may be then injected by C/C++, Ada and Java code. The development may be also supported by formal modeling and verification. Translation rules of main AADL structures into Colored Petri nets and possibilities for merging formal verification with AADL development process are also presented.

Indoor Precise Infrared Navigation

Paweł Marzec, Andrzej Kos
AGH University of Science and Technology
Faculty of Computer Science, Electronics and Telecommunications
Krakow, Poland
pmarzec@agh.edu.pl, kos@agh.edu.pl

***Abstract*–The paper proposes an original solution enabling the navigation of a blind person in such buildings as shopping malls and offices as well as public and private institutions. A GPS system fitted with an infrared sensor in the form of a camera is used for navigation. The system detects the surrounding walls in buildings and enables a blind person to keep a safe distance from the walls while moving indoors. Navigational instructions and directions are transmitted to a blind person by means of vibration sensors placed on this person wrists.**

***Keywords*–thermo-navigation, blind people, infrared sensor, indoor navigation**

EXTENDED ABSTRACT

Currently, the number of the blind is increasing, amounting to approx. 36 million, while roughly another 250 million people suffer from vision problems of some kind. The main problem affecting the blind is getting around in an urban environment. In this article is three different methods for determining the distance between a blind person and selected object are described below.

A. Method I – navigating by utilizing the temperature difference between the wall and the base surface

This method makes use of the difference between the temperatures measured by a thermographic camera, which often results from different emissivities of, for example, the wall and the ground. Fig. 1 shows a sample photograph taken inside a building with a conventional camera and a thermographic camera. The maximum measurement error of the distance obtained from the method I is approx. 5 cm relative to the reference measurement.

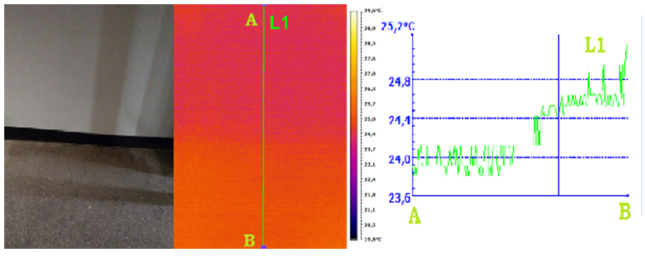


Fig. 1. A fragment of a wall and the ground inside a building (on the left - an image from a photo camera; in the middle – from a thermographic camera; on the right – the temperature diagram for the line L1)

B. Method II – navigating by using one's own reflective heat

In this method, a moving person's own heat that is reflected from an object with a low emissivity coefficient (a high reflection coefficient) is used to determine the distance between a blind person and selected object (Fig. 2). From the thermographic image generated by a thermal sensor we obtain the image S , which the size is proportional to the distance D. The measurement error of the distance obtained from the method II is approx. 2 cm.

Fig. 2. (On the left) - The thermographic image showing the reflection of the heat generated by a human from a glass wall (Method II). (On the right) - a photograph and thermographic image showing a wall with a mounted aluminum tape (Method III)

C. Method III - navigating with the use of an element with a low emissivity coefficient

The suggested solution consists in the use of a thin element, e.g. in the form of a tape, which is placed on an inner wall of a building at a specified height over the base surface (Fig. 2). The tape, having a high thermal reflection coefficient, will cause the heat generated by the person being next to the wall to be reflected from the tape and subsequently recorded by a thermal sensor mounted on the person's arm. The measurement error of the distance obtained from the method III is approx. 3 cm.

This paper presents methods facilitating the mobility of the blind inside buildings like schools or shopping malls. All these methods are complementary and can be simultaneously used for navigating a blind person indoors. In the conducted measurements, the lowest measurement error of approx. 2 cm was achieved for Method II.

ACKNOWLEDGEMENTS

The authors wish to thank for financial support from the subvention No. 16.16.230.434 payed for by the AGH University of Science and Technology, Krakow, Poland

Linux Kernel Driver for External Analog-to-Digital and Digital-to-Analog Converters

Paweł Skrzypiec, Zbigniew Marszałek
Department of Measurement and Electronics
AGH University of Science and Technology
Krakow, Poland
pawel.skrzypiec@agh.edu.pl, antic@agh.edu.pl

***Abstract*—The paper presents the Linux kernel driver for analog-to-digital and digital-to-analog converters control. The proposed module is the main part of the distributed embedded system for impedance measuring applications. The designed prototype consists of three hardware components: Raspberry Pi 3, microcontroller and personal computer. Two experiments verified the functionality and parameters of the constructed system. The first one confirmed that the driver does not utilize processor time while the data processing application is not running. It also showed that the module consumes only 0.7 % and 3.3 % of two cores of a quad-core processor for data readout and its copying to the user space. The mentioned test was performed with the sampling frequency equal to 256 kHz. The second experiment determined the accuracy of impedance measurements done by the constructed prototype. Results were compared with ones realized with the commercially available measuring device usage. The determined measurements uncertainty did not exceed 1.5 %.**

***Keywords*—Linux, kernel, driver, embedded system, microcontroller, impedance measurements.**

I. Introduction

The trend in the modern embedded systems design aims to increase the functionalities of devices working at the network edges [1], [2]. One of the most difficult challenges related to that kind of system design is increasing its functionality without deterioration of its maintainability. The mentioned challenge can be met by open-source libraries or operating systems usage.

The embedded operating systems, such as Linux, allow programmers to focus their attention on problems much more abstract than particular registers accessing. It can solve problems related to data acquisition and processing, but it is not possible to develop one low-level library working on each hardware configuration. The way to improve embedded systems flexibility is an implementation of the hardware-specific logic as custom device drivers.

The proposed Linux kernel driver [3] implements functionalities related to the analog-to-digital (ADC) and digital-to-analog (DAC) converters control. Due to the lack of converters in the Raspberry Pi 3 device, it was adapted to work with external ones integrated with ARM Cortex-M7 core in the STM32F746ZG microcontroller, connected through the Serial Peripheral Interface (SPI) bus. The developed driver was used in the stability and performance requiring impedance measuring system.

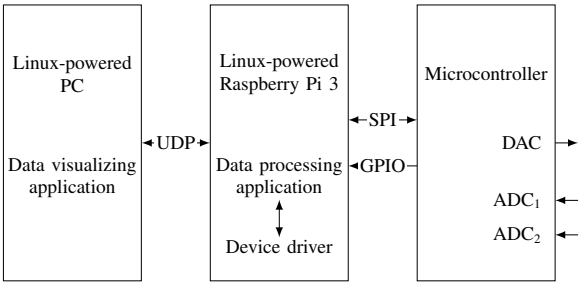


Fig. 1. Distributed system for impedance measurements architecture.

Due to the necessity of the developed driver verification, the test environment was built. It contained two additional software components: data processing application executed in the Raspberry Pi user space and the data visualizer running on the personal computer. The system correctness was verified by the impedance measurements and the comparison of the results with ones done with the Agilent E4980A multimeter usage. The architecture of the constructed system is shown in Fig. 1.

In this work, the Linux kernel driver for external analog-to-digital and digital-to-analog converters was presented. The conducted experiments confirmed that it can be used in the impedance meauring systems requiring precisely synchronized digital-to-analog and analog-to-digital conversions.

The proposed architecture of the impedance measuring system was summarized with the Agilent E4980A multimeter. Results of the realized measurements were compared and used for the constructed system uncertainty estimation. The calculated differences were relatively low: 0.49 Ω and 1.03 Ω for resistance and reactance respectively. It suggests that the proposed architecture can be used in applications not requiring uncertainties lesser than 1 Ω as an alternative for more expensive devices.

References

[1] M. Donno, K. Tange and N.Dragoni, *Foundations and Evolution of Modern Computing Paradigms: Cloud, IoT, Edge, and Fog*, IEEE Access, 10.1109/ACCESS.2019.2947652, Oct. 2019.

[2] C. Avasalcai, C. Tsigkanos and S.Dustdar, *Decentralized Resource Auctioning for Latency-Sensitive Edge Computing*, IEEE International Conference on Edge Computing (EDGE), 2019.

[3] P. Skrzypiec *Development and testing of the embedded operating system kernel module for handling fast A/D and D/A processing*, M.Sc. thesis. AGH 2019.

Multipoint Wireless Humidity and Temperature Monitoring Network for HVAC Systems Validation

Michał Zbieć, Dariusz Obrębski
ICs and Systems Design Department
Sieć Badawcza Łukasiewicz — Instytut Technologii Elektronowej
Warsaw, Poland
E-mails: zbiec@ite.waw.pl, obrebski@ite.waw.pl

***Abstract*—This paper describes multipoint wireless humidity and temperature measurement network designed for validation of HVAC systems performance. It consists of main data logger module and multiple measurement nodes connected via wireless link in 868 MHz ISM band. It characterizes temperature and humidity distribution within measured residential or commercial spaces.**

***Keywords*—Multipoint measurements, IoT, Embedded systems, Wireless communication**

INTRODUCTION

Heating, ventilation and air conditioning (HVAC) systems are not only widely used in big scale commercial buildings, but nowadays more and more often in residential ones too. Their proper operation influences both mood and health of people working and living in climate controlled environment, therefore it is crucial that HVAC system works properly, as designed, not only right after system launch, but through the whole exploitation period. Manual measurements are not sufficient to establish if temperature distribution and air humidity is consistent in large scale living or working space. They only provide single point data from very limited time frame. To properly characterise the HVAC system data from multiple points and long observation time is needed. Periodic measurements lasting few days can reveal instabilities in the system, chart influence of daily variations of external environment etc. They are also able to confirm the performance problems of HVAC installation, that can periodically appear due to the excessive sun operation during summer and low outside temperature in winter. In complicated big scale systems it is also important to measure climate conditions in multiple points. Overall performance of such a system is derived from proper behavior of many HVAC devices. Only by gathering data from multiple sensors located in different parts of controlled environment one can ensure proper behavior of every device involved in the system and localize faulty ones. Such a wide HVAC system characterization can be useful both during system installation, when technicians need to validate if the system have been installed and configured properly, and during exploitation, when it can help user in detection where the problems with HVAC system are located.

Multipoint wireless humidity and temperature monitoring network was developed to answer the above needs. Key concepts in its designing were:

Data logger module - main device of the system. It is responsible for tasks like: measurement scheduling (triggering sensor nodes in correct time slots), data acquisition and logging, user interface, local measurements (measurements with sensor included in data logger module) and system wide settings management. Data logger module can operate as a standalone device, supervising the work of slave devices - sensor nodes - and recording acquired data into the commonly used data carrier - microSD card. Besides, it can operate as a data source for another controller (e.g. PC) connected via USB link.

Sensor nodes - system measurement nodes. Their main role is to carry out measurements, when triggered, and sending them back to the data logger module. Sensor nodes are meant to be dispersed in monitored space and provide data from different locations within it.

Wireless communication - data logger module and sensor nodes are connected together via wireless link working in 868 MHz ISM band. Data logger uses it to schedule measurements, transfer data from sensor nodes, monitor state of their batteries and manage system wide settings.

User interface - data logger provides user interface with 240x128 graphic display and 4x4 keypad. It supports following features: file management (creating, deleting, assigning to sensors), sensor management within the network, current measurements visualization (timestamp, temperature, humidity and state of sensor battery), logged measurements visualization (as a list or graph), system settings (time and data, measurement period, node output power, display brightness).

Battery operation - sensor nodes should be easily settled in various temporary locations, where it may by impossible or impractical to connect them to the power grid. Having that in mind both data logger module and sensor nodes were designed to support battery operation. They are powered from single cell Li-Ion battery and utilize robust battery charging and monitoring system. Current battery state of the sensor nodes is available to data logger via wireless link.

Low power consumption - since the system supports battery operation mode it was crucial to decrease its power consumption to absolute minimum. The lower power consumption the longer devices can operate without recharging. Various software and hardware techniques were used to satisfy this simple statement.

Performance Analysis of Convolutional Neural Networks on Embedded Systems

Łukasz Grzymkowski, Tomasz P. Stefański
Faculty of Electronics, Telecommunications and Informatics
Gdańsk University of Technology, Gdańsk, Poland
emails: lukegrzym@gmail.com, tomstefa@pg.edu.pl

Extended Abstract

The number of applications, where machine learning and neural networks (NNs) have been successfully used, is constantly growing. Examples include object classification [1], object recognition [2],[3], speech recognition [4], sensor data analysis [5].

Training NNs usually requires vast amount of data and takes place in cloud, data centers and servers with powerful computing resources, e.g., with graphics processing units (GPUs). For inference, however, the requirements on processing are not necessarily as high and NNs are often deployed on devices in Internet of Things (IoT). These are embedded systems with hardware and software built for a specific function (e.g., to drive a DC motor, collect sensory data), often with real-time response.

Embedded systems have, however, specific requirements and constraints, especially when machine learning use cases are considered. Energy efficiency is key to prolong the battery life and maximize the duration for which the device can remain operational. Sophisticated power saving modes are supported with deep-sleep modes of operation, voltage and frequency scaling, dynamic disabling of peripherals and clocks. Many of such systems perform periodic operations, e.g., collect sensory data, process it and then switch back to low-power mode for the majority of time. If the time to complete a task is long, however, then the duty cycle, i.e., percentage of time spent in high-power mode, is greater and so is the power consumption.

Other constraint of IoT systems is the dynamic memory. It is especially evident on microcontrollers that may only have SRAM available in hundreds of kilobytes inside the system-on-chip (SoC). This resource must be shared between all applications running on a target platform, including connectivity stack, operating system, drivers, data and I/O buffers and finally weights and intermediary buffers for NNs. Additionally, memory access or cache latency have significant impact on the overall performance of the system.

Finally, the performance of the system is limited by its computing resources. These depend on the type and architecture of processing units used, e.g., a single or multi-core system, instruction set and parallelism, core frequency. IoT systems are, in contrast to a near infinitely scalable data center, always constrained and have a cap on maximum number of computations that can be executed. As mentioned before, embedded systems often run multiple applications simultaneously that share all resources. It is therefore important from the architectural perspective to view the system as a whole and understand the entire software stack when building such systems.

The purpose of this paper is to benchmark performance of convolutional NNs (CNNs) on embedded systems under various conditions. In presented benchmarks, a general-purpose central processing unit (CPU) is used, ARM Cortex-M7 SoC with ARMv7E-M architecture and DSP instructions to accelerate execution of inference engines, i.e., software that implements NN kernels and operations. The benchmarks cover changing core frequency by switching to one of supported SoC run modes, disabling data and instruction cache, disabling DSP instructions support. On the software side, TensorFlow Lite and CMSIS NN [6] are used as inference engines with CNN deployed with varying number of layers. Both real-valued NNs (RVNNs) and complex-valued NNs (CVNNs) are tested, and we elaborate on necessary extensions to functions and operations of RVNN for the complex arithmetic.

We conclude that the system must be tuned in a holistic way to achieve optimal efficiency. This includes core frequency and architecture, memory latency, type of workload and software as well as other system requirements, e.g., power efficiency.

References

[1] A. Krizhevsky, *Learning Multiple Layers of Features from Tiny Images*, University of Toronto, 2009.
[2] A. Krizhevsky, I. Sutskever, and G. E. Hinton, *ImageNet classification with deep convolutional neural networks*, Adv. Neural Inf. Process. Syst., vol. 25, 10.1145/3065386, 2012.
[3] C. Szegedyd, S. Ioffe, V. Vanhoucke, and A. A. Alemi, "Inception–v4, inception–ResNet and the impact of residual connections on learning," in Proceedings of the Thiry-First AAAI Conference on Artificial Intelligence, Feb. 2017, pp. 4278-4284.
[4] G. Hinton, et al., "Deep neural networks for acoustic modeling in speech recognition: the shared views of four research groups," IEEE Sig. Process. Mag., vol. 29, no. 6, pp. 82-97. 2012.
[5] D. Ravi, Ch. Wong, B. Lo, and G. Yang, "A deep learning approach to on-node sensor data analytics for mobile or wearable devices," IEEE J. Biomed. Health Inform., vol. 21, no. 1, pp. 56-64, 2017.
[6] L. Lai, N. Suda, and V. Chandra, "CMSIS-NN: Efficient Neural Network Kernels for Arm Cortex-M CPUs," arXiv preprint, arXiv:1801.06601, 2018.

Rigorous Development of Embedded Systems Supported by Formal Tools

Tomasz Szmuc, Wojciech Szmuc
Department of Applied Computer Science
AGH University of Science and Technology
30-059 Kraków, Poland
tsz@agh.edu.pl, wszmuc@agh.edu.pl

Extended Abstract

Growing scope of embedded systems application domains and extending functionality of microcontrolers raise new challenges in their implementation. Microcontrollers embedded in complicated subsystems cooperating with different environments need careful approach in design and implementation to reduce risk of failures. Cyber Physical Systems (CPS) [2] are good examples of the complexity. Architecture of CPS systems is formed from microcontrolers, networks sensors (IoT) and usually collections of data stored in nebula or cloud structure. Complexity system architecture enormously increases when Smart City applications are considered. Cyber Physical systems of systems architectures are applied in the development. Integration and synchronization of several different subsystems are critical aspects in development of such systems. There are also other application domains where embedded systems are applied in different subsystems. Robot controllers, avionic controllers and autonomous (intelligent) cars should be mentioned here. The later domains are specific due to very hard safety requirements. Development of the all above described systems should be supported by systematic modeling and attentive analysis/verification of developed artifacts. Correctness and safety requirements should be hardly satisfied for Safety Critical Systems [1].

Increasing complexity of embedded systems and large number of safety critical applications imply needs for systematic development methodologies supported by formal methods for analysis and verification during the development. The paper presents next steps in the research towards efficient application of formal methods to support development of embedded systems. Some results in this area were published in the previous publications. General rules for mapping of main UML diagrams into CPN models have been used as a basis in definition of translation rules for SysML. The translation rules for common diagrams have been directly applied, and the selective remaining ones i.e. block definition and internal block diagrams have been defined in [3].

The goal of the paper is to collect the earlier developed partial results and also to complete SysML → CPN the translation algorithm by adding remaining modules, especially translating of use case and sequence diagrams into CPN models. Complemented steps of the translation-verification chain are also described. The remaining links are focused on transformation of CPN output into nuXmv [4] input format and then use of the later system for verification (model checking) of the CPN models.

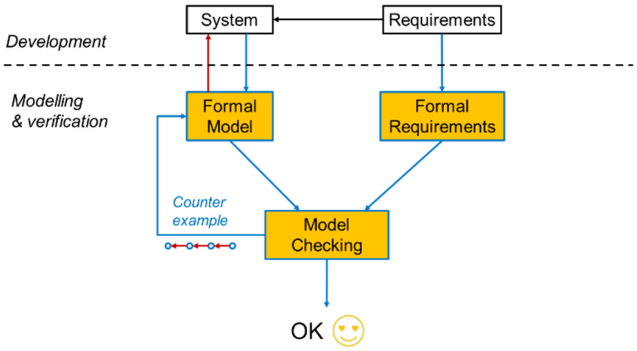


Fig. 1. General concept of formal methods applications

References

[1] J. Boercsoek, JM. Schwarz, E. Ugljesa, P. Holub, and A. Hayek, "*High-availability controller concept for steering systems: The degradable safety controller",* Recent Researches in Circuits, Systems, Communications and Computers, WSEAS. 2011, pp. 222–228.

[2] H.Song, D. B. Rawat, S. Jeschke, and Ch. Brecher, Cyber-Physical Systems. Foundations, Principles, and Applications, Elsevier, Intelligent Data Centric Systems, 2017

[3] W. Szmuc, and T. Szmuc, "Modeling UML object event handling with Petri nets. Towards improvement of embedded systems analysis and design", Proceedings of the 23rd International Conference "Mixed Design of Integrated Circuits and Systems" June 23-25, 2016, Łódź, Poland, pp. 454-457

[4] W. Szmuc, and T. Szmuc, "Towards embedded systems formal verification. Translation from SysML into Petri nets", Proceedings of the 25th International Conference "Mixed Design of Integrated Circuits and Systems" June 21-23, 2018, Gdynia, pp. 420-423

[5] https://nuxmv.fbk.eu/ the nuXmv model Checker

Sensor Fusion Algorithm Implementation on Microchip PIC Microcontroller

Sergio Salas Arriarán*, Carlos Valdez*, Kalun Lau*, M. Hadi Amini†, Marek Kropidłowski‡, Paweł Śniatała‡
*Universidad Peruana de Ciencias Aplicadas (UPC), Prolongacion Primavera 2390, Monterrico, Surco Lima, Peru
†Florida International University, 11200 SW 8th Street Miami, FL 33199
‡Poznan University of Technology, Piotrowo 2, 60-965 Poznań, Poland
E-mail: pawel.sniatala@put.poznan.pl

***Abstract*—The paper describes an implementation of a Brooks-Iyengar algorithm on the Microchip PIC18F4550 platform. The circuit is considered as a testing platform to check the algorithm concept simulated in MATLAB before the final implementation as ASIC IP core. The results confirm the correctness of the proposed approach, which will be used in the final IP Core design.**

***Keywords*—Sensor Fusion, Microcontroller PIC18 family.**

I. Introduction

The introduction of the IoT technology and the various smart environments open new areas of new applications that arise for sensors and sensor networks [1]. Though Wireless Sensor Netwwork (WSN) offers a lot on the plate, some issues have to be addressed. Some of these issues include the possibility of transmission of inaccurate or faulty data. Sensor fusion is a term that is associated with combining of sensory data or data derived from multiple sources such that the resulting information has less uncertainty than would be possible when these sources were used individually [2]. An

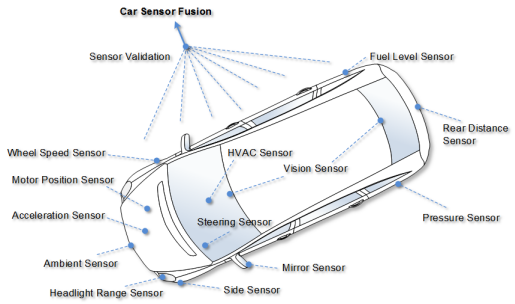


Fig. 1. Example of sensors in a car.

example of the sensor fusion application can be a distance measurement in a modern car, which is illustrated in Fig.1. The information about the measure distance comes from a set of sensors. The system can have many sensors and/or they can be of different types. As mentioned above the signals collected from the sensors can be inaccurate or even unavailable. The final decision about the measured distance should be calculated in a way that faulty sensors would not affect significantly the correctness of the result. It is the purpose of sensor fusion algorithms.

II. Results

In this paper, we focus on the Brooks-Iyengar Hybrid Algorithm [3]. The Brooks-Iyengar hybrid algorithm is suitable for distributed systems that are working in the presence of noisy or inaccurate data. It combines the Byzantine agreement with sensor fusion and seamlessly bridges the gap between them. The algorithm can be touted to be the ideal mix of the famous Dolev's algorithm with the Mahaney and Schneider's Fast Convergence Algorithm (FCA). The algorithm is efficient and runs in $O(NlogN)$ time. The purpose of the implementation of the Brook-Iyengar algorithm on the microcontroller platform is to test the algorithm concept in a real circuit, before the final implementation dedicated for the ASIC realization. We have chosen the PIC18F4550 microcontroller from the Microchip PIC 8-bits family. MPLAB Integrated Development Environment was used to design and compile the program. Proteus simulator has allowed to emulate the circuit. The testing circuit consists of 5 temperature sensors connected to the PIC18F4550 microcontroler. Two analog sensors - LM35 - are connected to analog inputs, which measure the output voltage from the sensor. The ouput range, in the tested environment, is between $0V...5V$. There will be increase in $10mV$ for raise of every $1°C$. Next three sensors are digital: two DS1621 and one SHT11. The DS1621 digital thermometer and thermostat provides 9–bit temperature readings which indicate the temperature of the device. The SHT11 is a single chip relative humidity and temperature multi sensor module comprising a calibrated digital output.The actual results, obtained based on the real circuit experiment, confirm the correctness of the proposed microcontroller based approach.

Acknowledgement

This work has been partially (PŚ, MK) supported by Poznań University of Technology, source: 0311/SBAD/0678

References

[1] B. P. L. Lau, S. H. Marakkalage, Y. Zhou, N. U. Hassan, Y. Chau, Z. Meng, and U. Tan. A survey of data fusion in smart city applications. *Information Fusion*, 52:357–374, 2019.
[2] P. Arroyo, H. J. Luis, J. I. Suárez, and J. Lozano. Wireless sensor network combined with cloud computing for air quality monitoring. *Sensors (Basel, Switzerland)*, 19(3), 2019.
[3] P Śniatała, M. Hadi Amini, and Kianoosh G. Boroojeni. *Fundamentals of Brooks-Iyengar Distributed Sensing Algorithm*. Springer, 2020.

Virtualization of an Aluminum Cans Production Line Using Virtual Reality

Lucas Sales de Oliveira Almeida[1], Alexandre Baratella Lugli[1], Tales Cleber Pimenta[2],
Matheus Vinícius Cirino e Silva[1], João Paulo Carvalho Henriques[1], Renzo Paranaíba Mesquita[1]
[1] Department of Industrial Automation
National Institute of Telecommunications (INATEL)
CEP , 37.540-000, Santa Rita do Sapucaí, MG, Brazil
[2] Institute of Engineering System and Information Technology
Federal University of Itajubá (UNIFEI)
CEP 37.500-903, Itajubá, MG, Brazil
lucassales@gea.inatel.br, baratella@inatel.br, tales@unifei.edu.br,
matheuss@gec.inatel.br, joao.paulo@inatel.br, renzo@inatel.br

Extended Abstract

In this context of the 4.0 industry, new technologies have been aggregated to the industries, which has been pushing production levels and through the use of Big Data keeping great control over its products. Connectivity has been the main focus of this new revolution highlighting the Internet of Things and Systems Integration. One pillar of this massive change industries is Augmented and Virtual Reality (VR), which shows itself as a promising area for training purposes and error diagnoses.

The focus of this paper is to develop a virtual reality system capable of showing a can production company operators the procedure for components exchange in a machine responsible for the extrusion of aluminum cups. For this end an vive device was employed for the immersion of the operator, the full modeling of the machine was also needed. The methods used to fulfill the project goals are presented as well as the tools used to develop the proposed system.

Based on the wide range of Virtual Reality (VR) usage and aiming to create a solution to solve a real problem of a company, comes the proposal of this work: the creation of a Virtual Reality (VR) production line machine with the goal of training employees of a can production company in how to operate, upkeep and overall understand the performance and workings of it. With this solution, factory employees are expected to know how to operate the equipment in advance before they get their hands on the physical equipment, preventing errors from impacting the production process and even causing financial losses for the company.

Unity is the most popular game development platform in the world. It facilitates most of the game development process supporting developers with a vast number of tools to create 2D, 3D, Virtual Reality (VR) and augmented reality (AR) projects. Furthermore, it also counts with a broad community, granting exchange of information among the users. Unity Editor consists of many windows, each one with its specific function. The main screen of the Virtual Reality (VR) Project can be visualized in Figure 1.

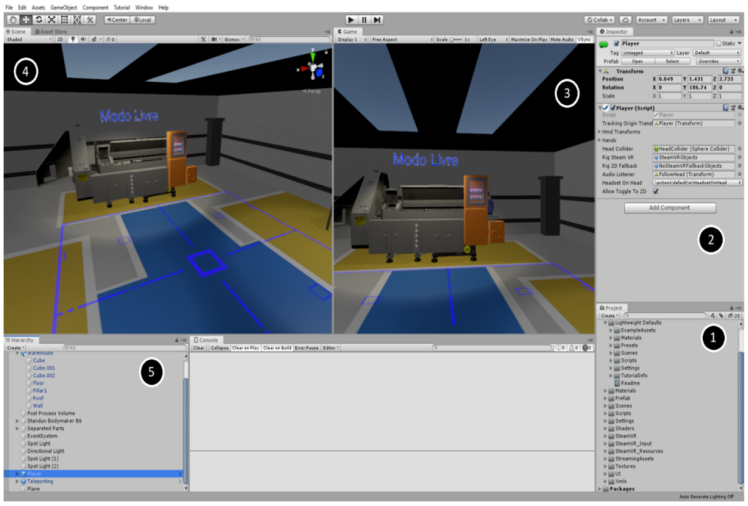


Fig. 1. Virtual Reality (VR) - main screen.

Index of Authors