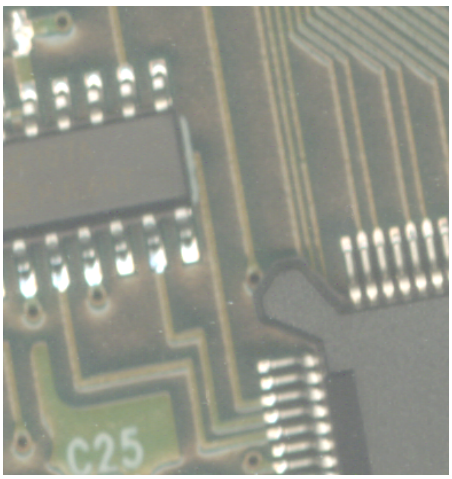
Book of Abstracts of 28th International Conference

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

MIXDES 2021



Łódź, Poland
June 24 – 26, 2021

Organised by:

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

in co-operation with:

Poland Section IEEE - ED & CAS Chapters

Section of Microelectronics & Electron Technology
and Section of Signals, Electronic Circuits & Systems
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee
of International Union of Radio Science – URSI

supported by:

Ministry of Science and Higher Education

Edited by
Andrzej Napieralski

Lodz University of Technology
Department of Microelectronics and Computer Science
ul. Wólczańska 221/223
90-924 Łódź, Poland

Phone: +48 42 631 26 45
Fax: +48 42 638 03 27
E-mail: napier@dmcs.pl
Web: http://www.mixdes.org

Dofinansowano z programu „Doskonała nauka” Ministra Nauki i Szkolnictwa Wyższego.

Printed by
Department of Microelectronics and Computer Science, Lodz University of Technology
ul. Wólczańska 221/223, 90-924 Łódź, Poland

Preface

For 27 years the MIXDES Conference is a forum devoted to recent advances in micro- and nanoelectronics design methods, modelling, simulation, testing and manufacturing technology in diverse areas including embedded systems, MEMS, sensors, actuators, power devices and biomedical applications.

Due to the coronavirus (COVID-19) pandemic, the Scientific and Organising Committees have decided again this year to hold a virtual conference. We are extremely disappointed that we will not meet in person, but we hope, that despite this, the presentations and discussions will be efficient and fruitful.

The program of the conference consists of three days of sessions starting each day with invited talks. The following invited talks will be presented:

- *ASCENT+ European Infrastructure for Nanoelectronics: a Deep Dive to All-GaN IC Technology for Power Electronics*
  Urmimala Chatterjee (IMEC, Belgium)
- *Modeling Passive Devices for CMOS RF Circuits*
  Roberto S. Murphy Arteaga (INAOE, Mexico)
- *Modeling and Simulation of Charge Trapping in 1/f Noise, RTN and BTI: from Devices to Circuits*
  Gilson I. Wirth (Universidade Federal do Rio Grande do Sul, Brazil)

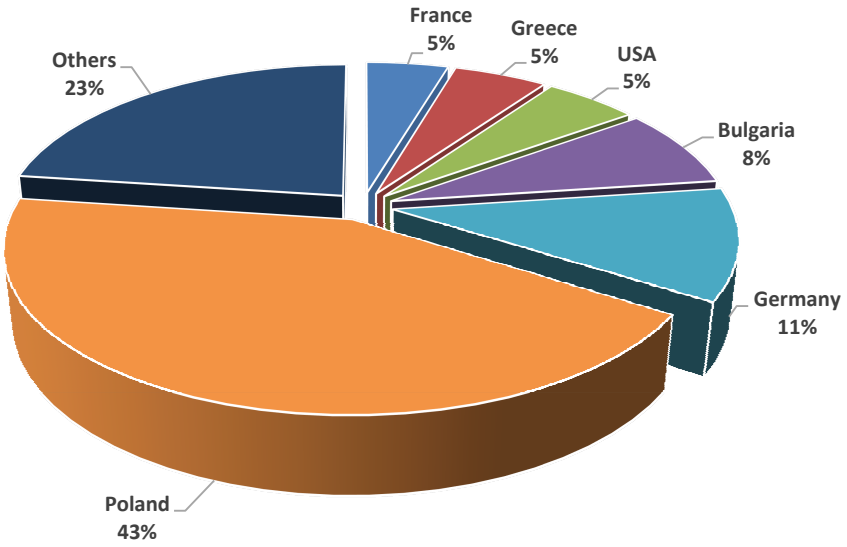
The program of MIXDES 2021 also includes 2 special sessions:

- *Compact Modeling for Semiconductor Device, Sensor and IC Design*
  organised by D. Tomaszewski (Łukasiewicz - Institute of Microelectronics and Photonics, Poland)
  and W. Grabiński (GMC, Switzerland)
- *Fusion Diagnostics I&C Workshop*
  organised by Dr. Stefan Simrock (ITER, France), Dr. Axel Winter (Max Planck Institut für Plasmaphysik, Germany)
  and Dr. Dariusz Makowski (Lodz University of Technology, Poland)

Number of accepted papers and authors by country

Country	Number of		Country	Number of		Country	Number of	
	papers	co-authors		papers	co-authors		papers	co-authors
Armenia	1	1	Greece	1	8	Saudi Arabia	1	2
Belgium	1	1	Iran	2	4	Slovakia	1	4
Brazil	1	1	Ireland	1	1	Spain	0	4
Bulgaria	4	12	Italy	0	3	Switzerland	1	3
Egypt	0	1	Mexico	1	3	Taiwan	1	1
France	5	7	Poland	28	66	UK	1	4
Germany	7	17	Portugal	1	2	USA	3	8
						Total	**61**	**153**

Number of Authors by Country



All regular papers were reviewed and selected from submissions from 21 countries. The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing contributed papers.

We hope that you are safe and healthy and remain so, and we will meet together next year in Wrocław, June 23-25, 2022.

Since our last meeting two members of the conference Programme Committee: Prof. Andrzej Jakubowski and Prof. Ninoslav Stojadinović have passed away. We have experienced a great loss within our community.

Łódź, June 2021

Andrzej NAPIERALSKI
Department of Microelectronics and Computer Science
Lodz University of Technology, Poland
General Chairman of MIXDES 2021

International Programme Committee

Prof.	M. Bucher	Technical University of Crete, Greece
Prof.	J. Cabestany	Universitat Politecnica de Catalunya, Spain
Prof.	J. Collet	LAAS - CNRS, Toulouse, France
Prof.	A. Dąbrowski	Poznan University of Technology, Poland
Prof.	G. De Mey	University of Ghent, Belgium **(Vice-Chairman)**
Prof.	J. Deen	McMaster University, Canada
Prof.	M.H. Fino	Universidade Nova de Lisboa, Portugal
Dr.	D. Foty	Gilgamesh Associates, USA
Prof.	L. Golonka	Wrocław University of Science and Technology, Poland
Prof.	K. Górecki	pGdynia Maritime University, Poland
Dr.	W. Grabiński	GMC, Switzerland
Prof.	P. Gryboś	AGH University of Science and Technology, Poland
Prof.	V. Hahanov	Kharkiv National University of Radioelectronics, Ukraine
Prof.	A. Handkiewicz	Poznan University of Technology, Poland
Prof.	A. Hatzopoulos	Aristotle University of Thessaloniki, Greece
Prof.	S. Hausman	Lodz University of Technology, Poland
Dr.	G. Jabłoński	Lodz University of Technology, Poland
Prof.	A. Kos	AGH University of Science and Technology, Poland
Prof.	W. Kuźmicz	Warsaw University of Technology, Poland
Prof.	C. Lallement	Strasbourg University, France
Prof.	M. Lobur	State University Lviv, Ukraine
Dr.	M.M. Louerat	Université Pierre et Marie Curie, Paris, France
Prof.	T. Łuba	Warsaw University of Technology, Poland
Prof.	B. Macukow	Warsaw University of Technology, Poland
Prof.	J. Madrenas	Universitat Politecnica de Catalunya, Spain
Dr.	D. Makowski	Lodz University of Technology, Poland
Prof.	A. Martinez	LAAS - CNRS, Toulouse, France **(Honorary Chairman)**
Prof.	A. Materka	Lodz University of Technology, Poland
Prof.	W. Mathis	Leibniz University of Hannover, Germany
Prof.	J.M. Moreno	Universitat Politecnica de Catalunya, Spain
Dr.	M. Napieralska	Lodz University of Technology, Poland
Prof.	A. Napieralski	Lodz University of Technology, Poland **(General Chairman)**
Prof.	J. Nishizawa	Semiconductor Research Institute, Japan
Prof.	L. Opalski	Warsaw University of Technology, Poland
Prof.	A. Pfitzner	Warsaw University of Technology, Poland **(Programme Chairman)**
Prof.	E. Piętka	Silesian University of Technology, Poland
Prof.	W. Pleskacz	Warsaw University of Technology, Poland
Dr.	B.F. Romanowicz	Nano Science and Technology Institute, USA
Prof.	J.A. Rubio	Universitat Politecnica de Catalunya, Spain
Prof.	A. Rybarczyk	Poznan University of Technology, Poland
Dr.	J.-M. Sallese	Swiss Federal Institute of Technology, Switzerland
Prof.	D. Sankowski	Lodz University of Technology, Poland
Dr.	M. Schwarz	Robert Bosch GmbH, Germany
Prof.	T. Szmuc	AGH University of Science and Technology, Poland
Dr.	P. Śniatała	Poznań University of Technology, Poland
Prof.	M. Tadeusiewicz	Lodz University of Technology, Poland
Dr.	D. Tomaszewski	Institute of Electron Technology, Warsaw, Poland
Dr.	P. Tounsi	INSA de Toulouse, France
Dr.	M. Turowski	Alphacore, Inc.,USA
Prof.	R. Ubar	Tallinn Technical University, Estonia
Prof.	G. Wachutka	Technische Universitaet Muenchen, Germany
Prof.	K. Wawryn	Technical University of Koszalin, Poland
Prof.	B. Więcek	Lodz University of Technology, Poland
Prof.	S. Yoshitomi	Toshiba Corporation, Japan
Prof.	J. Zarębski	Gdynia Maritime University, Poland
Prof.	M. Zubert	Lodz University of Technology, Poland

Organising Committee

Prof.	A. Napieralski	(Chairman)
Dr.	M. Orlikowski	(Secretary)
Dr.	M. Napieralska	(Vice-Chairman)
Dr.	G. Jabłoński	Department of Microelectronics and Computer Science, Lodz University of Technology, Poland
Prof.	W. Kuźmicz	Institute of Micro- and Optoelectronics, Warsaw University of Technology, Poland

Table of Contents

2 Thermal Issues in Microelectronics

3 Analysis and Modelling of ICs and Microsystems

6 Power Electronics

7 Signal Processing

8 Embedded Systems

MIXDES 2021 Programme

MIXDES 2021 Timetable

Day 1	Thursday, June 24th, 2021		
	ROOM A	ROOM B	ROOM C
09:00	Conference Opening		
09:15	Plenary Session I		
09:45	Session 5	Session 6 (Part 1)	Special Session I
10:45	Break		
11:15	Session 1 (Part 1)	Session 6 (Part 2)	Special Session I

Day 2	Friday, June 25th, 2021		
	ROOM A	ROOM B	ROOM C
09:00	Session 1 (Part 2)	Session 2 & 4 (Part 1)	Special Session II
10:20	Break		
10:40	Session 1 (Part 3)	Session 4 (Part 2)	Special Session II
12:00	Plenary Session II		
13:00			Special Session II

Day 3	Saturday, June 26th, 2021	
	ROOM A	ROOM B
09:00	Plenary Session III	
09:30	Session 1 (Part 4)	Session 3
11:00	Conference Closing	

The MIXDES 2021 Conference sessions are organized using Microsoft Teams platform. We recommend you to install MS Teams application on your computer. It is also possible to connect using MS Teams web application, but note that not all browsers are compatible.

Here are the links for on-line MIXDES 2021 Microsoft Teams sessions for each room valid for all conference days:

ROOM A

ROOM B

ROOM C

For testing purposes we have prepared a test meeting, where we can assist you with testing your connection. Every working day 9:00-11:00 CET till the conference and during the first day conference sessions, we will keep the test meeting opened. You can connect to it, and our colleagues will help you with testing your voice/video connection and screen presentation from your computer. For other hours, please contact us via email (mixdes2021@dmcs.p.lodz.pl).

TEST MEETING

MIXDES 2021 Schedule

Day 1: June 24th 2021 (Thursday)

Time	Room A
09:00	**Conference Openning** Chairman: Prof. A. Pfitzner
09:15	**Plenary Session I** Chairman: Prof. A. Pfitzner *ASCENT+ European Infrastructure for Nanoelectronics: a Deep Dive to All-GaN IC Technology for Power Electronics* U. Chatterjee (IMEC, Belgium), G. Fagas (Univ. College Cork, Ireland)
09:45	**Session 5**: Signal Processing Chairman: Prof. W. Kuźmicz *Safety Application Car Crash Detection Using Multiclass Support Vector Machine* M. Schwarz (Tech. Hochschule Mittelhessen - Univ. of Applied Sciences, Germany), A. Buhmann (Robert Bosch GmbH, Germany) *Comparison of the Effectiveness of the Methods of Recording Physiological Signals Using Passive Electronic Sensors to Obtain Respiratory Parameters in People with Respiratory Dysfunction* I. Karpiel, J. Wołoszyn, K. Olesz, M. Mysiński, M. Urzeniczok, D. Feige, A. Sobotnicki, M. Czerw (Łukasiewicz Research Network - Institute of Medical Techn. and Equipment, Poland) *Structure and Software Elements of Enavi Radar for Large Drones* G. Jaromi (EUROTECH Sp. z o.o., Poland), P. Kabacik, D. Sysak, R. Makowski (Wroclaw Univ. of Techn., Poland)
10:45	***Break***
11:15	**Session 1 (Part 1):** Design of Integrated Circuits and Microsystems Chairman: Prof. W. Kuźmicz *A New High-Speed and Low Power Synchronous Up/Down Counter* M. Ghasemzadeh (Urmia Univ., Iran) *A W-band SiGe BiCMOS I/Q Receiver with Tunable Conversion Gain for Radar Applications* M. Kucharski, M. Widlok (SIRC Sp. z o.o., Poland), P. Bajurko (Warsaw Univ. of Techn., Poland), R. Piesiewicz (SIRC Sp. z o.o., Poland) *Analysis the Effect of Transit Capacitances in Fully Differential Operational Transconductance Amplifiers* I. Uzunov (GlobalFoundries, Bulgaria), B. Nikov (On Semiconductor, Switzerland) *Class AB Operational Amplifier in CMOS 55 nm Technology* P. Pieńczuk (Łukasiewicz Research Network - Inst. of Microel. and Photonics, Poland), W.A. Pleskacz (Warsaw Univ. of Techn., Poland), M. Teodorowski (OmniChip Sp. z o.o., Poland)

Day 1: June 24th 2021 (Thursday)

Time	Room B
09:45	**Session 6 (Part 1)**: Embedded Systems Chairman: Dr. D. Makowski *A Microcontroller Based System for the Selected Gases Detection with Alert Feature* M. Niewiński, W. Szczerek (Warsaw Univ. of Techn., Poland) *A Study of Detection Probabilities and Real-World Testing of a Human Immunity Inspired Intrusion Detection System* P. Widulinski, K. Wawryn (Koszalin Univ. of Techn., Poland) *Comparative Analysis of Methods and Tools for Formal Modelling and Verification for Embedded Systems. Probabilistic Approach* M. Golonka (AGH Univ. of Science and Techn., Poland)
10:45	**Break**
11:15	**Session 6 (Part 2)**: Embedded Systems Chairman: Dr. D. Makowski *Comprehensive Information System for Management of Personalized Protective Thermally Active Clothing* R. Kotas, M. Kamiński, W. Tylman, S. Woźniak, M. Wojtera (Lodz Univ. of Techn., Poland), A. Dąbrowska (Central Inst. for Labour Protection - National Research Inst., Poland) *Implementation of Coprocessor for Integer Multiple Precision Arithmetic on Zynq Ultrascale+ MPSoC* T. Stefanski (Gdansk Univ. of Techn., Poland), K. Rudnicki (Brightelligence Sp. z o.o., Poland), W. Żebrowski (Aldec Inc., Gdansk Office, Poland) *Logging Debug Data from IoT Embedded Devices over the GSM Network* L. Bogdanov (Tech. Univ. Sofia, Bulgaria) *The Comparison of Native and Hybrid Mobile Applications for Android System* A. Kaczmarczyk, W. Zabierowski (Lodz Univ. of Techn., Poland)

Day 1: June 24th 2021 (Thursday)

Time	Room C
09:45	**Special Session I (Part 1):** Compact Modeling for Semiconductor Device, Sensor and IC Design Chairman: Prof. M.H. Fino *Compact Device Modeling and Simulation with Qucs/Qucs-S/Xyce Modular Libraries* M. Brinson (London Metropolitan Univ., UK), F. Salfelder (Univ. Leeds, UK) *Modelling Challenges for Enabling High Performance Amplifiers in 5G/6G Applications* N. Poluri, M.M. De Souza (The Univ. of Sheffield, UK), N. Venkatesan, P. Fay (Univ. of Notre Dame, USA) *Simulation and Modeling Methodologies: Enabler for Neuromorphic Computing Applications* M. Schwarz (Tech. Hochschule Mittelhessen - Univ. of Applied Sciences, Germany)
10:45	**Break**
11:15	**Special Session I (Part 2):** Compact Modeling for Semiconductor Device, Sensor and IC Design Chairman: Dr. W. Grabiński *Compact Analytical Model of Nanowire Junctionless ISFET* A. Yesayan (Inst. of Radiophysics and Electronics, Armenia), J.-M. Sallese (Swiss Federal Inst. of Techn., Switzerland) *Mechanical and Electrical Design Strategies for Flexible InGaZnO Circuits* G. Cantarella, N. Münzenrieder, L. Petti (Free Univ. Bozen-Bolzano, Italy), K. Ishida, T. Meister, C. Carta, F. Ellinger (TU Dresden, Germany), R. Hopf (Swiss Federal Inst. of Techn., Switzerland) *A Model-oriented Methodology for the Automatic Parameter Extraction of TFT Model* M.H. Fino (Univ. Nova de Lisboa, Portugal), P. Barquinha (Nova School of Science and Techn., Portugal) *Variability-Aware Characterization of Current Mirrors Based on Organic Thin-Film Transistors on Flexible Substrates* A. Nikolaou, J. Leise, J. Pruefer (Tech. Hochschule Mittelhessen - Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), U. Zschieschang, H. Klauk (Max Planck Inst. for Solid State Research, Germany), G. Darbandy (Tech. Hochschule Mittelhessen - Univ. of Applied Sciences, Germany), B. Iniguez (Univ. Rovira i Virgili, Spain), A. Kloes (Tech. Hochschule Mittelhessen - Univ. of Applied Sciences, Germany)

Day 2: June 25th 2021 (Friday)

Time	Room A
09:00	**Session 1 (Part 2)**: Design of Integrated Circuits and Microsystems Chairman: Dr. M. Schwarz *GaN-AlGaN on SiC pHEMT Advanced Design for a Digital Radio Frequency Memory* C. Lessi (National Tech. Unive. Athens, Greece), V. Vallindras, K. Hadjisavva (Hellenic Naval Academy, Greece), E. Karagianni (Hellenic Naval Academy and Hellenic Naval Academy, Greece), G. Deligeorgis, A. Stavrinidis, G. Konstantinidis (Foundation for Research and Techn. Hellas, Creta, Greece), A. Panagopoulos (National Tech. Unive. Athens, Greece) *Exploiting Design Modularity and Relocation to Increase Productivity in FPGA-based Computing Systems* Z. Mudza (Lodz Univ. of Techn., Poland) *Investigation of Inductor-based Fully On-chip Boost Converter* R. Ondica, D. Arbet, M. Kováč, V. Stopjaková (Slovak Univ. of Techn. in Bratislava, Slovakia) *Hardware Obfuscation of the 16-bit S-box in the MK-3 Cipher* J. Blocklove (Rochester Inst. of Techn., USA), S. Farris, M. Kurdziel (L3Harris Technologies, USA), M. Łukowiak, S. Radziszowski (Rochester Inst. of Techn., USA)
10:20	***Break***
10:40	**Session 1 (Part 3)**: Design of Integrated Circuits and Microsystems Chairman: Prof. A. Pfitzner *Molecular Diffusion Simulation on ARUZ - Massively-parallel FPGA-based Machine* R. Kiełbik, K. Hałagan (Lodz Univ. of Techn., Poland), K. Rudnicki (Brightelligence Sp. z o.o., Poland), P. Polanowski, G. Jabłoński, J. Jung (Lodz Univ. of Techn., Poland) *Molecular Simulations Using Boltzmann's Thermally Activated Diffusion - Implementation on ARUZ - Massively-parallel FPGA-based Machine* G. Jabłoński, P. Amrozik, K. Hałagan (Lodz Univ. of Techn., Poland) *Modelling of First- and Second-order Chemical Reactions on ARUZ - Massively-parallel FPGA-based Machine* P. Amrozik, K. Hałagan (Lodz Univ. of Techn., Poland), K. Rudnicki (Brightelligence Sp. z o.o., Poland) *Tree-Based Hardware Recursion for Divide-and-Conquer Algorithms* B. Morrison, M. Łukowiak (Rochester Inst. of Techn., USA)
12:00	**Plenary Session II** Chairman: Dr. D. Tomaszewski *Modeling and Simulation of Charge Trapping in 1/f Noise, RTN and BTI: from Devices to Circuits* G. Wirth (Univ. Federal do Rio Grande do Sul, Brazil)

Day 2: June 25th 2021 (Friday)

Time	Room B
09:00	**Session 2 & 4 (Part 1):** Thermal Issues in Microelectronics & Power Electronics Chairman: Dr. M. Janicki *Analysis of Heat Transfer Processes in Electronic Nanostructures Using the Dual-Phase-Lag Model* M. Janicki, A. Sobczak, G. Jabłoński (Lodz Univ. of Techn., Poland) *Comparison of the Usefulness of Selected Thermo-sensitive Parameters of Power MOSFETs* K. Górecki, K. Posobkiewicz (Gdynia Maritime Univ., Poland) *Application of Thin Film Ultralow-Power Lead-Free Perovskite Solar Energy Harvesters in Power Management Systems* M. Aleksandrova, I. Pandiev (Tech. Univ. Sofia, Bulgaria) *Spatial Radiation Patterns of Selected Solid State Light Sources* *K. Górecki, P. Ptak, Ł. Bruski (Gdynia Maritime Univ., Poland)*
10:20	***Break***
10:40	**Session 4 (Part 2):** Power Electronics Chairman: Dr. M. Janicki *Dedicated Multi-element Electronic System for Personalized Protective Thermally Active Clothing* B. Pękosławski, P. Marciniak, Ł. Starzak, A. Stawiński (Lodz Univ. of Techn., Poland), G. Bartkowiak (Central Inst. for Labour Protection - National Research Inst., Poland) *Design of an Overcurrent Protection Relay Based on Electronics Technology* B. Agheli, A. Kalami (Urmia Branch, Islamic Azad Univ., Iran), A. Amini (Sina Bioelectronics Company, Iran) *Development of A Laser Headlight Driver and Dynamic Resistance Variations of Laser Diodes* K.-J. Pai (National Taiwan Normal Univ., Taiwan) *New Monolithic Multi-terminal Si-chips Integrating a Power Converter Phase-leg for Specific Applications* A. Oumaziz (LAAS-CNRS, Univ. Toulouse and LAPLACE, Univ. Toulouse, France), A. Bourennane (LAAS-CNRS, Univ. Toulouse, France), F. Richardeau (LAPLACE, Univ. Toulouse, France)

Day 2: June 25th 2021 (Friday)

Time	Room C
09:00	**Special Session II (Part 1):** Fusion Diagnostics I&C Workshop Chairman: Dr. S. Simrock *Introduction* D. Makowski (Lodz Univ. of Techn., Poland) *Imaging Diagnostics at ITER* S. Simrock (ITER Organization, France) *Overview of Image Data Acquisition for W7-X Stellarator* A. Winter (Max Planck Inst. for Plasma Physics, Germany) *Challenges of Data Acquisition and Real-time Processing for ITER Imaging Diagnostics* V. Martin (Bertin Technologies, France) *Scalable and Versatile Image Acquisition and Processing System Based on MictoTCA.4 Standard* D. Makowski (Lodz Univ. of Techn., Poland)
10:20	***Break***
10:40	**Special Session II (Part 2):** Fusion Diagnostics I&C Workshop Chairman: Dr. D. Makowski *Universal Image Acquisition Software Framework Based on GenICam Standard* P. Perek (Lodz Univ. of Techn., Poland) *Architecture of the W7-X Real Time Divertor Protection System* S. Fischer (Max Planck Inst. for Plasma Physics, Germany) *Imaging Diagnostics at W7-X* M. Jakubowski (Max Planck Inst. for Plasma Physics, Germany) *Real-time Detection of Overloads on Plasma Facing Components* A.P. Sitjes (Max Planck Inst. for Plasma Physics, Germany)
12:00	**Lunch**
13:00	**Special Session II (Part 3):** Fusion Diagnostics I&C Workshop Chairman: Dr. A. Winter *Evaluation of Nvidia Xavier NX Platform for Real-Time Image Processing for Fusion Diagnostics* B. Jabłoński, D. Makowski, P. Perek (Lodz Univ. of Techn., Poland) *Tomographic Reconstruction for Soft X-ray Diagnostics* D. Mazon (CEA, IRFM, France) *ThermaVIP Framework for Image Processing* V. Moncada (CEA, IRFM, France) *Low-noise Amplifier for Photomultiplier Tube Detectors for Plasma Diagnostics* P. Nowak vel Nowakowski, D. Makowski, A. Mielczarek (Lodz Univ. of Techn., Poland) *Novel ANC Simulation Based on VSSLMS Method for Reducing the Microphonics Effects in Cavities* F. Abdi, W. Jałmużna, W. Cichalewski, A. Napieralski (Lodz Univ. of Techn., Poland)

Day 3: June 26th 2021 (Saturday)

Time	Room A
09:00	**Plenary Session III** Chairman: Prof. A. Pfitzner *Modeling Passive Devices for CMOS RF Circuits* J. Valdés, R. Torres, R. Murphy (INAOE, Mexico)
09:30	**Session 1 (Part 4):** Design of Integrated Circuits and Microsystems Chairman: Prof. K. Górecki *Implementation of a Modified High-Voltage Unity-Gain Voltage Buffer* M. Jankowski (Lodz Univ. of Techn., Poland) *Queuing Parallel Computing CAD Tasks in the Design and Optimization of IC Topography* A. Wojtasik (Warsaw Univ. of Techn., Poland) *Rail to Rail Comparator for SAR ADC in Biomedical Applications* N. ALjehani (King Saud Univ., Saudi Arabia), M. Abbas (King Saud Univ., Saudi Arabia and Assiut Univ., Egypt) *Software Tool Aiding Analysis and Design of Low Power Parallel Prefix Adders* I. Brzozowski (AGH Univ. of Science and Techn., Poland)
11:00	**Conference Closing**

Time	Room B
09:30	**Session 3:** Analysis and Modelling of ICs and Microsystems Chairman: Dr. M. Schwarz *A Simple Method for Analysis of Operation of JLFET THz Radiation Sensors* M. Zaborowski, D. Tomaszewski, J. Marczewski (Łukasiewicz Research Network - Inst. of Microel. and Photonics, Poland), P. Zagrajek (Military Univ. of Techn., Poland) *Application of Maximum Power Point Tracking Algorithm in Simulation of PV Systems* J. Nazdrowicz, M. Jankowski (Lodz Univ. of Techn., Poland) *Development of PSpice Macromodel for Monolithic Single-Supply Power Amplifiers* I. Pandiev (Tech. Univ. Sofia, Bulgaria) *Study of Nanowire Characteristics of a Junctionless Transistor Depending on the Gate Length* G. Angelov, R. Rusev, I. Ruskova, E. Gieva, D. Nikolov, M. Spasova, M. Hristov, R. Radonov (Tech. Univ. Sofia, Bulgaria)

General Invited Papers

ASCENT+ European Infrastructure for Nanoelectronics: a Deep Dive to All-GaN IC Technology for Power Electronics

Urmimala Chatterjee
GaN Power Electronics
IMEC, Belgium
Leuven, Belgium
urmimala.chatterjee@gmail.com

Giorgos Fagas
Tyndall National Institute
University College Cork
Cork, Ireland
georgios.fagas@tyndall.ie

I. Introduction

ASCENT+ brings together 15 partners to foster the nanoelectronics community, integrating a unique research infrastructure with unprecedented credentials. ASCENT+ serves as a direct entry point to key enabling capabilities in state-of-the-art processing, modelling and simulation data sets, metrology and characterization, and devices and test structures. Focus areas include: Quantum advantage using solid-state platforms; Low-power, energy-efficient, high-performance computing based on disruptive devices; Increased functionality through advanced integration of a diverse range of materials and innovative technologies. The ASCENT+ program offers free-of-charge access to world-leading infrastructure empowering users to make advances in nanoelectronics. Below, we take a deep dive into the GaN IC offer by Imec for power electronics.

II. IMEC Offer: All-GaN GANIC Technology

Discrete GaN devices today dominate the GaN market either as Off-the-shell components or customized designs through foundry technology. Furthermore, to unlock the full potential for fast switching GaN technology in high power application, monolithic integration is crucial. For instance, integration reduces the parasitic between the driver and the power devices or between the two power devices and a half bridge (HB) at the switching node etc. It helps to reduce ringing, switching loss which in-turn makes a smooth highly efficient circuit. Moreover, GANIC provides a faster, smaller, lighter, and more cost-effective solution compared to its other silicon alternatives. However, this monolithic integration in GaN technology faces some technological and circuit level challenges. One of the those is back-gating effect (BGE) that makes monolithic integration of half-bridge (HB) switches very difficult, in which two devices are connected in a single substrate and source of both devices are not in a same potential. This effect highly impacts the performance of the high-side switch.

As a potential solution we propose to implement it on GaNon-SOI with trench isolation to fully isolate the HEMTs as well as their respective silicon device layers that are cut off horizontally by a trench. It means for a HB on SOI with deep trench isolation, the buried oxide, and the oxide field trench, isolate the HS switch galvanic from the LS devices, and from the Si substrate. The local deep Si contact connecting the source of each device to the thin Si layer which is the top of the original SOI substrate guarantees that the source-bulk potential is zero. This technology is capable to eliminate the BGE completely. Besides, p-GaN HEMTs passive components are also integrated and that can be used to make integrated circuits. An example of a HB switch with integrated driver is shown in Fig. 1 [1].

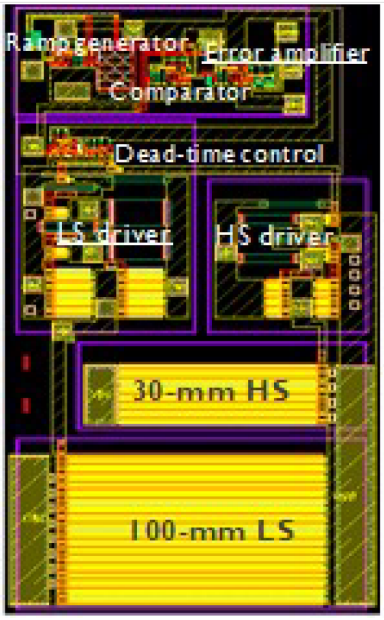


Figure 1. Layout of HB switch with integrated drivers

Acknowledgment

The ASCENT+ programme receives funding from the European Union through H2020 Grant Agreement 871130.

References

[1] X. Li, N. Amirifar et al., "GaN-on-SOI : monolithically integrated All-GaN ICs for power conversion," IEEE IEDM, San Francisco, CA, USA, December 2019.

Modeling Passive Devices for CMOS RF Circuits

José Valdés, Reydezel Torres, Roberto Murphy
Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE)
Tonantzintla, Puebla, México
rmurphy@ieee.org

Extended Abstract

As technology evolves, more and more functions and applications are readily implemented using CMOS circuitry; wireless electronics have become commonplace in our daily life. The development of these circuits involves extensive research leading to accurate models for simulation, which have to include all the effects associated with the circuit, which is embedded in the substrate. As frequency of operation increases, many more effects, which are negligible at lower frequencies, become apparent, up to the point that some can become dominant in this range.

RF modeling of the MOS transistor has thus been the object of extensive research over the last few decades, and a continuous field of endeavor since higher operating frequencies can be reached as the devices become smaller, and hence, faster, and better models —electrical, physical, mathematical and for simulation, have to be developed on an almost daily basis.

But ICs are not made solely of transistors; many passive structures have to be built on the same chip to attain the desired function of the circuit, such as resistors, capacitors, inductors, transformers and interconnects.

Throughout the years, many articles have also been published in reference to the parasitic effects associated with these components, as well as forms to ameliorate them, as they can lead to catastrophic failure if they are not adequately taken into account at the design and simulation stages.

In this paper we present the models of an integrated inductor and that of a coplanar waveguide (CPW), compared to measurements up to 60 GHz. These are common structures now present in almost all modern ICs, and an important effect associated with them are the losses due to the ground shields that are built underneath these structures to reduce electromagnetic interference. These shields are generally made of metal or poly silicon, and they can be solid, meshed or patterned, as represented in Fig. 1. The response of the device is highly influenced by the type of shield over which it is built, and there is no clear-cut distinction as to which is better, the answer varying according to the application.

All the structures were fabricated at IMEC; Fig. 2 shows a micrograph of the integrated inductors. Identical structures were built using different types of ground shields, in order to be able to compare their response. Octagonal and circular devices were available.

Several CPWs were also fabricated on the same chip; a depiction of a typical one is shown in Fig. 3.

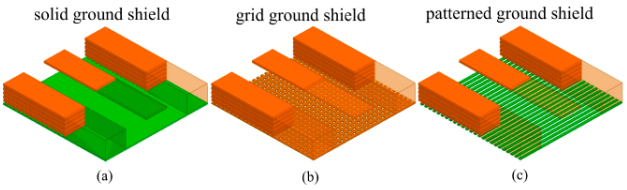


Fig. 1. Common types of ground shields. a) Solid ground shield (SGS). b) Mesh ground shield (MGS). c) Patterned ground shield (PGS).

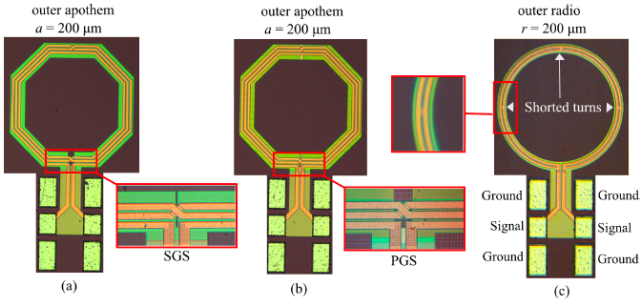


Fig. 2. Micrograph of some of the integrated inductors.

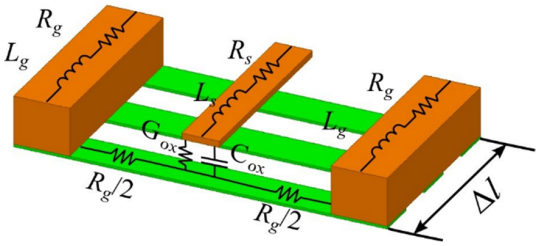


Fig. 2. Typical structure for a CPW.

In both cases, the models herein developed compare very well to experimental data up to 60 GHz. They are simple and easily implemented at the design and simulation stages of wireless ICs.

Acknowledgment

The authors want to thank CONACyT, Mexico, for the partial support of this work through grants 285199 and 288875 and scholarship number 455123. They also thank IMEC, Heverlee, Belgium, for the fabrication of the structures used for these studies.

Modeling and Simulation of Charge Trapping in 1/f Noise, RTN and BTI: from Devices to Circuits

Gilson Wirth
Electrical Engineering Department, UFRGS
Porto Alegre, Brazil
gilson.wirth@ufrgs.br

EXTENDED ABSTRACT

Besides the already well-established time-zero variability, there is an additional stochastic shift of device's electrical parameters related to charge trapping and de-trapping [1-3]. This means that the electrical behavior may change from one instant in time to the other. In this presentation we discuss the unified statistical modeling of charge trapping in the context of 1/f noise, RTN and BTI. The focus is on circuit (electrical) level models to support circuit designers. First, modeling at device (transistor) level is presented. Then, the time dependent performance variability of circuits is discussed.

Modeling is based on discrete device physics quantities, which cause variability in the electrical behavior of MOSFETs. It allows for the derivation of analytical formulations for 1/f noise (frequency domain), RTN (time domain) and BTI using a single modeling framework.

Transistor area plays a major role when it comes to time dependent variability. The area scaling of threshold voltage (or drain current) variance over time is detailed and discussed, supporting designers in transistor sizing towards a more reliable design. The impact of time-dependent variability is smaller in larger area transistors. On the other hand, to achieve higher performances and lower power consumptions, the capacitive load must be minimized, which is achieved by reducing the transistor area. Obviously, there is a trade-off between performance, power consumption and reliability. The circuit designers must work to find the optimal device sizing, demanding accurate models to support their work.

Large devices employed in the past behaved almost identically over time due to the large number of defects stochastically distributed in the device. However, as devices shrink to nanometer dimension, the number of defects per device decreases [1-3]. Consequently, devices that by design should behave identically may show different behavior, and the behavior of a single device may be different at different times.

This increase in time-dependent variability related to charge trapping challenges the design of circuits with nanometer sized devices, as either the margin becomes too pessimistic, or the circuit becomes unreliable. Also, traditional statistical average modeling is not suitable. An average based assessment will not guarantee reliability. Guaranteeing reliability by using a worst margin will be too stringent on circuit design.

As relevant case studies at circuit level, it is discussed how charge trapping produces timing jitter in digital circuits and phase noise in analog circuits.

A reliable estimate of the delay through a CMOS logic gate is a key point in VLSI design. The actual gate delay depends on the state of each trap in its transistors. If a trap is occupied, the transistor shows a lower drain current, leading to a longer propagation delay. Hence, trap switching causes time dependent variability (jitter) of propagation delay. In the case of a ring oscillator, it induces oscillation period jitter. The observed delay or period jitter depends on observation window and circuit bandwidth.

In frequency domain, RTN produces phase noise [4]. An ideal oscillator would show power only at the oscillation frequency. The up conversion of 1/f noise leads to phase noise, spreading the power around the oscillation frequency. In communication systems, the frequency band is divided into frequency slots for the different channels. The phase noise around a carrier frequency interferes with the signal in the adjacent channel. The higher the phase noise, the further apart the channels must be placed. This leads to fewer channels in the available bandwidth: lower capacity of the communication system.

Parameter extraction is also addressed, showing that it is possible to extract model parameters without having to characterize individual trap step heights (individual trap amplitudes). For both time and frequency domain, the model parameters are trap amplitude contribution and trap density. These parameters can be extracted from measured distributions, either in time domain or frequency domain. Also of interest is that once the parameters are extracted from frequency domain measurements (low frequency) noise, they may be used for the modeling in time domain. The reciprocal also holds, parameters extracted from time domain measurements may be used for modeling in frequency domain.

Charge trapping in novel nano-electronic devices, such as resistive switching devices (ReRAM) is also addressed [5].

REFERENCES

[1] T Grasser (ed.), Noise in Nanoscale Semiconductor Devices, Springer, 2020.

[2] T Grasser (ed.), Bias Temperature Instability for Devices and Circuits, Springer, 2014.

[3] G. Wirth, "Time-Dependent Random Threshold Voltage Variation Due to Random Telegraph Noise," in IEEE TED, pp. 17-23, Jan. 2021.

[4] M von Haartman and M Östling, Low-Frequency Noise in Advanced MOS Devices. Springer, 2007.

[5] T. Becker et al., "An Electrical Model for Trap Coupling Effects on Random Telegraph Noise," in IEEE EDL, pp. 1596-1599, Oct. 2020.

Compact Modeling for Semiconductor Device, Sensor and IC Design

A Model-oriented Methodology for the Automatic Parameter Extraction of TFT Model

Maria Helena Fino
Department of Electrotechnical and Computer Engineering
Nova School of Science and Technology
Caparica, Portugal
hfino@fct.unl.pt

Pedro Barquinha
Department of Material Science
Nova School of Science and Technology
Caparica, Portugal
pmcb@fct.unl.pt

***Abstract*—The paper presents a model-driven methodology for the determination of thin-film transistors compact model parameters. The implementation of the proposed extraction methodology in python is presented. The validity of results obtained against devices characteristics is demonstrated. The advantage of the proposed methodology against a previously proposed approached is also discussed.**

***Keywords*—TFTs, compact model parameters**

I. Introduction

Due to the ever-growing application of thin-film transistors (TFT) in a wide range of industrial applications, , e.g., displays, radio-frequency identification tags (RIFID), a strong effort has been paid to the development of TFT compact models, as a way of offering designers the possibility of accurately simulating systems comprising this type of transistors [1]. Several methodologies for evaluating Mosfet threshold have been presented and critically compared [2]. In [3], particular emphasis is given to the extraction of the threshold voltage, the mobility enhancement factor, and the series resistance of TFTs. In this paper a methodology for the automatic evaluation of TFT model parameters will be presented.

II. Thin Film Transistor Model

The drain current of the thin film transistor is based on the model proposed in [3], and is given by:

$$I_{Ds} = \begin{cases} \frac{\mathrm{K}\, V_{ovd}^{m-2}}{0.5\ \alpha}\left(V_{ovd} - \frac{V_{DS}}{2\alpha}\right) V_{DS}(1+\lambda V_{DS}) & V_{DS} < V_{DSAT}, \\ \mathrm{K}\, V_{ovd}{}^{\mathrm{m}} \quad V_{DS}(1+\lambda V_{DS})\alpha & V_{DS} \geq V_{DSAT}, \end{cases} \tag{1}$$

where α is a fitting parameter and *K* and *m* are given by

$$K = \frac{W}{L_{eff}} \frac{\mu_0}{V_{AA}{}^{\gamma}} C_i \alpha \tag{2.a}$$

$$m = 2 + \gamma \tag{2.b}$$

III. Parameter Extraction Methodology

The methodology adopted comprises two steps. In the first step parameters for saturation regime are evaluated. In the second step linear regime is accounted for.

In the saturation regime, we may conclude that by

$$\frac{I_{DS\_sat}}{gm} = \frac{(V_{GS} - V_T)}{m} \tag{7}$$

The first step in the proposed methodology, considers evaluating *gm*, from the TFT transfer characteristic and then, fitting Id/gm to (6) as a way of obtaining values for the threshold voltage *Vt,* and the power parameter *m*. Then the remaining parameters are obtaining through curve fitting to the device characteristics obtained from measurements. Validation of the results obtained is illustrated in Fig. 1.

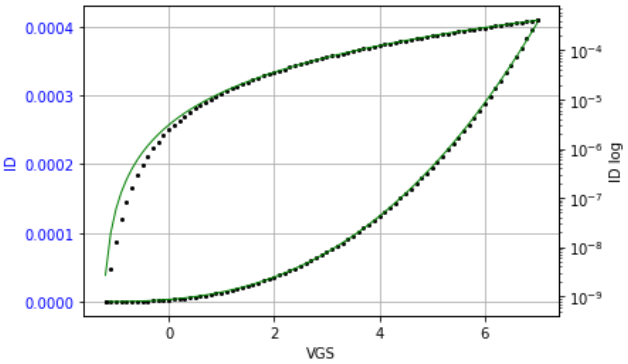


Fig. 1. Id(vgs) characteristics

References

[1] N. Lu, W. Jiang, Q. Wu, D. Geng, L. Li, and M. Liu, "A review for compact model of thin-film transistors (TFTs)," *Micromachines*, vol. 9, no. 11, 2018.

[2] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. Terán Barrios, J. J. Liou, and C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods," Microelectron. Reliab., vol. 53, no. 1, pp. 90–104, Jan. 2013.

[3] R. Rodriguez-Davila, A. Ortiz-Conde, C. Avila-Avendano, and M. A. Quevedo-Lopez, "A New Integration-Based Procedure to Extract the Threshold Voltage, the Mobility Enhancement Factor, and the Series Resistance of Thin-Film MOSFETs," IEEE Trans. Electron Devices, vol. 66, no. 7, pp. 2979–2985, 2019.

Compact Analytical Model of Nanowire Junctionless ISFET

Ashkhen Yesayan
Institute of Radiophysics and Electronics
Ashtarak, Armenia
yesayan.ash@ieee.org

Jean-Michel Sallese
Swiss Federal Institute of Technologyin Lausanne,
Lausanne, Switzerland
jean-michel.sallese@epfl.ch

Extended Abstract

Ion sensitive field effect transistors (IS FET) attracted a lot of attention as bio-chemical sensors since they provide high sensitivity, high spatial resolution enabling very focused detection, and ease of integration within CMOS technology. The ISFET technology was moved to nanowires ISFETs at the beginning of this century. Nanowires become widely used as biosensors [1]. The high surface to volume ratio of NWs is a great advantage over the bulk devices. The conversion of an FET into a sensing device involves the replacement of the metal gate electrode by a biochemically sensitive surface which is brought into contact with the analyte solution. In this paper we discuss analytical modeling of nanowire junctionless ISFETs (JL NW ISFET). The main advantage of junctionless architecture is the simplification of its fabrication technology.

The analytical model for JL NW ISFET valid in all regions of operation was introduced in [2]. The presented discussion on device sensitivity makes evident that the high sensitivity is reached when JL ISFETs operate in subthreshold regime. Hence considering the importance of this operation mode we developed here an explicit model of JL NW ISFET compatible with circuit simulators. A simple compact model is introduced to calculate the Current-pH characteristics relying on JL FET explicit drain current model [3]. The model is validated with COMSOL Multiphysics simulations and presented in Fig. 1-2. The NW JL ISFET sensitivity dependence on pH is illustrated in Fig. 1, where inset illustrates NW JL ISFET structure. The Current-pH characteristics are illustrated in Fig. 2.

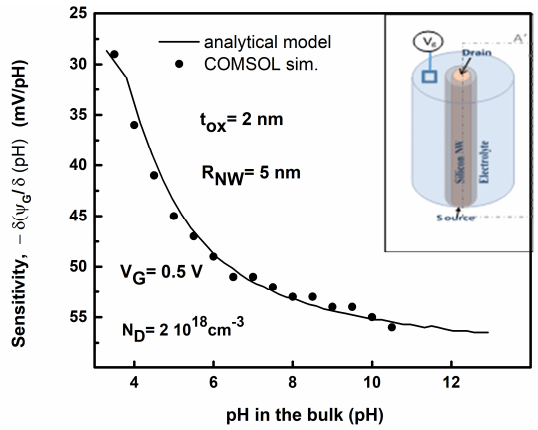


Fig. 1. Sensitivity calculated as a derivative of oxide surface potential versus pH. Inset: structure of NW JL ISFET.

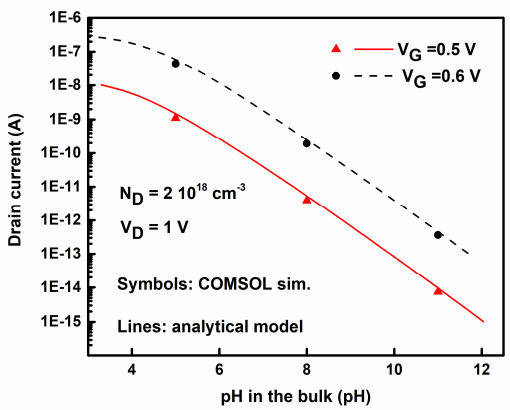


Fig. 2. The drain current versus pH in the bulk.

Finally, the sensitivity dependence on nanowire physical and geometrical parameters are discussed as guidelines for the device optimization. We have analyzed JL NW ISFET sensitivity dependence on nanowire diameter, doping density and oxide thickness. These are important to optimize the device technological process.

Calculations show that the sensitivity is higher for thinner oxide layers, whereas it decreases with increasing NW doping density. By moving to nanowires with large radii, the sensitivity of NW JL ISFET is decreasing. This is because, in nanowire with a large radius, the channel conductivity is no longer controlled by the solid surface/electrolyte gating potential. Also, the maximum sensitivity is achieved for nanowires with a radius of less than 20 nm.

References

[1] M. Noor, and U. Krull, "Silicon nanowires as field-effect transducers for biosensor development : a review," Anal. Chim. Acta, vol. 825, pp. 1–25, 2014.

[2] A. Yesayan, F. Jazaeri, J.M. Sallese, "Analytical modeling of double-gate and nanowire junctionless ISFETs" - IEEE Trans. Electron Devices, vol. 67 (3), pp. 1157-1164, 2020.

[3] A. Yesayan, F. Prégaldiny, and J. M. Sallese, "Explicit drain current model of junctionless double-gate field-effect transistors," Solid. State. Electron., vol. 89, pp. 134–138, 2013.

Compact Device Modeling and Simulation with Qucs/Qucs-S/Xyce Modular Libraries

Mike Brinson
Centre for Communications Technology
London Metropolitan University
UK
Email: mbrin72043@yahoo.co.uk

Felix Salfelder
School of Computing
University of Leeds
UK
Email: felix@salfelder.org

EXTENDED ABSTRACT

The continuous development of semiconductor materials and devices has for some time been a catalyst driving improvements in compact modelling and circuit simulation. Increasing numbers, and indeed the diversity of emerging technology devices, implies that future modelling and simulation tools must allow users to select only those models applicable to specific design or simulation tasks. Previous and current generations of circuit simulators provide at least a minimal set of component and device models based on SPICE [1] [2]. These are considered to be an industrial baseline standard. Over time new models have been added or existing model features extended. The adoption of Verilog-A has both simplified and standardised compact model construction [3]. However, adding significant numbers of new models to a circuit simulator does increase the size and complexity of the software, which in turn makes code maintenance more onerous. One solution to this trend is to release circuit simulators with libraries of predefined models that can be loaded as needed.

With legacy Qucs [4] divided into a library and optional plugins, new possibilities will arise in applications based on Qucs. One of the motivations behind Qucs-S is to run SPICE simulators. Any two SPICE implementations are slightly different, and hence plugins supporting one will pave the way to add any other in the long run. In this work, we focus on use cases that make use of Xyce as a simulation engine. These extensions will be implemented in turns, either derived from existing plugins, ported from Qucs-S or implemented from scratch. The block diagram diagram drawn in Fig. 1 outlines how the modular approach to Qucs will facilitate the integration of those features. This paper introduces a user-defined/plugin toolkit library for constructing and simulating new device models from linear and non-linear building blocks, where their properties are defined by netlists and Verilog-A modules plus a unified set of schematic drawing symbols. The toolkit has been implemented with the Qucs-S/Xyce [5][6] package as a user-defined library. It will also be available as a plugin for the next generation Qucs modular circuit simulator [7]. To illustrate the toolkit properties its structure, modeling features, and applications are described. A number of Qucs-S/Xyce compact device models plus simulation test benches are also included, and their performance discussed.

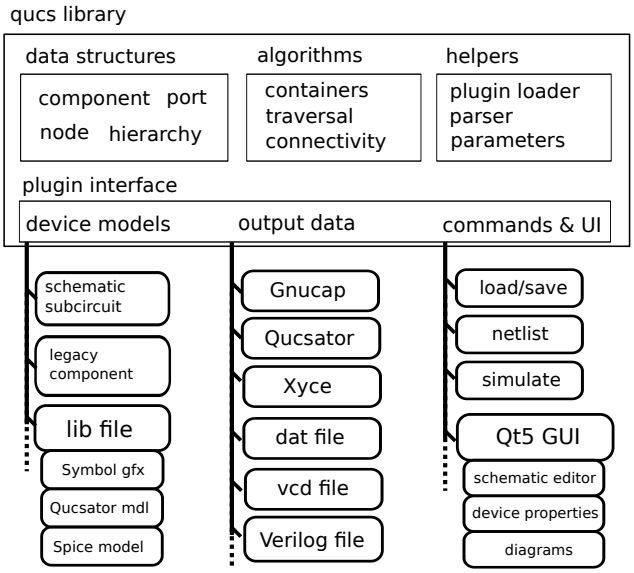


Fig. 1. Modular Qucs, structural view. A slim library provides circuit modeling essentials and infrastructure for extensions. Replaceable plugins (in rectangles with rounded corners) add further functionality that may be application specific and usually involves choices.

REFERENCES

[1] A.R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, "SPICE Version 2g User's Guide", Department of Electrical Engineering and Computer Sciences, University of California: Berkeley, CA. 1981.
[2] B. Johnson, T. Quarles, A.R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, "SPICE3 Version 3f User's Manual", Department of Electrical Engineering and Computer Sciences, University of California: Berkeley, CA. 1992.
[3] Accellera, "Verilog-AMS Language Reference Manual, version 2.2", available from: http://www.accellera.org, [Accessed April 2021].
[4] Sourceforge, Qucs project: Quite Universal Circuit Simulator, Available qucs.sourceforge.net. [accessed April 2021].
[5] V. Kusnetsov and M. Brinson, "Qucs-S: Qucs with SPICE". Version 0.0.22, https://ra3xdh.github.io/, 2020. [Accessed April 2021].
[6] Sandia National Laboratories, "Xyce Parallel electronic simulator: version 6.8", 2015, https://xyce.sandia.gov/ [Accessed April 2021].
[7] F. Salfelder and M. Brinson, "A modular approach to next generation Qucs", 1st Asia/South Pacific MOS-AK Workshop, (virtual/online) Feb. 25-26, 2021.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Mechanical and Electrical Design Strategies for Flexible InGaZnO Circuits

Giuseppe Cantarella, Niko Münzenrieder, Luisa Petti
Faculty of Science and Technology
Free University of Bozen-Bolzano
39100 Bozen-Bolzano, Italy
giuseppe.cantarella@unibz.it

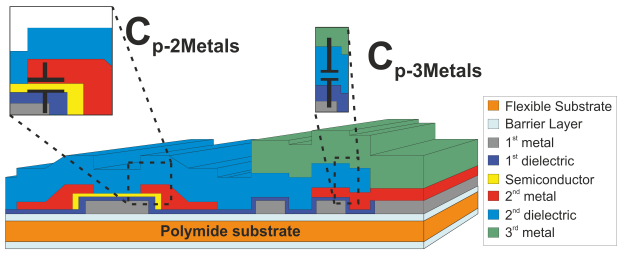
Koichi Ishida, Tilo Meister, Corrado Carta, Frank Ellinger
Chair of Circuit Design and Network Theory
TU Dresden
01069 Dresden, Germany

Raoul Hopf
Institute of Mechanical System
Swiss Federal Institute of Technology
8092 Zurich, Switzerland

SUMMARY

Thin-film transistors (TFTs) and circuits based on oxide semiconductors fabricated on flexible plastic foils and stretchable substrates are reported. Reliable fabrication protocols, using InGaZnO as n-type semiconductor, in combination with different design strategies, aiming at the improvement of both the electrical performance and the mechanical stability of such electronics, are discussed. First, simulation models are used to guide the fabrication of operational amplifiers and logic circuits on flexible polyimide foil, using an additional third metal layer for the interconnections. Thanks to the reduced parasitic resistances and capacitances, the resulting circuits have yielded improved electrical performances with respect to a two-metals architecture. In particular, an increase of 5.7% of the Gain-Bandwidth-Product (GBWP) for operational amplifiers, and an average reduction of 22% of the rise times, fall times and propagation delays for digital circuits, were achieved. In parallel, Finite-Element Modeling (FEM) has supported the design of engineered stretchable substrates shaped with pillar (or mesa) structures. The reduction of the strain experienced by the electronics, located on the mesa surfaces, during stretching, bending, and twisting, resulted in highly flexible digital circuits with functionality up to 20% elongation.

a)



b)

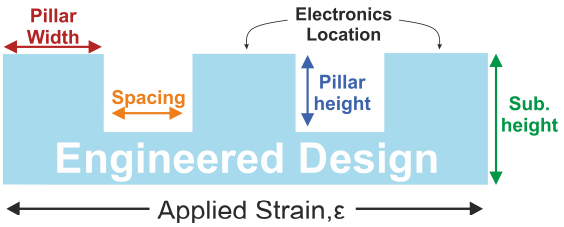


Figure. (a) Graphical representation of flexible InGaZnO based circuits fabricated with three-metals architecture, aiming at improved electrical performances; (b) engineered substrate with pillar (or mesa) structures for the realization of stretchable InGaZnO based electronics.

REFERENCES

[1] L. Petti, N. Munzenrieder, C. Vogt, H. Faber, L. Buthe, G. Cantarella, *et al.*, "Metal oxide semiconductor thin-film transistors for flexible electronics," *Applied Physics Reviews,* vol. 3, Jun 2016.

[2] G. Cantarella, C. Vogt, R. Hopf, N. Münzenrieder, P. Andrianakis, L. Petti, *et al.*, "Buckled thin-film transistors and circuits on soft elastomers for stretchable electronics," *ACS applied materials & interfaces,* vol. 9, pp. 28750-28757, 2017.

[3] G. Cantarella, K. Ishida, L. Petti, N. Münzenrieder, T. Meister, R. Shabanpour, *et al.*, "Flexible In–Ga–Zn–O-based circuits with two and three metal layers: simulation and fabrication study," *IEEE Electron Device Letters,* vol. 37, pp. 1582-1585, 2016.

[4] R. Shabanpour, T. Meister, K. Ishida, B. Boroujeni, C. Carta, F. Ellinger, *et al.*, "A transistor model for a-IGZO TFT circuit design built upon the RPI-aTFT model," in *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2017, pp. 129-132.

[5] G. Cantarella, V. Costanza, A. Ferrero, R. Hopf, C. Vogt, M. Varga, *et al.*, "Design of engineered elastomeric substrate for stretchable active devices and sensors," *Advanced Functional Materials,* vol. 28, p. 1705132, 2018.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Modelling Challenges for Enabling High Performance Amplifiers in 5G/6G Applications

Nagaditya Poluri, Maria Merlyne DeSouza
Electrical and Electronics Engineering
The University of Sheffield, Sheffield, UK
m.desouza@sheffield.ac.uk

Nivedhita Venkatesan, Patrick Fay
Dept. of Electrical Engineering
University of Notre Dame, Notre Dame, IN USA

Extended Abstract

High efficiency broadband power amplifiers (PA) are critical for the realization of Fifth-generation (and beyond) mobile communications networks. Accurate modelling of the transistor in the PA is one the main challenges to achieving high performance. In the frequency range from 20-50 GHz, GaN HEMTs have demonstrated efficiency comparable to or better than Silicon CMOS, SiGe HBT, GaAs pHEMT, but at a higher output power [1]. This can be attributed to the high-breakdown voltage capability of GaN that can be exploited in continuum mode amplifiers which rely on harmonic tuning that results in high efficiency broadband performance. An accurate model of the transistor up to the third harmonic is a necessity for exploiting these amplifier classes.

In this work, we present the considerations and challenges associated with modelling the device, and in particular the impact of extrinsic parasitics, for operation at high frequencies. We focus on empirical models (i.e., equivalent circuit-based models) that offer a compromise in terms of simplicity, ease of implementation, accuracy and usefulness for circuit design. A modified version of the extraction procedure for the intrinsic parasitics by Dambrine, Flores, and Lin is implemented for frequencies less than 6 GHz to extract the parasitic elements of the device model in Fig. 1. The non-linear intrinsic capacitances are extracted from S-parameters of the device at multiple bias points. For each bias point, the extrinsic elements are de-embedded from it's S-parameters, as illustrated by Dambrine. The extraction process relies on the combination of the analytical and curve-fitting based approaches. For fine tuning

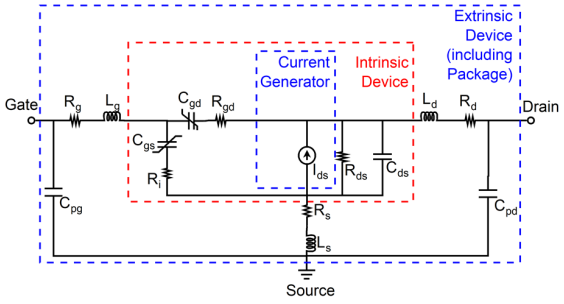


Fig. 1. The equivalent circuit of a GaN HEMT up to 6 GHz.

the extracted parasitic values, rather than optimizing all the components in a single step, we partition the optimization problem into steps, based on the relative sensitivity of the S-parameters to the particular elements. The S-parameters of the extracted equivalent model after optimization and the vendor model over the frequency range 0.5 GHz to 6 GHz, plotted in Fig. 2, are in close agreement.

We demonstrate the utility up to 80 GHz by application in the extraction of a simulated GaN HEMT. The S-parameters of the extracted equivalent model after optimization and the TCAD simulation over the frequency range 0.1 GHz to 80 GHz, compared in Fig. 3, show a close match. Owing to its simplicity the applicability to high frequencies eases modelling effort.

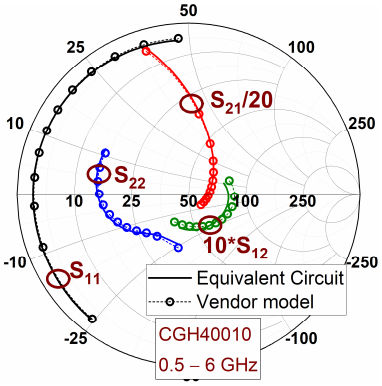


Fig. 2. Comparison of the S-parameters of the equivalent model after optimization with the S-parameters of vendor model of CGH40010 at V_{dsq}=28 V and I_{dsq}=150 mA.

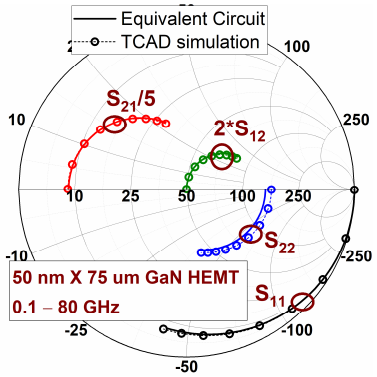


Fig. 3. Comparison of the S-parameters of the equivalent model after optimization with the S-parameters from the TCAD simulation of a 50 nm X 75 µm GaN HEMT at V_{dsq}=5 V and V_{gsq}=-2.3 V.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Simulation and Modeling Methodologies: Enabler for Neuromorphic Computing Applications

Mike Schwarz
NanoP, Technische Hochschule Mittelhessen - University of Applied Sciences, Germany
Email: mike.schwarz@ei.thm.de

***Abstract*—Neuromorphic computing is of worldwide interest. Compared to the von Neumann's computer architecture, neuromorphic systems offer advantages and novel approaches for artificial intelligence problems to be solved. Inspired by biology, neuromorphic systems adopt the theory of the human brain modeling by implementing neurons and synapses with the help electronic devices and circuits. Many researchers developed new algorithms, learning approaches, models, etc., implement them into hardware to explore the neuromorphic system. However, many of the promising approaches concentrate on the realization not taking into account the feasibility for industrial or consumer application of the various concepts. In this paper we would like to draw the attention of the reader why it makes sense to use the support of predictive simulations and why it is so important to push the development of simulation and modeling for neuromorphic computing systems.**

***Keywords*—artificial intelligence, framework, modeling and simulation methodologies, neuromorphic computing**

I. Introduction

Nowadays, neuromorphic computing is an emerging field due to several aspects, e.g. computing cognitive tasks [1]. Contrary to the von Neumann architecture, the neuromorphic computing tries to mimic the human brain [2], [3].

Taking hundreds of neurons and several layers into account, computation of such networks are hungry in terms of power consumption for software realizations with digital electronics. Even for GPU implementations [4] which overcome the bottleneck of classical CPU by huge parallelism require a lot of power. These reasons are the main driver for bringing the power hungry software realization into hardware.

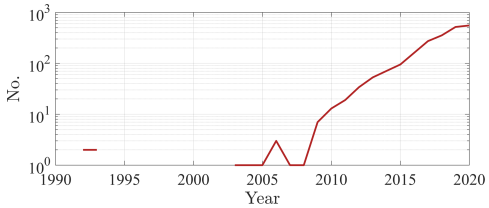


Fig. 1. Number of papers for "neuromorphic computing" in log-scale via Semantic Scholar (access/search on 23.11.2020).

The realization of such systems requires devices to mimic the neural and synaptic behavior. Several candidates are in the scope, e.g. memristive devices such as memristors, non-volatile memory (NVM) technologies as resistive random access memories (RRAM), phase change memory, or valence change memory effects, etc. aligned in crossbar arrays [2], [5]–[10].

The simulation and modeling is one of the key components within the development process of new neuromorphic computing devices, architectures, and applications. It bridges the physics, e.g. the physical process, process development, electronic circuit(s), ASIC interface, etc. Knowing the interaction of tolerances and variability between the various process parameters and system components allows to concentrate on the potential technology for neuromorphic computing applications.

To draw attention of the reader for the demand of simulation and modeling methodologies one notice the amount of papers published the last decade regarding "neuromorphic computing", see Figure 1, a term which was coined in 1990 by Carver Mead [11]. Furthermore, one can clearly see the growth of interest after the announcement of the memristor by Strukov et al. in 2008 [12] and proposed by Leon Chua in 1971 [13].

References

[1] R. P. Würtz, "Organic Computing," *Springer*, 2008.
[2] R. Waser, et al., "Introduction to nanoionic elements for information technology," in Resistive Switching, edited by D. Ielmini and R. Waser, *Wiley-VCH Verlag GmbH & Co. KGaA*, 2016.
[3] E. Kandel, et al., "Principles of Neural Science, 5th ed.," *McGraw Hill Professional*, 2013.
[4] R. Raina, et al., "Large-scale Deep Unsupervised Learning using Graphics Processors," *Computer Science Department, Stanford University*, 2009.
[5] C. Wenger, et al., "Inherent Stochastic Learning in CMOS-Integrated HfO2 Arrays for Neuromorphic Computing," *IEEE Electron Device Letters 40(4)*, 2019.
[6] H. Y. Jeong, et al., "Graphene oxide thin films for flexible nonvolatile memory applications," *Nano Letters 10(11)*, 2010.
[7] J. S. Seo, et al., "A 45nm CMOS neuromorphic chip with a scalable architecture for learning in networks of spiking neurons," *2011 IEEE Custom Integrated Circuits Conference (CICC)*, 2011.
[8] K.-H. Kim, et al., "A Functional Hybrid Memristor Crossbar-Array/CMOS System for Data Storage and Neuromorphic Applications," *Nano Letters 12 (1)*, 2012.
[9] H. Y. Chen, et al., "HfOx based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector," *2012 International Electron Devices Meeting*, 2012.
[10] S. Ambrogio, et al., "Spike-timing dependent plasticity in a transistor-selected resistive switching memory," *Nanotechnology 24(38)*, 2013.
[11] C. Mead, "Neuromorphic electronic systems," *Proceedings of the IEEE 78(10)*, 1990.
[12] D. B. Strukov, et al., "The missing memristor found," *Nature 453(7191)*, 2008.
[13] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory 18(5)*, 1971.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Variability-Aware Characterization of Current Mirrors Based on Organic Thin-Film Transistors on Flexible Substrates

Aristeidis Nikolaou[1,2], Jakob Leise[1,2], Jakob Pruefer[1,2], Ute Zschieschang[3], Hagen Klauk[3], Ghader Darbandy[1], Benjamin Iñiguez[2], Alexander Kloes[1]
[1] NanoP, TH Mittelhessen University of Applied Sciences, 35390 Giessen, Germany
[2] DEEEA, Universitat Rovira i Virgili, Tarragona, Spain
[3] Max Planck Institute for Solid State Research, Stuttgart 70569, Germany
aristeidis.nikolaou@ei.thm.de

Extended abstract

In the current paper, the variability of the electrical characteristics of current-mirror circuits based on organic thin-film transistors is investigated. Typically, the variability analysis of organic TFT-based circuits is performed using Monte Carlo simulations, accurate physics-based variability compact models [1] or novel noise-based simulation approaches [2]. The experimental data based on which the impact of variability on the circuit characteristics is analyzed are usually obtained exclusively at the device level, i.e., from the transistors. Here, we analyze the variability of analog organic-TFT-based circuits by considering experimental data acquired not only from a large number of discrete organic TFTs, but in addition from a large number of TFT-based current mirrors.

For this purpose, a large number of nominally identical TFTs and nominally identical current mirrors were fabricated and characterized (Fig. 1). For the discrete TFTs, the expected behavior of the bias-dependent drain-current variability was confirmed [1]. The statistical behavior of the TFT-based current mirrors, quantified here in terms of the mean value and the standard deviation of the reference and output currents, are similar to those of the discrete TFTs. The drain-current mismatch of the current-mirrors is fluctuating from 1% to 25% depending on the dimensions of the circuit transistors and the circuit biasing conditions (Fig. 2).

References

[1] A. Nikolaou, G. Darbandy, J. Leise, J. Pruefer, J. W. Borchert, M. Geiger, H. Klauk, B. Iñiguez, and A. Kloes, "Charge-based model for the drain-current variability in organic thin-film transistors due to carrier-number and correlated- mobility fluctuation," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4667–4671, 2020.
[2] A. Nikolaou, J. Leise, J. Pruefer, U. Zschieschang, H. Klauk, G. Darbandy, B. Iñiguez, and A. Kloes, "Noise-based simulation technique for circuit-variability analysis," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 450–455, 2021.

This project is funded by the German Federal Ministry of Education and Research ("SOMOFLEX", No. 13FH015IX6) and the German Research Foundation (DFG) under the grant KL 1042/9-2 (SPP FFlexCom). We would like to thank AdMOS GmbH for support.

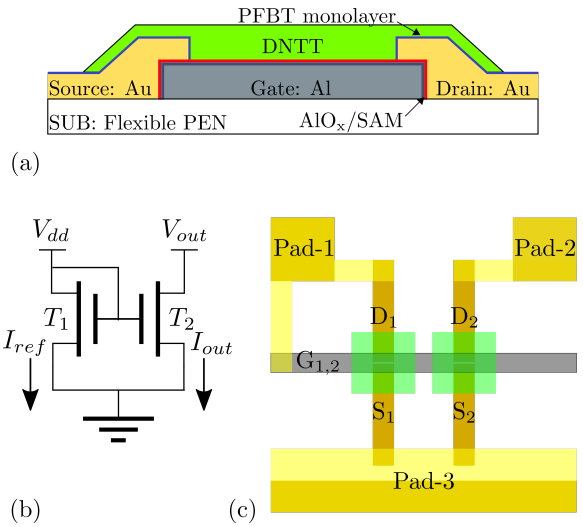


Figure 1. (a) Cross-section of the organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) architecture. (b) Schematic and (c) layout of a current mirror comprised of two nominally identical p-channel TFTs with a channel width (W) of 50 µm and a channel length (L) of 5 µm.

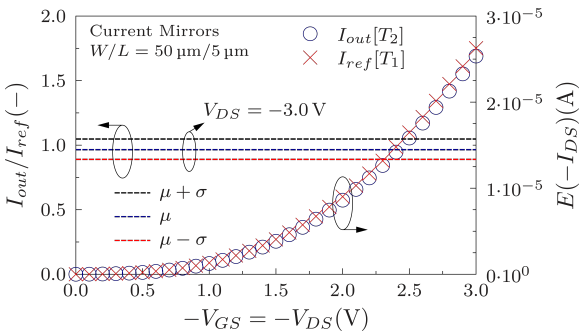


Figure 2. Symbols: Mean value drain current $E[-I_{DS}]$ of the reference TFT ($I_{ref}[T_1]$) and of the output TFT ($I_{out}[T_2]$) employed in the current mirrors. Dashed lines: Mean-value μ and corner-value $\mu \pm \sigma$ characteristics of the parameter I_{out}/I_{ref} at the maximum gate-source and drain-source voltages ($V_{GS} = V_{DS} = -3.0V$).

Fusion Diagnostics I&C

Evaluation of Nvidia Xavier NX Platform for Real-Time Image Processing for Fusion Diagnostics

Bartlomiej Jablonski, Dariusz Makowski, Piotr Perek
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
jablonskiba@dmcs.pl

EXTENDED ABSTRACT

Real-time image processing is the core component of image plasma diagnostics. Efficient algorithms enable machine protection, contributing to future steady-state operation in nuclear fusion devices. The paper evaluates the applicability of the newest low-power Nvidia Jetson Xavier NX platform (see Fig. 1) for fusion diagnostics.

This embedded Nvidia Tegra System-on-a-Chip (SoC) integrates a Graphics Processing Unit (GPU) and Central Processing Unit (CPU) on the single chip. General-Purpose Computing on Graphics Processing Units (GPGPU) provides high parallelism that is advantageous in image-based calculations. It is especially beneficial in Wendelstein 7-X (W7-X) diagnostics that operate on full-width frames instead of small Region-of-Interests (ROIs). The hardware differences in comparison to the previous Nvidia Jetson TX2 based on Pascal architecture, including innovations introduced in the Volta architecture for Nvidia Tegra, are signified. The evaluation is performed on the W7-X stellarator experimental data. Implemented algorithms visualise, segment and detect thermal events in real-time utilising the embedded GPU. Investigated thermal events are strike-lines, overload hotspots, reflections and surface layers (see Fig. 2 and Fig. 3).

Their detection allows the automated real-time risk evaluation incorporated in the feedback plasma control and interlock systems in the W7-X. The speedup resulting from the upgrade to the Xavier NX platform is presented in the paper, along with techniques pertaining to key hardware differences and programming aspects specific to the Nvidia Tegra facilitating real-time computing on the low-power embedded device.

Fig. 1. Nvidia Jetson Xavier NX Developer Kit

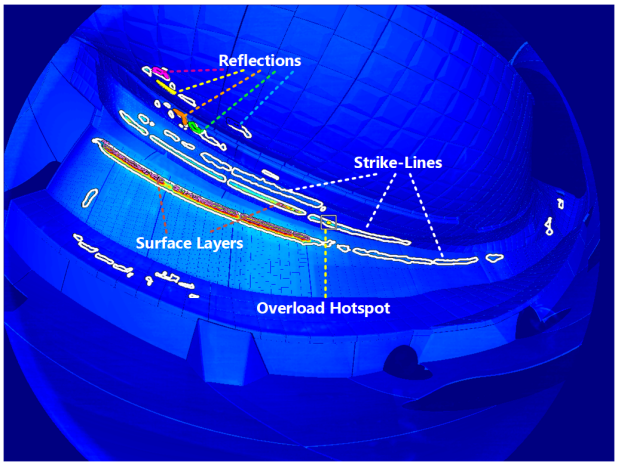


Fig. 2. Detected thermal events in 20171114.053 (AEF20) dataset

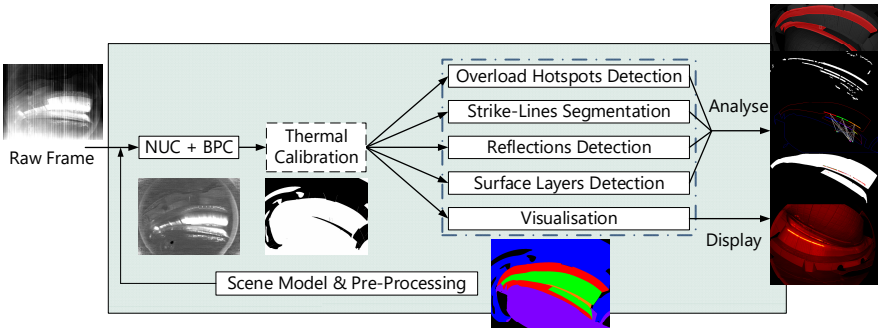


Fig. 3. Implemented image processing pipeline with evaluated sections marked with a blue outline

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Low-noise Amplifier for Photomultiplier Tube Detectors for Plasma Diagnostics

Patryk Nowak vel Nowakowski, Dariusz Makowski, Aleksander Mielczarek
Lodz University of Technology
Lodz, Poland
(nowakow, dmakow, amielczarek)@dmcs.pl

Extended Abstract

Photomultiplier Tube (PMT) detectors are commonly used for plasma diagnostics in fusion devices such as tokamaks or stellarators. These detectors measure spectrum of soft and hard X-ray radiation. Modern spectroscopy systems use Digital Pulse Processing (DPP) in contrary to analogue systems [1]. Scintillator used together with PMT converts X-ray radiation to electrical signal. PMT is superior in response speed and detection of low-light-level sources such as single photons [2]. This type of sensor is often used in application that rely on fast digital pulse processing.

Low output voltage level is the main concern when dealing with PMT. Depending on supplied biasing voltage the output voltage of pulse coming out of PMT can be in range of mV or even lower [2]. Such low output voltage levels require low-noise amplification to keep good signal to noise ratio (SNR) before digitalisation. Fall-time of pulses coming from PMT can be as low as 1 ns, that require amplifier to have respectively bandwidth of at least 300 MHz. What is more large size fusion devices such as ITER tokamak require sensitive electronic device to be placed far away from reactor due to high radiation and magnetic field levels. PMT assembly has to be installed ca. 20 m away from reactor, then signal is sent for long distance reaching over 100 m using coaxial cables. Amplifier have to supply power to drive signal over such long distance. Environment near fusion reactor is heavily polluted by strong magnetic fields and electromagnetic noise. Electromagnetic interferences can couple into signal cables. Cable should be well shielded and amplifier ought provide high amplitude output, to assure high signal-to-noise ratio. Therefore, sending fast analogue signal from PMT via long coaxial cable is a challenging task.

Due to ITER specification a dedicated Photomultiplier Tube amplifier is required. A suitable ultra low-noise amplifier with 300 MHz bandwidth, gain of at least 100x (with possible adjustment), high voltage output and which will be able to drive long coaxial cables is required. Market search was carried to find amplifier suitable for low-noise application and fulfilling requirements ITER specification. Various available solutions were considered, but none of them did meet all requirements at once. Finally, low-noise two stage amplifier was designed from scratch to meet all specification required by PMT-involved applications. Paper discusses how to design a low noise amplifier suitable for Photomultiplier Tube applications. Characteristics and measurements of the prototype are presented in this paper.

After evaluation and simulation of different amplifier circuits, two-stage topology has been chosen, as it allow to achieve wide bandwidth, high output voltage and yet be low noise. Amplifier is based on ultra low-noise preamplifier ($0.69\ nV/\sqrt{Hz}$) and high power second stage amplifier (output voltage swing 28 Vpp). Amplifier circuit board is enclosed in aluminium RF-sealed enclosure to protect circuitry from electromagnetic interferences. The first prototype of the PMT amplifier was developed and evaluated at Department of Microelectronics and Computer Science (DMCS). After series of tests and tuning of the prototype, device was finally connected to PMT. Developed amplifier will be used in ITER Hard X-Ray Monitor diagnostic system.

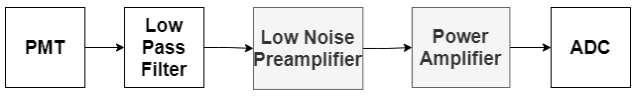


Fig. 1. HXRM chain

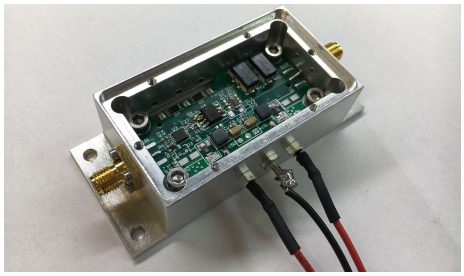


Fig. 2. PMT amplifier prototype

References

[1] I. Hafizh, M. Carminati, C. Fiorini, Assessment of analog pulse processor performance for ultra high-rate x-ray spectroscopy, Nuclear Inst. and Methods in Physics Research, 2019
[2] A. G. Wright, *The Photomultiplier Handbook*, Oxford University Press, 2017.

Novel ANC Simulation Based on VSSLMS Method for Reducing the Microphonics Effects in Cavities

Fatemeh Abdi, Wojciech Cichalewski, Wojciech Jalmuzna, Andrzej Napieralski
Microelectronics and Computer Science Department
Lodz University of Technology
Lodz, Poland
Email: Fatemeh.abdi@dokt.p.lodz.pl, wojciech.cichalewski@p.lodz.pl, wjalmuzn@dmcs.pl, napier@dmcs.pl

Extended Abstract

The microphonics vibrations inside cryomodules are coupled into the cavity walls, leading to transient deformations in its shape. In the paper, the main goal of the presented method is to reduce the microphonics effects in the superconducting cavities. The main error sources are the vacuum pumps at the cryomodule test bench (CMTB) at DESY. The microphonics, related to the vacuum pumps, are narrow bandwidth and concentrated below 100 Hz, exact propagation in the cryomodule vary from a cavity to another cavity [1]. A novel adaptive controller based on variable step size least mean squares (VSSLMS) method has been presented to reduce the microphonic vibrations that are created in cavities environment. We presented two methods for identifying and estimating the microphonics effects:

1) The active noise control (ANC) with the VSSLMS algorithm.
2) The narrowband active noise control (NANC) algorithm with the VSSLMS algorithm [2].

The adaptive filters have been implemented to identify the mechanical vibrations in different frequencies and to adapt the filter coefficients based on the changes of the detuning signal at the system. The main idea is to improve the performance of the ANC and the NANC methods by changing the step size based on tracking the sign of the error signal. The main features of the proposed method are:

1) An improved VSS method to achieve better performance in convergence rate and steady-state MSE when the algorithm is at a low SNR environment and also has maintained low computational complexity.
2) The VSS method is applied to update the coefficients of the primary path and the coefficients of the secondary path in the NANC algorithm.
3) The auxiliary noise is scaled with the magnitude of one-sample-delayed residual noise and leads to a significantly improving convergence rate of the overall NANC system.
4) The sign of the error signal has been used to calculate the VSS method which makes the algorithms intrinsically sensitive to the measurement noise.

Simulation Result

In simulation section, we simulated the other two methods for comparing with the presented methods. In Fig. 1, the error signal indicates that the proposed method can track the system changes faster than the simple LMS algorithm and the conventional VSSLMS algorithm. The results show that the error signal (red-line) reaches zero in a shorter time than other algorithms. This means that the presented method identifies detuning signal variations faster and has higher tracking abilities. In Fig. 2, the error signals are compared between the NANC algorithm and the ANC algorithm based on the VSSLMS method. At the beginning of the identification, the NANC algorithm with the method mentioned identifies the changes of the detuning signal faster and has no spikes after identification of the changes.

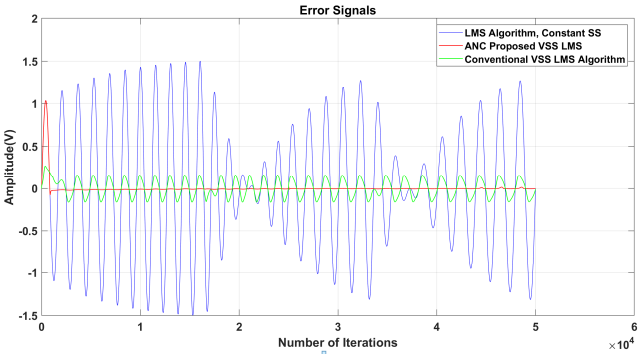


Fig. 1. Compare between the error signal in three methods.

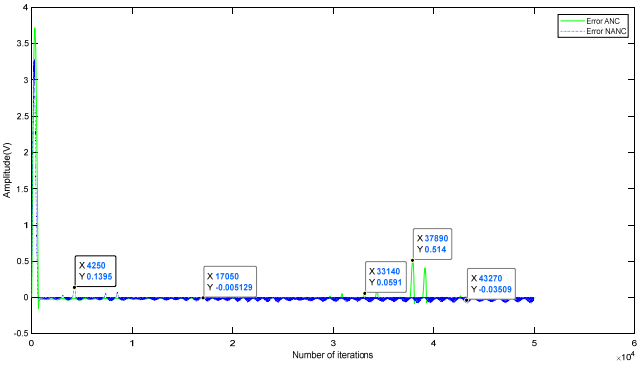


Fig. 2. Compare the error signals in the NANC algorithm and the ANC method with VSSLMS algorithm in each LMS block.

References

[1] R. Rybaniec, K. Przygoda, W. Cichalewski, V. Ayvazyan, J. Branlard, Ł. Butkowski, "FPGA-Based RF and Piezo controllers for SRF Cavities in CW Mode", in IEEE Transactions on Nuclear Science, vol. 64, no. 6, pp. 1382-1388, June 2017.

[2] S. Bose, Arijit De, and I. Chakrabarti, "Framework for Automated Earthquake Event Detection Based on Denoising by Adaptive Filter," IEEE Transactions on Circuits and System, 2020.

Design of Integrated Circuits and Microsystems

A New High-Speed and Low Power Synchronous Up/Down Counter

Mehdi Ghasemzadeh
Department of Microelectronic Research Laboratory
Urmia University, Urmia, Iran
M.Ghasemzadeh@urmia.ac.ir

***Abstract*—A high speed and low power up/down counter is proposed in this paper with the ability of up and down counting at the same time. For this reason, straight forward circuit architecture is adopted for the counter. This counter has been simulated in TSMC 0.18µm CMOS process with 1.8 V as power supply. The post layout results show that an 8-bit resolution is feasible for the maximum operating frequency of 3.34 GHz with the power dissipation of 946 µW. The layout of the proposed counter occupies about 0.025mm^2 of the chip area.**

***Keywords*—up/down counter, level crossing ADC, synchronous counter, PLL**

EXTENDED ABSTRACT

In this paper, a new architecture is proposed for an Up/Down counter which uses a novel count-up and count-down method based on universal multiplexer structure. The counter is suitable for random counting with ability to follow the signal at any moment correctly.

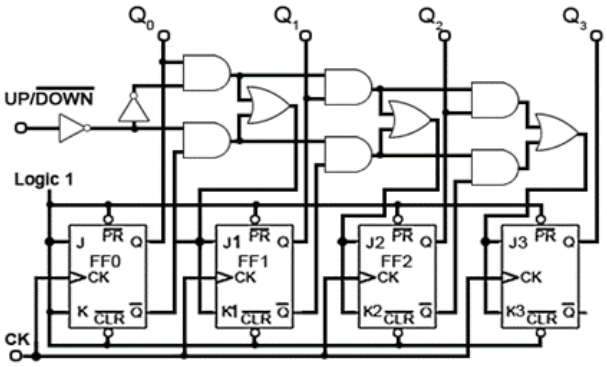


Fig. 1. 4Bit conventional synchronous an up/down counter

The point of attraction of this paper as a cornerstone is the simplicity of the circuit design and the simplicity of up and down counting. Fig 2 depicts the block diagram of one bit of the proposed programmable counter which consists of four main modules including half-adder (H.A), half subtractor (H.S), DFF and 4:1 MUX. The proposed up/down counter is synchronous with a clock active on the rising edge.

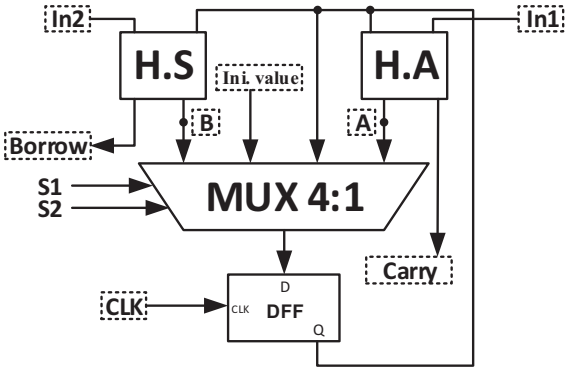


Fig. 2. One bit of proposed An Up/Down counter structure.

TABLE I. MULTIPLEXER OPERATION

S_0	S_1	Q(t+1)
0	0	Q(t)+1
0	1	Q(t)
1	0	New input
1	1	Q(t)-1

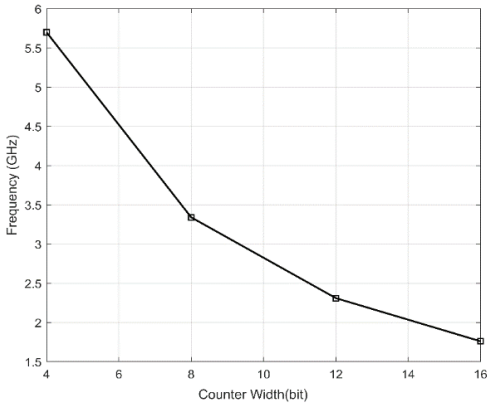


Fig. 3. Worst-case maximum clock frequency verses counter width (size) in bits

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

A W-band SiGe BiCMOS I/Q Receiver with Tunable Conversion Gain for Radar Applications

Maciej Kucharski[1], Michał Widlok[1], Paweł Bajurko[2], Radosław Piesiewicz[1]
[1] SIRC Sp. z o.o., ul. Sobieskiego 47, 84-230 Rumia, Poland
[2] Warsaw University of Technology, Institute of Radioelectronics and Multimedia Technology
ul. Nowowiejska 15/19, 00-665 Warszawa, Poland
Email: m.kucharski@si-research.eu, m.widlok@si-research.eu, P.Bajurko@ire.pw.edu.pl, r.piesiewicz@si-research.eu

Extended Abstract

This paper presents an 89-102 GHz I/Q receiver (RX) containing an LO frequency multiplying chain (×4) manufactured in SiGe BiCMOS technology. The RX entails a two-stage low-noise amplifier (LNA) followed by a lumped version of Wilkinson power splitter to feed two mixers driven by LO signals shifted by 90 degrees. Quadrature LO signals are generated using a reduced-size branchline coupler. The mixing stage enables conversion gain (CG) tuning in 13.2-26.8 dB range at 94 GHz by means of pMOS transistors biased in triode region. The RX provides 13 GHz 3-dB bandwidth with peak CG of 26.8 dB and NF of 11.7 dB consuming 80 mA from 3.3 V supply. The chip occupies 1.07 mm^2 silicon area.

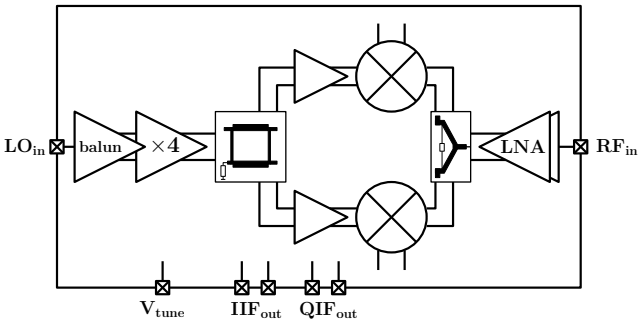


Fig. 1. Block diagram of W-band I/Q receiver.

Block diagram of the W-band RX is depicted in Fig. 1. A K-band LO signal is up-converted to W-band using a frequency multiplying chain containing two cascaded frequency doublers. A branchline coupler is used to produce quadrature LO signals driving the mixers with tunable load via V_{tune} voltage. The RF input signal is amplified by a two-stage LNA and split using a Wilkinson divider. The RX was fabricated using SG13S BiCMOS process from IHP. For measurement purposes the RX IC was mounted on a dedicated PCB with all DC and IF outputs connected to the board using aluminum bondwires. The RX characterization was performed in the Antenna and Sub-terahertz Technology Laboratory at Warsaw University of Technology. Fig. 2 presents CG versus mixer

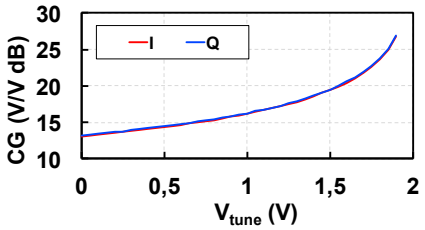
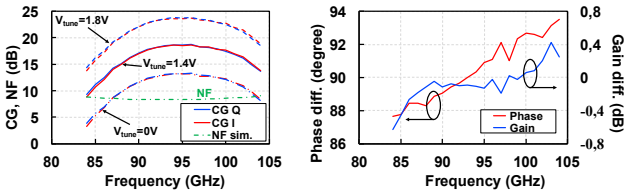


Fig. 2. RX CG against V_{tune} at 94 GHz.

load tuning voltage V_{tune}. The realized CG tuning range spans from 13.2 dB to 26.8 dB for I and Q channel, respectively. CG over the frequency for selected V_{tune} settings is presented in Fig. 3a. The gain of I and Q channel is well balanced in 84-104 GHz range. The RX achieves 3-dB bandwidth of 13 GHz in 89-102 GHz range for V_{tune}=1.8 V. The I/Q balance-relevant parameters are presented in Fig. 3b. The gain difference between the channels is below 0.2 dB and the phase deviation from 90 degrees does not exceed 2.5 degree in 87-102 GHz range.



(a) (b)

Fig. 3. (a) Measured TX output power versus frequency. (b) Measured TX output power versus frequency.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Analysis the Effect of Transit Capacitances in Fully Differential Operational Transconductance Amplifiers

Ivan Uzunov
PDK Services Bulgaria EAD
GlobalFoundries Inc.
Sofia, Bulgaria
ivan.uzunov@globalfoundries.com

Boncho Nikov
Advanced Solutions Group
On Semiconductor
Zürich, Switzerland
boncho.nikov@onsemi.com

EXTENDED ABSTRACT

The analysis of fully differential (FD) analog circuits is more complicated and often it is done by using their single-ended counterparts, which usually are received by grounding an input and an output terminal of the fully differential devices. In most of the cases this approach works, however there are cases when it can cause a confusion if it is not applied carefully. An example is the analysis of the effect of transit capacitances of single-stage operational transconductance amplifiers (OTA) – such grounding removes at least one of the transit capacitances. Usually the effect of these capacitances is approximated by negative real zero in the expression for OTA transconductance, however is correct only when OTA output is close to short circuited.

Two equivalent single-ended circuits for transit capacitances of FD OTA are proposed in the paper - for inverting and for noninverting OTA. Of course, when FD OTA is used alone, is it inverting or not is conditional; however when it is included in more complicated circuit with feedbacks, it does matter. Both equivalent circuits are shown in Fig. 1 and 2. Both equivalent circuits preserve the current, flowing through transit capacitances. If take the inverting FD OTA in Fig. 1(a) and ground the nodes "i2" and "o1" the remaining transit capacitance will be C_t, while its correct value should be $C_t/2$ as it is in the model in Fig. 1(b).

Transit capacitances have effect mainly in single-stage FD OTA realized as differential amplifiers or as pairs of inverters. Their values could be in the range of OTA input capacitance, as it is shown by an example in the paper.

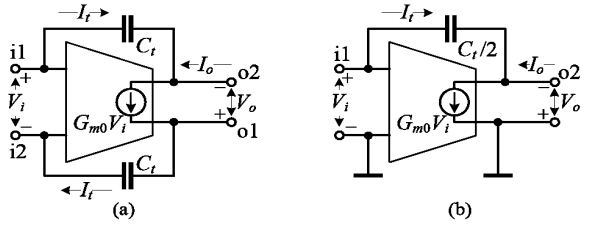


Fig. 1. (a) Inverting FD OTA with transit capacitances; (b) its single-ended model.

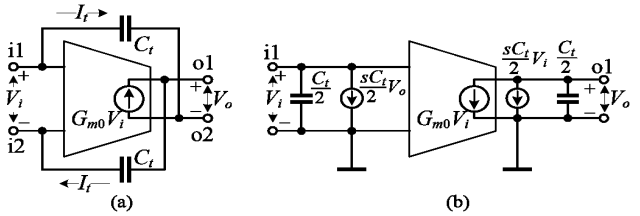


Fig. 2. (a) Non-inverting FD OTA with transit capacitances; (b) its single-ended model.

The use of the proposed equivalent circuits is demonstrated for analyzing the effect of the transit capacitances in two simple examples. Firstly is considered a single OTA loaded by different loads: pure resistor, pure capacitance and parallel RC group. In all cases transit capacitances introduce a positive real zero and a real negative pole in the voltage gain. Transit capacitances change also OTA input impedance. It can be represented as series RC group when the load is a resistor; parallel RC group when the load is capacitor; and parallel RC group in series with another capacitor when the load is resistor in parallel with capacitor.

The second example is a FD gyrator resonance circuit. The analysis gives decreasing of the pole frequency and of the pole Q-factor by the same factor according the formulas

$$\omega_p = \frac{\omega_{p0}}{\sqrt{1+\frac{C_t}{C}}}; \quad Q_p = \frac{Q_{p0}}{\sqrt{1+\frac{C_t}{C}}};$$

where ω_{p0} and Q_{p0} are the corresponding parameters if transit capacitances are missing and C is the value of the capacitors, connected at both sides of the gyrator.

The examples demonstrate that the proposed single ended models are useful tool simplifying analysis of OTA transit capacitances in FD circuits. Evidently, the models can be generalized and can be used for analysis of circuits having FD OTAs with parallel impedances between their input and output terminals.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Class AB Operational Amplifier in CMOS 55 nm Technology

Paweł Pieńczuk
Łukasiewicz Research Network – Institute of Microelectronics and Photonics
Warsaw, Poland
pawel.pienczuk@ite.lukasiewicz.gov.pl

Witold A. Pleskacz
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Warsaw, Poland
W.Pleskacz@imio.pw.edu.pl

Mateusz Teodorowski
OmniChip Sp. z o.o.
Warsaw, Poland
mateusz.teodorowski@omni-chip.com

***Abstract*—A class AB operational amplifier, designed in UMC CMOS 55 nm technology, is presented. A folded-cascode architecture with a inverter output buffer was implemented. Post-layout corners and Monte Carlo simulations ensure the minimum bandwidth equal to 2 MHz and DC gain equal to 85 dB. Phase margin with a minimum of 67º ensures the stability of the circuit. CMRR and PSRR of at least 85.9 dB and 62.5 dB, respectively, allow the operational amplifier to be used in the majority of applications. The static current consumption does not exceed 25 µA. The die dimensions are 85 µm x 67 µm.**

***Keywords*—operational amplifier, AB class, folded cascode, CMOS, UMC, 55 nm.**

Extended Abstract

Operational amplifiers (op-amps) are among the most important components in analog CMOS circuit design. Class AB is a trade-off between linearity and power consumption. Complementary Metal Oxide Semiconductor (CMOS) technology is a low-cost and easily scalable fabrication process.

The presented op-amp is based on the folded-cascode architecture, which offers the trade-off between gain, speed, and power consumption [2]. The input differential amplifier is based on larger NMOS transistors to minimize the input offset. The active load has the form of a current mirror. The input differential pair is driven by a cascoded current source to maximize the common-mode rejection ratio (CMRR). The current source is mirrored by another transistor with external current port. The output buffer is a push-pull amplifier, performing the AB class operation. It is biased by a floating current source, which separates the gates of the output buffer. This reduces the crossover distortion and ensures the control of the output buffer.

The compensation consists of source followers and metal-insulator-metal (MIM) capacitors. This technique improves the compensation by moving the zero to a very high frequency. As a result, the phase margin (PM) is higher, therefore the size of the capacitors may be reduced or bandwidth improved. A dedicated biasing circuit supplies the appropriate voltages to the floating current source or cascode transistors. Biasing circuit consumes less than 5 µA.

The layout of the op-amp is created. The whole block was tested by the Design Rule Check (DRC) tool provided by Mentor®. The circuit passes also the Layout Versus Schematic (LVS) test. In the end, the parasitic extraction (PEX) and post-layout analyses were performed.

The circuit was designed and simulated using the Cadence® Virtuoso® environment. A corner analysis, including 3 supply voltages, 3 biasing currents, 3 temperatures and process corners was performed. Additionally, the Monte Carlo (MC) analysis was performed for each test, with N = 100 points and σ = 3. 12 tests were carried out to check the op-amp performance. The main parameters of the designed op-amp are listed in Table I. Much less current consumption and area is observed at the expense of slight decrease in op-amp performance.

In this work, a two-stage, AB class, folded-cascode operational amplifier with rail-to-rail output is presented. The circuit is designed in UMC CMOS 55 nm technology and is widely characterized across post-layout corners and Monte Carlo analyses. The compensation with source followers extends gain bandwidth. The design offers low power consumption (<25 µA), while keeping good bandwidth (>2 MHz) and DC gain (>85 dB). Good phase margin (with a minimum of 67º) provide the stability of the block. CMRR and PSRR are larger than 85.9 dB and 62.5 dB, respectively.

TABLE I
Main analysis results

Parameter	Min.	Typ.	Max.	Unit	Note
VDD	3.0	3.3	3.6	V	
Curr. Consumption	11.6	16.9	23.1	μA	
Unity Gain Freq.	2.01	4.26	12.1	MHz	
DC Gain	85.4	91.7	104	dB	
Phase Margin	66.6	80.0	94.4	º	
SR	0.99	1.77	3.48	V/μs	$C_L = 1pF$
Offset	-14.1	1.09	19.3	mV	MC
CMRR	85.9	88.0	119	dB	@ 1 kHz
PSRR	62.5	76.6	82.5	dB	@ 1 kHz
V_N	15.6	17.1	19.2	nV/$\sqrt{\text{Hz}}$	@ 1 kHz

MC — Monte Carlo Analysis Results
C_L — Load Capacitance
SR — Slew Rate
PSRR — Power Supply Rejection Ratio
CMRR — Common-Mode Rejection Ratio
V_N — Equivalent Input Noise Voltage

Exploiting Design Modularity and Relocation to Increase Productivity in FPGA-based Computing Systems

Zbigniew Mudza
Department of Microelectronics and Computer Science, Lodz University of Technology
Lodz, Poland

EXTENDED ABSTRACT

Long development cycles are a crucial disadvantage of FPGA-based systems. The author proposes an FPGA configuration development methodology for Xilinx 7 Series, aimed at increasing productivity in partially reconfigurable designs. The general idea is to separate static design and reconfigurable module development and use identical implementation results for multiple instances of the same module, regardless of their location. Identical relative placement and routing can be forced at another position by applying extracted results, relocated to a new position, as fixed placement and routing constraints. Module relocation is only possible provided that source and target partitions:

1. Share the same netlist.
2. Use partial reconfiguration compatible PBlocks.
3. Have identically arranged reconfigurable resources.
4. Do not allow global routing feed-through.
5. Have identical partition-to-static connections.
6. Do not use location-specific routing resources.

The requirements can be met using module isolation, partition ports buffering and strict design constraining.

If identical partition-to-static implementation results are used for all compatible partitions across multiple designs, reconfigurable modules and static designs can be not only developed but also implemented completely independently. A mock design with a single "empty" reconfigurable partition is used to implement the interface in various PBlocks. Obtained relative placement and routing results for all interface elements are then exported as parametrized constraints.

Synthesized reconfigurable modules are implemented using the same reference partition design and appropriate PBlock specific interface implementation. Relative placement and routing for individual modules is exported similarly to what is done for the interface. Independently a static design with multiple reconfigurable partitions can be implemented in target platform. For each partition fixed interface implementation based on reference partition results for appropriate PBlock is forced. Fully implemented static design is then used with different reconfigurable modules using Partial Reconfiguration Flow. Instead of individual implementation for each partition, reconfigurable modules use reference partition results applied as fixed constraints. The proposed approach reduces placement and routing time for target design. Moreover, identically implemented modules can share reconfiguration data. Under certain restrictions entire partial bitstreams can be relocated to new position by simply modifying Frame Address Register and CRC values.

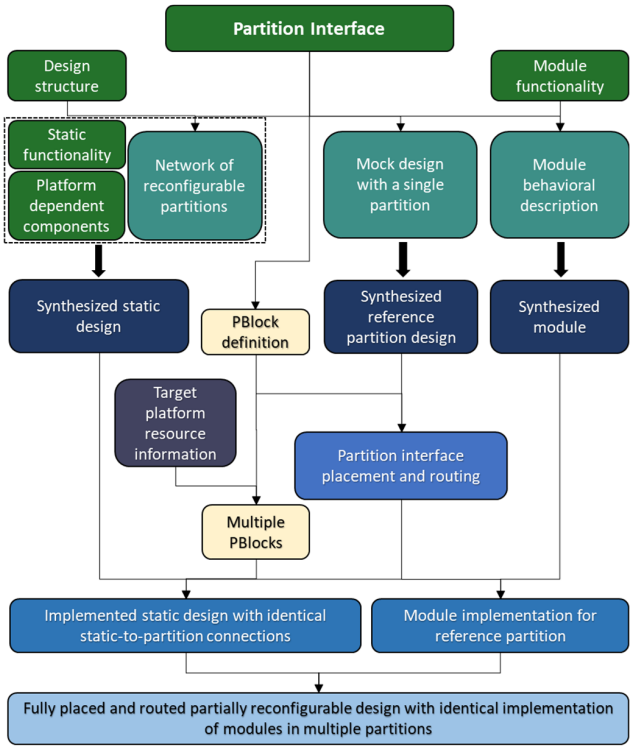


Fig. 1. General concept of the proposed design flow with common reconfigurable module implementations for multiple partitions.

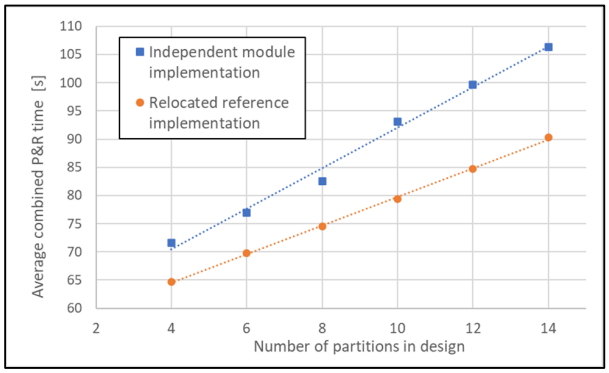


Fig. 2. Placement and routing time for conventional flow using independent module implementation and the proposed method with reference module relocation in design with scalable number of partitions (assigned to identical partition blocks). Average results for a set of reconfigurable modules of different complexity tested designs.

GaN-AlGaN on SiC pHEMT Design for a Digital Radio Frequency Memory

Christina C. Lessi[1], Vasileios T. Vallindras[2], Kleanthis V. Hadjisavva[2], Evangelia A. Karagianni[2], George Deligeorgis[3], Antonios Stavrinidis[3], George Konstantinidis[3], Athanasios D. Panagopoulos[1]
[1]School of Electrical and Computer Engineering, National Technical University of Athens, Greece
[2]Hellenic Naval Academy, Piraeus, Greece
[3]Foundation for Research and Technology Hellas, Creta, Greece
chrislessiee@gmail.com, basil.ballindras@gmail.com, kleanthish@hotmail.com, evka@hna.gr, thpanag@ece.ntua.gr, {deligeo, astav, aek}@physics.uoc.gr

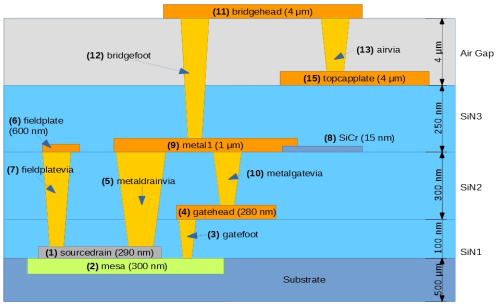
***Abstract*—High-electron-mobility transistor (HEMT) is a type of FET fabricated with a junction between two materials with different band gaps. The most common material that is used in HEMT fabrication is based on the Gallium Arsenide hetero-junction (GaAs-AlGaAs). However, Gallium Nitride (GaN) technology is entering dynamically in the area of transistor fabrication because of the high currents' control by using low voltages. In this paper, a 3D design is presented based on the finger topology. The heterojuction (GaN-AlGaN) creates a piezoelectric polarization and so the two-dimensional electron gas (2DEG), so a full pHEMT model was designed by using Advanced Design System (ADS) software. More specifically, a two-fingers structure is designed in which the two exterior fingers are the source and the one in between is the drain. The transistor size is 160μm length. The small signal model of the designed transistor was created, based on the simulation results. This structure is fabricated and the measured S-parameters are presented.**

***Keywords*—HEMT; GaN technology; AlGaN layer; SiC layer; small-signal model; finger structure**

SUMMARY

Based on the transistor epitaxial structure, a pHEMT transistor was designed in order to operate in 10GHz frequency. It will be designed to be part of the amplifier in a Digital Radio Frequency Memory (DRFM), which is used in Electronic Warfare, operational level.

Focusing on the layers that are used for the transistor design, there is the sourcedrain layer, with 290 nm width, which is used for source and drain design. The gatefoot is actually the transistor gate. The gate width is a critical size since a large width could cause high capacitance, which leads to a slow transistor operation and at the same time a small width could completely destroy the gate performance. For that reason, a gatehead layer is used, which has bigger width size that the gate. Therefore, there is a small width gate and at the same time there is a big width gatehead. The use of the fieldplate is also very important for the GaN HEMT design.

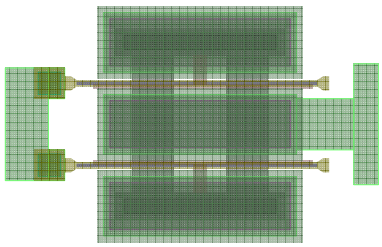


Field plate is a metal surface above gate,which is used to improve transistor's breakdown voltage and current voltage swing. At the same time, it offers additional stability and reliability in HEMT's performance. However, this extra layer creates an unwilling capacity between the source and gate. Therefore, it is important to make a compromise about its size in order to achieve a good transistor performance. Finally, there are other layers, such as the SiN passivation layer, which improves the transistor reliability and power performance. Additionally, a 300nm mesa layer, which is an AlGaN-GaN channel, is the heterostructure that creates the 2DEG.

When the design was completed, by using the simulated S-parameters, equivalent inductances and capacitances Leff and the Ceff respectively were calculated for the small signal model, in between gate, source and drain.

The designed GaN HEMT has been built at the Institute of Technology and Research of Foundation for Research and Technology Hellas (FORTH). Transistor's S-parameters were measured. The calculation of potential instabilities or the maximum gain estimation could be identifying by using the transistor's S-parameters. The Anritsu MS4644B Vector Network Analyzer (VNA) was used for the measurements and the results collection. The input power was 0dBm and the VGS (gate-source voltage) and the VDS (drain-source voltage) that was used to bias the transistor were 2.5Volts and 15Volts respectively, while the drain-source current was 32mA.

This research has been co-financed by the European Regional Development Fund of the European Union and Greek national funds through the Operational Program Competitiveness, Entrepreneurship and Innovation, under the call RESEARCH – CREATE – INNOVATE (project code: T1EDK-00329).



Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Hardware Obfuscation of the 16-bit S-box in the MK-3 Cipher

Jason Blocklove
Department of Computer Engineering
Rochester Institute of Technology
jmb8314@rit.edu

Steve Farris
L3Harris Technologies
Steve.Farris@L3Harris.com

Michael Kurdziel
L3Harris Technologies
Mike.Kurdziel@L3Harris.com

Marcin Łukowiak
Department of Computer Engineering
Rochester Institute of Technology
mxleec@rit.edu

Stanisław Radziszowski
Department of Computer Science
Rochester Institute of Technology
spr@cs.rit.edu

I. Summary

With the continuous growth of cyberinfrastructure in modern society, secure computing, storage, and communication require that the underlying framework utilizes both software and dedicated hardware components. These hardware components have traditionally been used to enhance overall systems' performance, cost, and energy efficiency. Unfortunately, adding specialized hardware into different points of the state-of-the-art cyberinfrastructure can create new security threats that did not exist in the past. These threats necessitate development of new methodologies and approaches for secure hardware design and manufacturing. The objective is to prevent malicious behavior such as insertion of hardware Trojans, overproduction, manufacturing of counterfeit devices, reverse engineering, or side-channel analysis.

One common technique used to protect hardware circuits against these threats is to obfuscate the implementation itself, such that necessary design analysis becomes too expensive, in either time or resources, for an adversary to realistically accomplish. These methods utilize additional logic gates added to a circuit such that a secret key is required for unlocking circuit's proper functionality. This can be e.g. done using Key Programmable Gates (KPGs), which are gates that use one input as a key bit in order for the circuit to act as expected.

In this paper we are using a SIMON block cipher as a One-way Random Function (ORF) for a logic locking method on a substitution box (S-box) from a customizable, authenticated encryption (AE) cipher MK-3. We utilized satisfiability (SAT) attacks as a method of attacking hardware obfuscation. A high-level diagram of the obfuscation approach is shown in Figure 1. Several configurations were tested with varying numbers of SIMON rounds and with fixed plaintext or fixed ciphertext inputs. The S-box obfuscated using this 32-bit key and a round-reduced implementation of the SIMON cipher is shown to be secure against a SAT attack within 5 days limit time.

We are convinced that using an ORF to transform key bits before another locking mechanism is the right approach. With a sufficient number of key bits we can expect any SAT attack to fail, if the ORF being used has proper cryptographic strength.The 32 bits used in our experiments, however, may not be enough for high security requirements

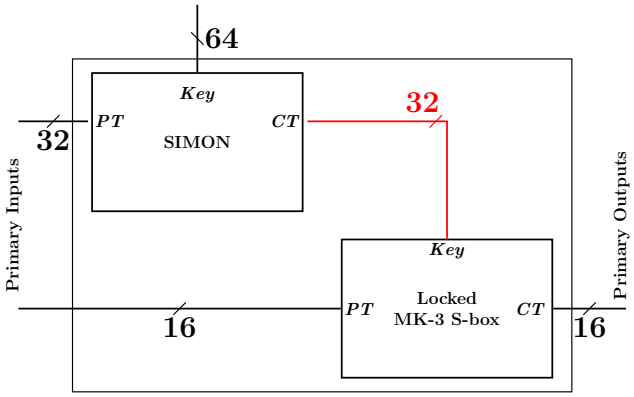


Fig. 1. SIMON as an ORF for Obfuscation

Implementation of a Modified High-Voltage Unity-Gain Buffer

Mariusz Jankowski
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
Mariusz.Jankowski@p.lodz.pl

EXTENDED ABSTRACT

This paper presents necessary modifications of a specialized high-voltage unity-gain buffer related to its physical implementation in a selected high-voltage SOI process. Several additional safety devices are required for non-destructive power-up, normal operation and power-down phases of this buffer function cycle. The modifications are largely related to intricacies of the buffer topology, as low- and high-voltage MOS devices are used there in close cooperation. Impact of the implementation-related changes on the buffer operation capabilities is presented and discussed.

High-voltage buffer discussed in the paper is introduced in [1]. This buffer offers very high input impedance and low output impedance. This structure offers unity-gain and can be considered as a voltage follower [1, 4]. The buffer is designed to operate with supply voltages over 5 V. Thus, it can be considered as a mid-voltage or high-voltage circuit. Depending on CMOS or SOI process capabilities, its maximum supply and input voltage amplitudes can reach up to tens of volts.

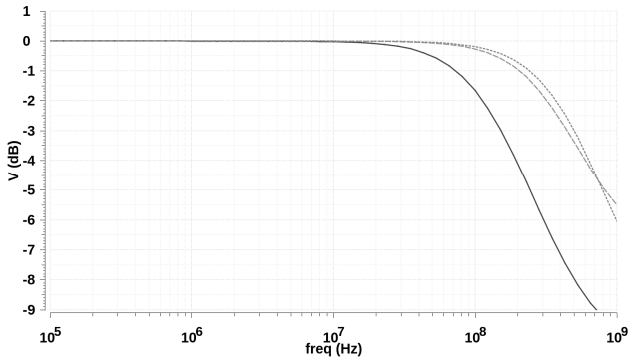


Fig. 1. AC-domain comparison of the buffer implementation stages: the original buffer – dotted line, the SOAC buffer – dashed line, the laid out buffer –solid line

The presented buffer is a part of a high-voltage integrated circuit designed in X-FAB XDM10 SOI process. All presented simulation results were obtained with application of Cadence Virtuoso software coupled with Spectre simulator and proper design-kit provided by the X-FAB company.

Simulations of all the buffer variants were conducted for 18 V high-voltage supply and 5 V low-voltage supply. Input signals are always added to 9 V offset voltage and then provided to the buffers inputs.

TABLE I.
COMPARISON OF THE BUFFER IMPLEMNENTATION STAGES

Comparison of the buffer implementation stages			
Buffer implemen-tation stage	***Small-signal cut-off frequency [MHz]***	***Output to input difference [mV]***	***Voltage gain for 11 V, 21 MHz sin. [dB]***
The riginal schematic	502.0	46,43	-3.10
The SOAC schematic	448.8	46,43	-3.49
The layout	152,9	60,90	-17.74

The performed comparison shows that influence of about 30 safety devices in form of diodes, Zener diodes, and stacks of diode-connected high-voltage transistors is very limited. This is a very valuable conclusion, as all these devices are needed for safe operation of the physically implemented buffer. The influence of the safely devices is limited owing to fact, that most of these devices are placed outside the buffer signal path.

The process of laying out the circuit causes much more pronounced deterioration of the buffer speed parameters, which is a typical outcome of physical implementation process and can be coped with during earlier stages of circuit design by means of preparing designs with parameter margins expendable during laying out process. Fig. 4 and Table 1 more insight into deterioration of the buffer parameters of the buffer.

ACKNOWLEDGMENT

This research is funded by Department of Microelectronics and Computer Science of Lodz University of Technology.

REFERENCES

[1] M. Jankowski, A. Napieralski, "High-Voltage high input impedance unity-gain voltage buffer," Microelectronics Journal, 2013, vol. 44, no. 7, pp. 576-585.

[2] A. Napieralski, et al., "Recent Research in VLSI, MEMS and Power Devices with Practical Application to the ITER and DREAM Projects," Facta Universitatis Series: Electronics and Energetics, Vol 27, No 4 (2014), December 2014, pp. 561—588.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Investigation of Inductor-based Fully On-chip Boost Converter

Róbert Ondica, Daniel Arbet, Martin Kováč, Viera Stopjaková
Institute of Electronics and Photonics, Faculty of Electrical Engineering and Information Technology
Slovak University of Technology in Bratislava
Email: robert.ondica@stuba.sk

Extended Abstract

This paper presents the efficiency investigation of a fully on-chip DC-DC step-up voltage converter. Research is mainly focused on finding the optimum operation point of power conversion to provide the high output power and conversion efficiency of the on-chip converter solution. Topology of voltage converter is based on high frequency switching of fully integrated inductor. The study also analyses the impact of inductor properties on circuit operation and on output power and conversion efficiency. For better evaluation of impact of inductor properties and for elimination of power losses in circuit design, the most simple circuit topology of step-up DC-DC power converter $-$ $boost\ converter$ [1] $-$ was chosen. Also, for further elimination of power dissipation, all components was considered ideal, except inductor itself.

Fully integrated symmetrical multilayer stacked inductor was proposed in previous work [2] and designed for low frequency inductive near-field electromagnetic energy transfer in conjunction with active implantable medical devices. Presented topology is symmetrical 5-turn square coil implemented in 5 metal layers. Outer diameter of inductor is $1.16\ mm$ and covers area of $1.346\ mm^2$. Inductor properties were measured and introduced in [3]. Alternative schematic was then derived from measurement results and used in simulated voltage converters. Best achieved results of integrated inductor properties were quality factor Q=3.03, inductance L=66.08 nH and series resistance Rs=7.63 Ω. For better understanding of significance of individual inductor parameters, another model of ideal integrated inductor with variable series resistance and quality factor was used in boost converters. Values of series resistance of ideal inductor was chosen in range from Rs_{min}=1 Ω to Rs_{max}=10 Ω resulting in quality factor of inductor up to Q_{max}=15. Chosen values respects theoretical technological possibilites and other works. Results of simulations of power converters with alternative schematic of real measured inductor was then comapred to converter circuits implementing ideal inductor with series resistance.

Core part of study consists of finding the optimum operation point of power conversion of voltage converter driven by different control circuits. In this case, we propose ideal pulse frequency modulation (PFM) circuit to control the level of output voltage. PFM control circuit holds output voltage at V_{out}=1.2 V. Boost converter operates with input voltage V_{in}=0.6 V, conversion ratio is therefore 2. Values of load resistor were chosen in broader range to find point of maximum output power. Boost voltage converter controlled by PFM control circuit with alternative schematic of measured inductor achieved top power conversion efficiency of 62.96 % at ouput power of 3.6 mW at rather high switching frequency Fsw=247.7 MHz. Maximum output power of 6 mW was achieved with corresponding power conversion efficiency 50.56 % at switching frequency Fsw=118.1 MHz. Best results of power conversion efficiency of voltage converter reached value of 98.6 % at low output power of 0.6 mW and switching frequency Fsw=7.57 MHz and the maximum output power of 6 mW with efficiency 84.81 % was achieved at Fsw=233.31 MHz. These results were achieved by voltage converter with ideal inductor with low series seristance of Rs=1 Ω and Rs=5 Ω, respectively. In all simulations, the converter operated in DCM. Conduction mode of inductor was not further investigated and has only information value.

Last part of this study compares achieved results to other work, especially the same design of voltage converter driven by pulse width modulation (PWM) control circuit with alternative schematic of the same integrated inductor proposed in [3]. Study also shows impact of main properties of integrated inductor on monolithical boost voltage converter and propose importance of individual parameters. We emphasize the importance of enhancing the quality factor of inductor and decreasing its series resistance for obtaining the best results. Inductance of inductor is then of lower importance, hovewer, it should be kept at reasonable values.

This feasibility study investigated the possibility of fully on-chip implementation of whole voltage converter circuit with suitable power conversion efficiency and output power. Proposed circuit should be able to compete with other step-up voltage converter circuits that uses external switched inductors (or capacitors) while offering higher power density and considerable space savings.

All voltage converter circuits were simulated for implementation into a standard UMC 130 nm CMOS technology and Cadence design environment was used for all simulations. Results obtained by simulations of voltage converters was only theoretical and should be investigated further.

Acknowledgement

This work was supported in part by the Slovak Research and Development Agency under grant APVV 19-0392, the Ministry of Education, Science, Research and Sport of the Slovak Republic under grants VEGA 1/0731/20 and VEGA 1/0760/21, and ECSEL JU under project PROGRESSUS (Agr. No. 876868).

References

[1] A. Shaltout, M. Lipski, and S. Gregori, "Analysis of boost dc-dc converters with integrated coupled inductors," in *2016 28th International Conference on Microelectronics (ICM)*, 2016, pp. 129–132.

[2] M. Kováč, V. Stopjaková, D. Arbet, L. Nagy, and J. Brenkuš, "Investigation of on-chip coil in 130 nm standard cmos for wpt and bio-applications," in *2016 International Conference on Emerging eLearning Technologies and Applications (ICETA)*, 2016, pp. 177–182.

[3] R. Ondica, D. Arbet, M. Kováč, and V. Stopjaková, "Feasibility study towards increasing efficiency of fully on-chip dc-dc boost converter," in *2020 International Conference on Applied Electronics (AE)*, 2020, pp. 1–4.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Modelling of First- and Second-order Chemical Reactions on ARUZ – Massively-parallel FPGA-based Machine

Piotr Amrozik
Department of Microelectronics and Computer Science
Lodz Univ. of Technology, Poland
Email: piotr.amrozik@p.lodz.pl

Krzysztof Hałagan
Department of Molecular Physics
Lodz Univ. of Technology, Poland
Email: krzysztof.halagan@p.lodz.pl

Kamil Rudnicki
Brightelligence Sp. z o.o., Poland
Email: publications@brightelligence.com

EXTENDED ABSTRACT

The ARUZ, built using the TAUR technology in Bio-NanoPark Lodz, is a massively-parallel FPGA-based HPC machine. It implements the Dynamic Lattice Liquid (DLL) model. The basic version of DLL algorithm models Brownian diffusion in a long time limit for simple liquids. In this paper, DLL extension, allowing the introduction of simple chemical reactions in simulations executed on ARUZ, is presented along with its implementation using FPGA technology. This extension is called the REACTION mechanism and can be used for modeling of first- (R1), second- order (R2) reactions, and their combination (R12).

In all three cases, the reaction depends on the fulfillment of the probability condition. In the case of simple R1 reactions, an element may spontaneously change its type regardless of its neighborhood (but may depend on its spatial position in the simulation box), e.g. $D1 \rightarrow D2$. The type change takes place when the probability: $p_1 = p_1(X) + p_1^e(X)$ of the reaction for the considered element is greater than the generated pseudorandom number in the range [0,1]. In the case of R2 reactions, the change of the element type occurs in interaction with its nearest environment, e.g. $A + B \rightarrow C + C$. First, one of the nearest neighbours is selected at random, if the reaction is possible, it is tested for the success of the reaction according to the specified probability: $p_2 = p_2(XY) + p_2^e(XY)$. Probability p_2 is defined for pairs of elements X and Y, and can also be dependent on spatial position ($p_2^e(XY)$).

One of the more interesting examples is presented in Figure 1 as the example of $A + B \rightarrow C + C$ reaction. In the first step, the E_{UT} selects a potential reaction partner on direction $d0$. At the same 3 neighboring (E_{d1}, E_{d3}, E_{d5}) elements indicated the E_{UT} as the reaction partner. The selections are communicated amongst each other. In the second step, the E_{UT} knows that element E_{d0} does not join the reaction with the E_{UT}. Since the element E_{d3} continues pointing at the E_{UT}, in step 3, the R2 reaction process occurs and consequently the E_{UT} changes type from $B \rightarrow C$ and $A \rightarrow C$.

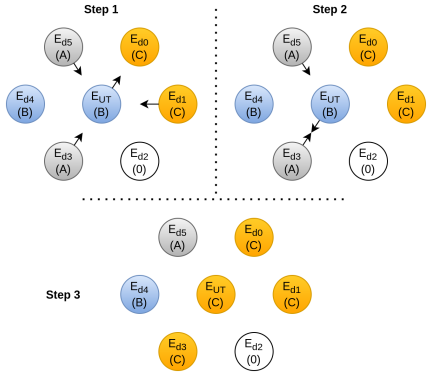


Fig. 1. 2-dimensional R2 reaction example - $A + B \rightarrow C + C$.

For each simulation variant, a separate bitstream file is generated. Consequently, if no reaction mechanism is needed in a simulation variant, it is excluded and effectively releases the FPGA resources. Mechanisms for R1 and R2 reactions can be included independently. Inclusion of both in the bitstream file means both reaction types are analysed. In such a case, by using appropriate probability factors, R1 or R2 can be softly eliminated from the simulation (for all / some / none of the elements), however, the resources are still in use.

The maximum number of simulation nodes in DSlave is most often limited by CLB (Configuration Logic Block), specifically LUT (Look-Up Table), resources. Consequently, the need to optimize the use of it becomes the highest priority when adding new features to ARUZ.

The proposed algorithm realizing the reaction model requires mostly the resource of BRAM (Block Random Access Memory), Flip-Flops and the resource of highest utilisation in the machine – LUTs. To save LUT resources, the BRAM is addressed by the registers already present in the analysis – the types of reacting elements and the reaction type. Thanks to the concatenation of such registers, a direct address is generated and no extra LUTs are used.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Molecular Diffusion Simulation on ARUZ – Massively-parallel FPGA-based Machine

Rafał Kiełbik[1], Krzysztof Hałagan[2], Kamil Rudnicki[3], Piotr Polanowski[2], Grzegorz Jabłoński[1], Jarosław Jung[2]
[1] Department of Microelectronics and Computer Science, Lodz University of Technology, Poland
[2] Department of Molecular Physics, Lodz University of Technology, Poland
[3] Brightelligence Sp. z o.o., Poland
Email: rkielbik@dmcs.p.lodz.pl, krzysztof.halagan@p.lodz.pl, publications@brightelligence.com,
piotr.polanowski@p.lodz.pl, gwj@dmcs.p.lodz.pl, jaroslaw.jung@p.lodz.pl

Extended Abstract

Simulations based on DLL (Dynamic Lattice Liquid) model are devoted and widely used to analyse phenomena in molecular environments. DLL quite precisely predicts the results of the investigated phenomena, but also properly models the dynamics of simulated processes by accurately imitating the behaviour of the analysed matter. The simulated physical substance (e.g.: a polymer immersed in a solvent) is modeled by a set of nodes representing elements of this substance (e.g.: atoms, particles, monomers) or empty regions, where such elements can enter during simulation. The nodes are logically positioned in the sites of face-centered cubic (FCC) lattice, chosen due to the highest packing factor among regular lattices. The FCC lattice has a coordination number $Z = 12$, which means that each node is connected to 12 neighboring nodes. As a consequence, in DLL simulations, each node directly interacts with the 12 nearest nodes. Clearly, long-distance interactions could be obtained by means of forwarding interactions through the nodes, but DLL does not involve such long-distance interconnections. This apparent limitation is actually the source of DLL efficiency, giving – for a wide range of applications – a satisfactory modelling precision.

DLL is a kind of Monte Carlo method used to obtain the statistical properties of simulated processes. Therefore, to achieve reasonable accuracy, DLL requires a substantial number of nodes used in simulation. It is commonly assumed that for the appropriate modelling accuracy, the number of nodes in the lattice should be of the order of 10^6. In DLL simulations, the set of nodes is treated as a cellular automaton. All nodes update their state using the same rules. Since the nodes model the elements of a simulated physical substance (e.g.: fluid, polymer, etc.), these rules correspond to the behavior of particles (or atoms, monomers, etc.) in such substance. Each node performs the computations responsible for modeling such physico-chemical mechanisms as: creating and breaking bonds, reacting, interfering with external fields, etc. DLL can model the movement of elements in dense environments, as it takes into account a so-called "cooperative movement". There are two possible cooperative movement scenarios considered (Figure 1): loops and ways.

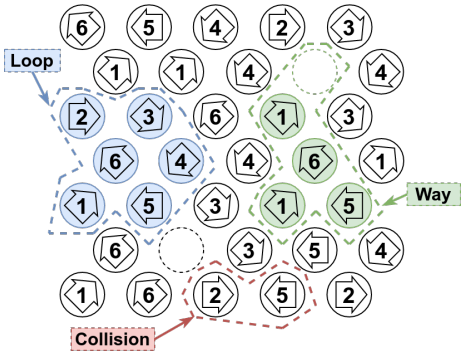


Fig. 1. Loop, way and collision in simplified (2D) lattice (coordination number $Z = 6$).

In case of the cooperative way a vacancy is required. The modeled element next to the vacancy can occupy it, making the vacancy for another element. In case of the cooperative loop, no vacancies are needed. Several modeled elements can switch their places at the same time. In DLL such a switching is allowed only for more than two elements. An attempt by two elements to exchange their positions is treated as a collision and is prohibited.

The paper presents two algorithms, sequential and parallel, implementing the DLL model for the analysis of molecular diffusion. The time required for each step in a sequential algorithm grows linearly with the number of nodes. For multi-core architectures, this algorithm can be partially parallelized. Unfortunately, synchronization of threads is required, what significantly reduces the efficiency of multi-threaded implementation of the sequential approach to DLL and as a consequence it limits its applicability. The bottlenecks of the sequential algorithm are solved by the parallel one, which uses a different principle, but requires a dedicated FPGA-based simulation hardware with very low interconnection latency. The speed of simulation performed using this hardware is 2 orders of magnitude higher when compared to the best known multi-threaded sequential solution.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Molecular Simulations Using Boltzmann's Thermally Activated Diffusion - Implementation on ARUZ – Massively-parallel FPGA-based Machine

Grzegorz Jabłoński, Piotr Amrozik
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
Email: gwj@dmcs.p.lodz.pl, piotr.amrozik@p.lodz.pl

Krzysztof Hałagan
Department of Molecular Physics
Lodz University of Technology
Lodz, Poland
Email: krzysztof.halagan@p.lodz.pl

EXTENDED ABSTRACT

ARUZ (Analizator Rzeczywistych Układów Złożonych, Analyser of Real Complex Systems) is a massively parallel FPGA-based simulator located at BioNanoPark Lodz. This machine has been designed to reflect the Dynamic Lattice Liquid (DLL) algorithm in hardware. https://www.overleaf.com/project/604f63a57f49625a17de87e0

The DLL model is based on the concept of cooperative motion of objects (elements). The algorithm works on a completely occupied lattice, where the elements cannot easily move over a long distance, due to the occupation of all neighboring lattice sites. In this case, the only way to move the elements with excluded volume preserved is cooperative motion. In DLL, cooperative rearrangements have a form of closed loops of displacements involving at least three elements. Loops are formed spontaneously in a random way.

To model more complex phenomena, DLL implemented on ARUZ was enriched with additional functionalities, the so-called "mechanisms". One of them is the ENERGY mechanism that allows reducing the thermal noise in simulations by lowering the temperature. This mechanism is useful in simulations of, e.g., phase separation processes where intermolecular interactions have to be varied. The system Hamiltonian for i-th lattice site populated by X-type element is defined as:

$$\frac{E_i}{k_BT} = \frac{1}{k_BT}(\frac{1}{2}\sum_j \varepsilon_{XY_j} + H_{X_i}) \tag{1}$$

where the sum extends over all nearest neighbors and j can take any type Y. T is the absolute temperature and k_B the Boltzmann constant. H_X/k_BT is the interaction energy of X type with the external field and can depend on the spatial position to model e.g. temperature gradient. ε_{XY}/k_BT is the interaction energy of the i,j pair and is position-independent. In presented model, ε_{XY} always equals ε_{YX}. Both, ε_{XY}/k_BT and H_X/k_BT, are input data. A kinetic Monte Carlo test, representing Boltzmann statistics, is applied, i.e., an effective attempt of motion is performed with probability proportional to the energy of the actual local state:

$$P_i = e^{-\frac{E_i}{k_BT}} \tag{2}$$

The test is executed for all elements in a given loop of possible cooperative movement - all elements must pass it, otherwise the whole loop is immobilized (when $exp(-E_i/k_BT) < random[0,1)$).

As a result, if $\varepsilon_{XY} > 0$ then attractive interaction is present for i,j pair. The interactions become effective at a finite temperature by reduction of the probability of motion. ε_{XY} describes the barrier which has to be overcome in order to release contact between X and Y during the thermally-activated diffusion process.

If we define $\varepsilon_w(X,Y) = e^{(-\frac{1}{2}\frac{\varepsilon_{XY}}{k_BT})}$ and $\varepsilon_e(X) = e^{(-H_X(x,y,z))}$, we obtain $P_i = \prod_{k=1}^{Z} \varepsilon_w(X,Y_k) \cdot \varepsilon_e(X)$

As $\varepsilon_w(X,Y_k)$ and $\varepsilon_e(X)$ are constant, no exponentiation operation is needed in FPGA fabric, as they can be precomputed in software and stored in BRAM. To store ε_w and ε_e and perform operations on them, we need to apply a floating-point format, as it ensures a constant relative precision for the full range of stored values.

To store ε_w and ε_e we need a 17-bit mantissa and a 9 bit exponent to encompass the entire assumed range. A special way of BRAM addressing was used, eliminating complicated calculations thanks to address vector concatenation. Artix XC7A200T has 740 DSP slices, each containing a 25 x 18 multiplier. To implement multiplication to calculate P_i, a single Xilinx Floating-Point Operator IP core was used. This multiplier needs two DSP slices, limiting the number of nodes that can be implemented in one DSlave to 370.

The performed simulations confirmed that the implementation gives exact results compared to theoretically calculated values.

The presented implementation is applicable to other lattice algorithms where Boltzmann weights need to be used.

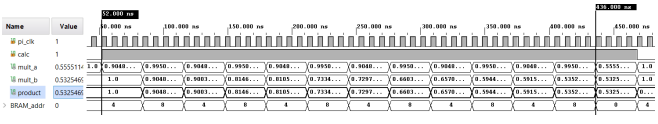


Fig. 1. Result of simulation.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Queuing Parallel Computing CAD Tasks in the Design and Optimization of IC Topography

Adam Wojtasik
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology, Warsaw, Poland
adam.wojtasik@pw.edu.pl

Extended Abstract

Designing the complex topography of integrated circuits and the development of new manufacturing technologies require the use of numerous and extensive computer aid systems. Various professional, commercial or academic educational software packages are used for such purposes. In the process of designing the topography of an integrated circuit, a specific sequence of these tasks must be solved iteratively. This will result in a rapid increase in computing time – it can be days or even weeks. So, it is clear that the most important issue here is the computing power of the computers used to carry out these experiments. At present, a significant increase in the computing power of computers is achieved practically only by introducing multi-core processors and multi-processor systems in the design of these computers. This qualitative change marked a new direction in the development of the software included in the design system – increasing the efficiency and computational capabilities of modeling by applying parallel processing. Therefore, there is a need to organize computational experiment in such a way that the best use is made of the existence of multiple cores and processors in a computer or entire computers organized in clusters. The designer should understand the dependencies occurring in parallel processing and should be able to analyze the experiment in terms of such processing. This will make it possible to design appropriate scenario of computational experiment and create optimal execution scripts allowing for a significant reduction of the time needed to perform this experiment. We present here two examples of such analyses.

A. Modeling of parametric yield

The parametric yield modeling scenario belongs to the type of experiment most often used among the verification and optimization procedures of an integrated circuit topography design – the Monte Carlo method. The goal here is to determine the statistical properties of the functional parameters of the topography implemented in a given technology, taking into account the production. This allows for the prediction of parametric yield. From the point of view of parallel processing, the subsequent runs of the main Monte Carlo loop are independent tasks. The only requirement for synchronization within these tasks is internal synchronization of the individual internal stages of the calculations to ensure that these stages are executed sequentially after the previous step is fully completed. Supervision and synchronization of the entire process can be performed here in two ways: 1) arranging a loop on each core with the number of passes equal to the sample size divided by the number of cores; 2) running subsequent tasks waiting in the queue on the cores that have already completed the previous execution. The first approach is simple but it is only suitable for tasks whose execution time is more or less the same and/or predictable. It means that all processors will the same time to complete the job. Unfortunately, the run times of most applications used in parametric yield modeling are unpredictable and may have very different execution time (heuristic algorithms and iterative numerical methods). The time needed to perform a step in one loop may differ even dozen times from the time necessary to perform the same step in another loop. In this situation, the scenario in which one large loop is divided into several smaller local loops seems to be more favorable. In yield modeling case, the computation can be divided into three stages organized as three local loops: extraction, modeling, simulation. This results in smaller tasks that may facilitate optimization of task synchronization and more efficient use of the cores – but controlling the entire computation stages is important. Therefore, a complex supervisory system should be used, which will optimize the occupancy of the cores.

B. Optimization of test vectors

Let us consider a scenario that allows finding the order of test vectors that will accelerate the detection of a possible failure of a given system. The idea behind the procedure is based on the fact that not all such failures are equally probable. There two main loops in these scenario (identification of unwanted wiring changes caused by possible defects; electrical and logical simulation of damaged circuits). The successive runs of the second loop are independent tasks (they relate to various electrical schemes). The first loop runs are not independent – they are based on the results obtained in the previous runs. Therefore, they must be executed sequentially on one core. The remaining cores do not work during these calculations. As a result, the test vector optimization scenario requires much more modification than just splitting the loops into smaller ones. There is a need to reorganize the entire procedure flow chart.

Conclussions

The time needed to perform a time-consuming computational experiment, assuming the use of parallel processing, is determined by hardware conditions. The important factor here is the number of processors or the number of cores available in computers, or the size and configuration of the computing cluster. However, it is equally important to correctly configure the computational experiment, i.e. to define such a calculation scenario and such construction of the execution scripts that the hardware capabilities are used in an optimal way.

Rail to Rail Comparator for SAR ADC in Biomedical Applications

Nawaf ALjehani[1], Mohamed Abbas[1,2]
(1) Electrical Engineering Department, College of Engineering, King Saud University, Kingdom of Saudi Arabia.
(2) Electrical Engineering Department, Faculty of Engineering, Assiut University, Egypt
437105870@student.ksu.edu.sa, mohabbas@ksu.edu.sa

SUMMARY

This paper presents low voltage low power a rail to rail common mode range clocked comparator. The target application of the proposed circuit is analog to digital converter for biomedical applications. The proposed comparator is composed of two stages which are pre-amplifiers and modified strong-Arm latch as shown in figure 1. The outputs of NMOS-input and PMOS-input pre-amplifiers are combined by the modified Strong-Arm latch producing rail to rail common mode range clocked comparator. Adopting TSMC 0.18µm technology, the preamplifier stages were designed to work in weak inversion using g_m/I_D design methodology. The simulation results show that the preamplifier stage consumes less than 0.275µW using power supply of 0.75V. The pre-amplifier DC gain of 43.15dB and unity gain frequency of 300 kHz. Figure 2 shows a sample output of the comparator as the input common mode is fixed.

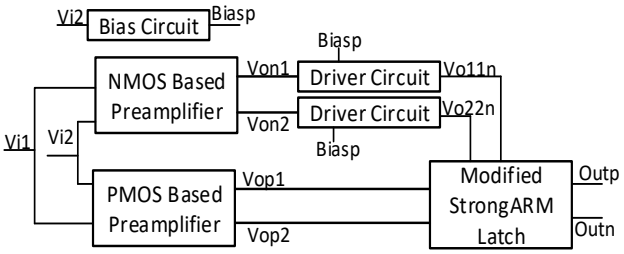


Figure 1. Complete comparator circuit block diagram

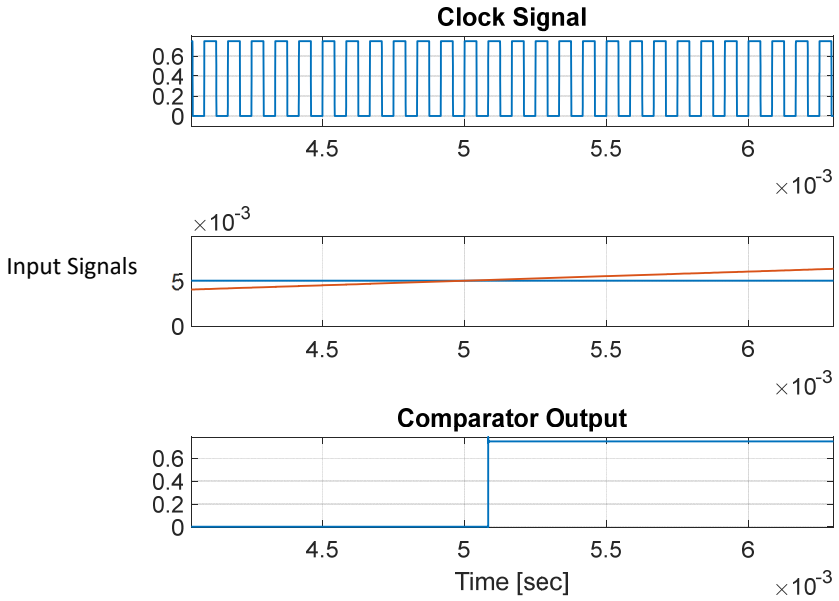


Figure 2. Rail to Rail comparator transient simulation with common mode voltage of 5mV zoomed view

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Software Tool Aiding Analysis and Design of Low-Power Parallel Prefix Adders

Ireneusz Brzozowski
AGH University of Science and Technology
Institute of Electronics
Krakow, Poland
ireneusz.brzozowski@agh.edu.pl

Extended Abstract

Adders are one of the basic and essential arithmetic circuits. Their design is still important, especially in the aspect of power consumption and speed. To achieve satisfactory results, a designer has to make more effort. He needs to do a thorough analysis. It is not enough to consider only general conditions of a circuit work only, but the designer must take an individual approach to the circuit. For an efficient and time-satisfying design, he needs specialist tools to do such task.

In this paper, a software tool aiding a design of Parallel Prefix Adders is presented. PPAs are seen as some of the fastest because of the way of carry signals generation. And a circuit responsible for these signals can be designed in many ways. In the literature, we can find many papers describing regular structures of PPA, but irregulars are also interesting and can yield a profit in design. The proposed software supports design of carry generation-propagation block by calculating a circuit activity and equivalent capacitance for the requested input activity behavior. Thanks to a graphical interface, a user can test many possibilities in an easy way by drawing a graph of propagation-generation block. Parameters are calculated and shown on the graph for all nodes. Finally, after checking of the graph completeness, the netlist of the adder is generated. The tool is useful when the designer, looking for the best solution, wants to analyze many adders' structures for given input activity scenarios.

The program consists of two main parts, graphical and computational. The first one is used to draw the PG graph and to invoke calculations of switching activity and equivalent capacitance for just drawn graph. The second part is responsible for the calculations. The program is created using Matlab environment. The main window of the program, with exemplary design, is shown in Fig. 1. It consists of a field with a mesh for drawing the PG graph, described by inputs and levels. At the bottom, there are a few push buttons and message fields. Drawing of the PG graph is very easy by mouse. After drawing a graph, the user can check the activity of the circuit by clicking the button "Check Activity". Appropriate functions are started and results are shown in the graph (Fig. 2). There are switching activity and equivalent capacitance for each node in the PG circuit. Finally, a netlist of the circuit is generated.

This work has been supported by AGH University of Science and Technology under subvention funds (no. 16.16.230.434).

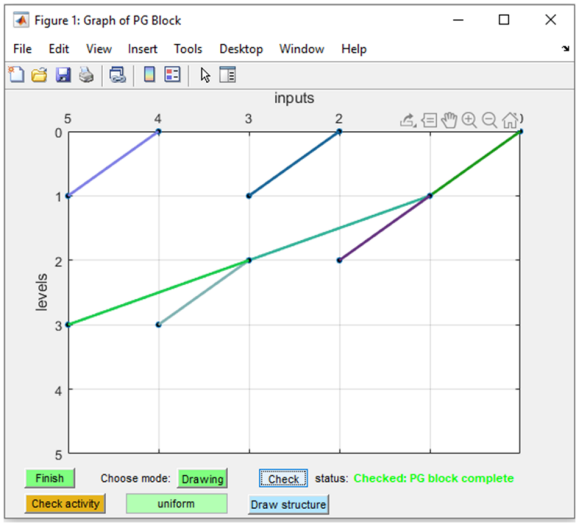


Fig. 1. The main window of the program with example adder.

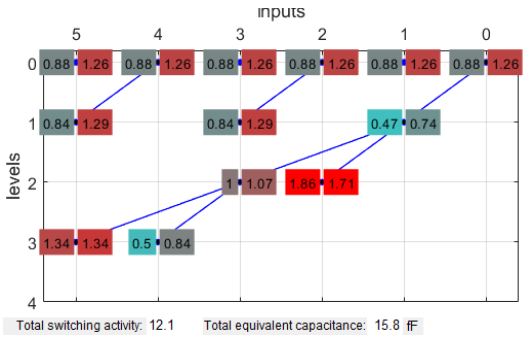


Fig. 2. Switching activity and equiv. cap. of the example 6-bit adder.

The paper shows a useful software tool which can be usable during the design of PG tree of PPA. The program allows a user to interactively design the circuit and analysis of its energy parameters (activity and equivalent capacitance). The designer can change structure of the graph in an easy way and check the properties of a new concept. The author uses the program in his research and on the other hand, he wanted to show the idea of such an interactive design focused on low-power.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Tree-Based Hardware Recursion for Divide-and-Conquer Algorithms

Braeden Morrison, Marcin Lukowiak
Rochester Institute of Technology, Rochester, NY USA
{bjm4184, mxleec}@rit.edu

EXTENDED ABSTRACT

It is well-known that custom hardware accelerators implemented as application specific integrated circuits (ASICs) or on field-programmable gate arrays (FPGAs) can solve many problems much faster than software running on a central processing unit (CPU). This is because FPGAs and ASICs can have handcrafted data and control paths which exploit parallelism in ways that CPUs cannot. However, designing custom hardware is complicated and implementing algorithms in a way that takes advantage of the desired parallelism can be difficult. Specialized Hardware Description Languages (HDLs) are used in the design process and hardware models must be tested via complex simulations, which are slow and difficult to debug. The benefit is that hardware implementations of algorithms can often process data orders of magnitude faster than their software equivalents and with lower energy expenditure. More recently, there have been efforts to make the hardware design process more similar to software development with the design methodology called High-Level Synthesis (HLS). HLS tools work by generating hardware designs from algorithms written in software programming languages, like C/C++. This allows for hardware design to use the more flexible software programming languages and can simplify the verification process. HLS is becoming an increasingly popular design methodology and has a lot of support from Electronic Design Automation (EDA) tool manufactures. For example, Intel and Xilinx have their own HLS tools that work with their respective FPGAs. Additionally, both companies have recently announced new high-level development platforms targeting heterogeneous systems indicating their continued investment in HLS technology. However, despite the popularity of HLS, there are some features of software programming languages that most HLS tools don't support, such as recursive functions and dynamic memory allocation. Given the popularity of HLS and the increasing prevalence of high-level abstractions in hardware design, the goal of this work was to examine the abstraction of recursion in detail and propose a new hardware implementation framework for it. In this paper we introduce a new framework for implementing recursive functions in hardware, which we call TreeRecur. TreeRecur uses trees to represent the branching recursive function calls of divide-and-conquer algorithms, which makes it possible to take advantage of their procedure-level parallelism. To allow for design flexibility, TreeRecur executes algorithms using a configurable number of independent function processors. These processors are generated using HLS design flow, making it easy to implement a variety of different algorithms. The TreeRecur system is comprised of three primary components: the HLS front-end, the tree back-end, and communication channels connecting them together as shown in Figures 1 and 2. The front-end is the user-facing part of the system. It contains the independent function processors that are used to execute the desired algorithms and when users want to implement a new algorithm, they simply change the processors running in the front-end. The back-end manages all of the aspects of the tree memory management. This is the same for all algorithms and doesn't need to be modified by the user. Finally, the communication system contains the First-In First-Out (FIFO) queues that the front-end and back-end use to communicate with each other. Functionality of our framework was tested using two simple algorithms and compared against software implementations of the same algorithms. Performance results were collected in terms of execution speed and energy consumption.

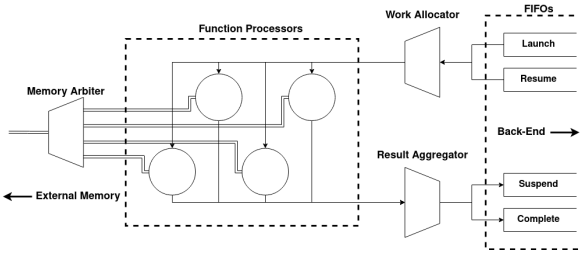


Fig. 1. System Front-End

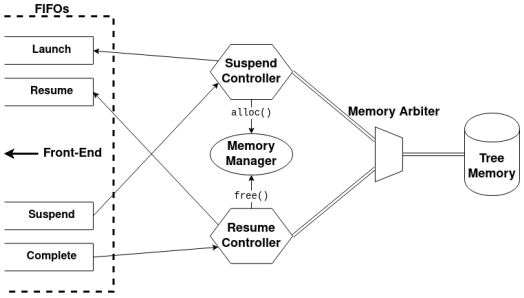


Fig. 2. System Back-End

Thermal Issues in Microelectronics

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Analysis of Heat Transfer Processes in Electronic Nanostructures Using the Dual-Phase-Lag Model

Marcin Janicki, Artur Sobczak, Grzegorz Jabłoński
Department of Microelectronics and Computer Science
Lodz University of Technology
Wólczańska 221, 93-005 Łódź, Poland
janicki@dmcs.p.lodz.pl

EXTENDED ABSTRACT

Temperature is an important factor affecting the operation of electronic devices. For two centuries thermal processes were modeled applying the classic Fourier heat transfer theory, but due to the miniaturization of electronic devices it has become necessary to consider various phenomena related to the phonon scattering at semiconductor boundaries or the ballistic effects. Consequently, alternative approaches taking into account the consideration of microscale effects in macroscale heat transfer models were developed.

This paper employs for thermal simulations of a nanosize structure the Dual-Phase-Lag (DPL) equation, presented in (1), which renders possible taking into account the mutual delays between changes of heat flux q and temperature T owing to the introduction into the Fourier law of heat conduction of two additional terms. They depend on the relaxation time constants τ_q and τ_T, which are the respective heat flux and temperature time lags, hence the name of the model. The parameter α in the equation is the thermal diffusivity and t denotes time.

Compared to the classic Fourier-Kirchhoff heat equation, there are two additional terms containing the second-order time derivative of temperature and the third-order mixed time and space derivative of temperature. The analyses carried out here are aimed at the determination of the influence of these new values on the heat diffusion speed. This is done by varying the value of the commonly encountered in literature dimensionless parameter B, which is equal to $\tau_T/(2\tau_q)$.

$$\alpha \tau_T \frac{\partial}{\partial t}\left(\nabla^2 T\right) + \alpha \nabla^2 T = \frac{\partial T}{\partial t} + \tau_q \frac{\partial^2 T}{\partial t^2} \qquad (1)$$

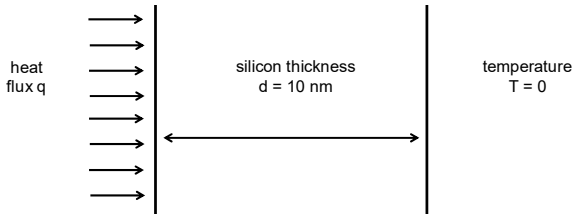


Fig. 1. One-dimensional benchmark structure.

The one-dimensional benchmark structure, shown in Fig. 1, is made of silicon and it has the thickness d of 10 nm. This structure is heated from the left side by the heat flux q and ideally cooled at the right one, where the isothermal boundary condition is applied. The influence of relaxation time constant values on the heat diffusion speed was investigated for three different values of parameter B; 0.05, 0.50 and 5.00, where the value of 0.5 corresponds to the classic Fourier heat conduction model. For each parameter value, the evolution of temperature in time simulated for the location distant by 1 nm from the left boundary is presented in Fig. 2. As can be seen, all the curves converge to the same steady state value, but the time required to reach half of this value depends on the value of parameter B.

Hence, the speed of heat diffusion processes in this model could be controlled by adjusting the ratio of the relaxation time constants, i.e. the value of parameter B. Therefore, it is possible to simulate thermal processes when heat diffuses either faster or slower than predicted by the classic Fourier theory. Thus, the DPL equation might become a promising alternative for modelling of various experimentally observed nanoscale non-Fourier phenomena using a macroscopic model.

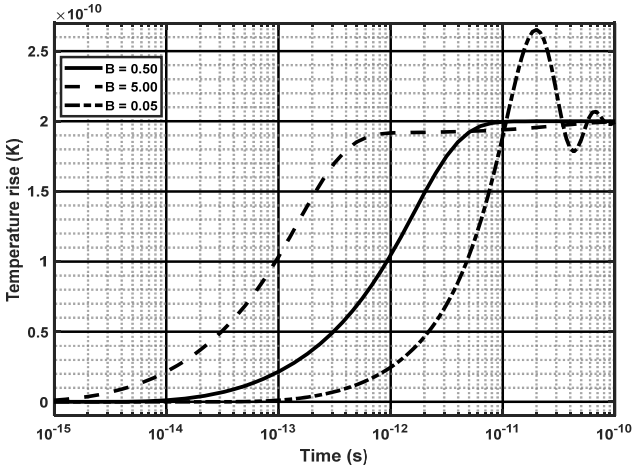


Fig. 2. Time evolution of temperature at 1 nm from the left boundary.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Comparison of the Usefulness of Selected Thermo-sensitive Parameters of Power MOSFETs

Krzysztof Górecki, Krzysztof Posobkiewicz
Department of Marine Electronics, Gdynia Maritime University, Gdynia, Poland
k.gorecki@we.umg.edu.pl, k.posobkiewicz@we.umg.edu.pl

EXTENDED ABSTRACT

The internal temperature of a semiconductor device can be measured using different indirect methods. It is often estimated by measuring the case temperature with a pyrometer recording the intensity of infrared radiation, a thermoresistor or a thermocouple glued to the case of the device under test. However, most commonly, indirect electrical methods are used, in which the value of internal temperature is determined on the basis of the measured value of the electrical parameter of this device with a known temperature dependence (TSP).

For power MOS transistors, the following TSPs are used:

a) v_{GS} voltage at a selected value of drain current i_D for the transistor operating in the saturation range,

b) v_D voltage on the forward-biased junction between the drain and the substrate of the transistor, at the selected value of this junction current,

c) v_{DS} voltage between the drain and the source of a transistor operating in a linear range at a selected drain current (R_{ON} resistance).

This paper presents the results of investigations illustrating the suitability of each of the three above-mentioned TSPs for measuring the internal temperature of the power MOS transistor. For each of the mentioned TSPs, thermometric characteristics are measured at selected drain current values. An analysis of the measurement error of thermal resistance of the power MOS transistor is carried out with the use of each of the considered TSPs. The results of thermal resistance measurements obtained with the use of the considered TSPs and with the use of a thermoresistor are compared and discussed.

The thermometric characteristics of the IRF840 transistor operating at different values of current I_M are measured. Based on the performed measurements, it was found out that only characteristics $v_D(T_j)$ are linear in a wide range of current and temperature changes. The remaining thermometric characteristics are non-linear. In particular, it is worth emphasising that the characteristics of $v_{GS}(T_j)$ show a strong dependence on drain current i_D and on voltage v_{DS}, which may be related to the sub-threshold effect in the tested transistor. The highest slope of the thermometric characteristics was obtained for voltage v_{GS} selected as the TSP.

From the point of view of the evaluation of the thermal resistance measurement error, the error in determining the temperature difference T_j-T_a is of high importance. The relative error in determining this difference depends e.g. on TSP, slope of the thermometric characteristic and the function used to approximate this characteristic.

In order to illustrate the influence of the selection of the TSP and the operating conditions of the tested transistor on the measurement error of R_{th}, the calculations were carried out, the results of which are shown in Fig. 1. In the calculations it was assumed that due to power dissipation in the transistor P = 10 W, at ambient temperature T_a = 20°C, internal temperature T_j increases to 120°C. So R_{th} = 10 K/W. The typical values of the temperature measurement error $\Delta T_a = \pm 0.5$°C and power $\Delta p/p = \pm 0.1\%$ were assumed.

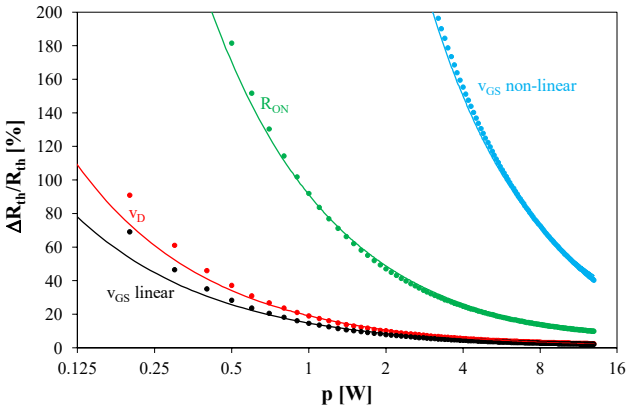


Fig. 1. Dependence of the relative error of the thermal resistance measurement on dissipated power at a selected TSP

As can be seen, the dependnece $\Delta R_{th}/R_{th}(p)$ is a decreasing function for all the considered TSPs. The error values $\Delta R_{th}/R_{th}$ are the lowest when the diode voltage v_D or voltage v_{GS} is used as a TSP with linear approximation of the thermometric characteristic. On the other hand, the use of voltage v_{DS} on the transistor operating in the linear range (proportional to R_{ON}) or voltage v_{GS} as a TSP and approximation of the thermometric characteristic by the quadratic function leads to a much bigger measurement error. The decisive influence on the value of this error is the inaccuracy in determining the coefficients of the function approximating the relation T_j(TSP).

It was found out that the use of linear approximation for the thermometric characteristic allows for a significant reduction in the value of the measurement error R_{th} in relation to the approximation of this relationship by the quadratic function. The smallest measurement error was obtained using voltage v_{GS} as a TSP and linear approximation of the characteristic $v_{GS}(T_j)$ measured for voltage v_{DS} of a few volts and drain current of 10 mA. When using the same TSP and approximating the thermometric characteristic with the quadratic function, the measurement error can be even 10 fold bigger.

Analysis and Modelling of ICs and Microsystems

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

A Simple Method for Analysis of Operation of JLFET THz Radiation Sensors

Michał Zaborowski, Daniel Tomaszewski,
Jacek Marczewski
Lukasiewicz Research Network
Institute of Microelectronics and Photonics
Warsaw, Poland

Przemysław Zagrajek
Institute of Optoelectronics
Military University of Technology
Warsaw, Poland

Extended Abstract

Field-effect transistors (FETs) have been used as room temperature sub-terahertz (sub-THz) radiation detectors, although this frequency range is a few orders of magnitude higher than the FET maximum generation frequency f_{max}. The THz detection has been also confirmed using MOSFETs on SOI wafers with the n-type channel and n^+ source/drain regions (Fig. 1a), which are in fact junctionless FETs (JLFETs). A standard configuration for the THz sensing consists in connecting antennas between the gate and source terminals and a sensitive voltmeter among the drain and source terminals for a DC photoresponse read-out. A small frequency lock-in technique is a standard noise resistant approach for these measurements.

There are two main theories describing THz sensing mechanism: Dyakonov-Shur and resistive mixing models. Both of them poorly relate to JLFET THz sensors and are not suited for a design or optimization of new sensors. Due to this the FETs as THz sensors may be considered as conductive objects of an unknown internal structure ("black boxes).

There are a few methods for characterization of such objects. In this paper we propose a "symptomatic" method of analyzing the operation of radiation sensors (somewhat analogical to the Impedance Spectroscopy). The signal, which is induced in the sensor under THz radiation, has been used for study its internal structure (Fig. 1b). This signal is measured versus gate voltage at the drain output with the lock-in working at the frequency below 1kHz. Both, the signal amplitude and phase, or the real and imaginary parts of the complex output are exploited. The method has been explained on the example on the SOI JLFET sensor. Its voltage and current mode lock-in characteristics were measured under the same radiation conditions (Fig. 1c, d). The admittance $Y(V_g)=I_d(V_g)/U_d(V_g)$ was presented on a graph similar to a Nyquist plot in the frequency domain. The conductance and susceptance as seen by the lock-in at the sensor drain according to $Y=G+j\cdot B$ are shown in Fig. 2. A detailed analysis of these values as function of gate DC bias together with a fundamental knowledge of the MOS transistor phenomena were used for equivalent circuit construction. The analysis of the JLFET sensor operation shows that for the gate bias near V_{th} either the mechanism or a place of the photoresponse signal generation vary. This variation does not occur in the same sensor working with a floating source potential when the photoresponse signal is also generated, although clearly smaller.

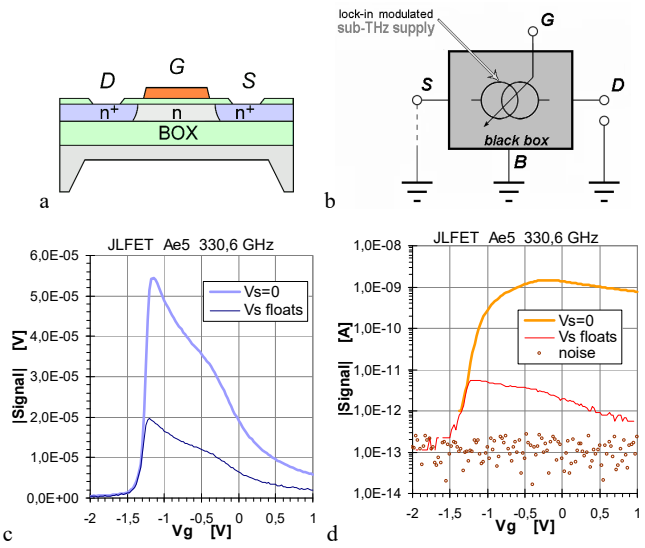


Fig. 1. a) A cross-section of the JLFET sensor; b) a diagram of the proposed analysis method (floating source – optional) c) voltage lock-in measurements; b) current lock-in measurements;

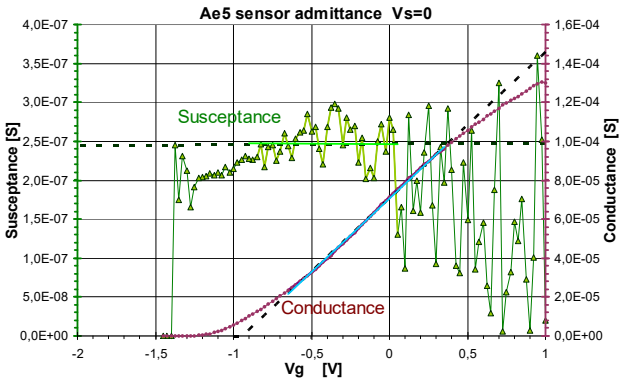


Fig. 2. Susceptance and conductance of the **A** sensor versus gate bias; $V_S=0$; approximation data range - light lines; approximation - dotted black lines.

The proposed method allows both to study the sensor structure and to investigate the principles of the DC signal generation if they are not fully understood. Of course, the area of application of this analysis method is not limited only to JLFET devices, but it is also possible to test other FET-based sensors and transducers.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Application of Maximum Power Point Tracking Algorithm in Simulation of PV Systems

Jacek Nazdrowicz, Mariusz Jankowski
Department of Microelectronics and Computer Science
Lodz Univeristy of Technology
Lodz, Poland
jnazdrowicz@dmcs.pl

EXTENDED ABSTRACT

In this paper modelling and simulation of photovoltaics array in local energy domain systems is presented. Photovoltaics array consists of group of connected PV modules. Thus, connected to energy domain system is building block of a photovoltaic energy conversion system. PV module is the essential power energy conversion unit of a solar energy transformation system. The output characteristics of a PV module are determined by solar irradiance, cell temperature and the output voltage of the PV module. Strong nonlinearity, in turn, enforces to use such energy system using maximum power point tracking (MPPT).

Typical photovoltaic system consists of PV modules (array), MPPT controller, DC-DC converter and optionally - battery pack to store energy excess. MPPT Controller (Maximum Power Point Tracking) is solar charge controller, which detects solar panel voltage and current in real time, thus allowing to track system and extract maximum power out of the PV cell based on specific environmental conditions. These conditions like irradiance or temperature are fundamental quantities for such tracking.

MPP operation of the inverter is in fact related to method of searching the maximum power with current-voltage characteristics use of PV module. In Fig. 1 there is characteristics of I-V and P-V of applied PV panels (330W) for different temperatures T_{cell}. Along with temperature drop the MPP increases (voltage and power increases). Current for different MPPs keeps constant – see results in fig 1: I-V and P-V plots of photovoltaic cell show that open circuit voltage between MPP and 0 and voltage with 0A current is considered as maximum voltage. Short circuit current is related to short circuit at voltage equals to 0. Photovoltaic cells generate maximum power at one specific point and this point visible on plot is simply called Maximum Power Point (MPP).

Because of simple implementation, the Perturb and Observe (P&O) method is commonly used in for tracking of the MPP (Maximum Power Point). The great advantage of this algorithm is high reliability and efficiency. This algorithm is presented in Fig. 2. Current power P generated from photovoltaics is calculated based on the voltage V and the current I. Next, it is compared with the previous value of power P in t-1 point in time. Maximum power is observed when calculated ΔP is zero value. When the power grows, it allows to keep next voltage change in the same direction, similarly to previous change voltage. In other case voltage change in the opposite direction of the previous voltage takes place.

MPPT (Maximum Power Point Tracker) is one of crucial elements of photovoltaic systems – a controller, which is an electronic "smart" DC to DC converter. It optimizes the match between PV panels, and utility grid (in case of "on-grid" system). Basically, it is an interface between load and PV cells – it controls duty cycle to obtain maximum power of the PV cell, taking into consideration environmental conditions like grid demand. DC-DC converter output may also be utilized to charge the batteries in case of off-grid systems.

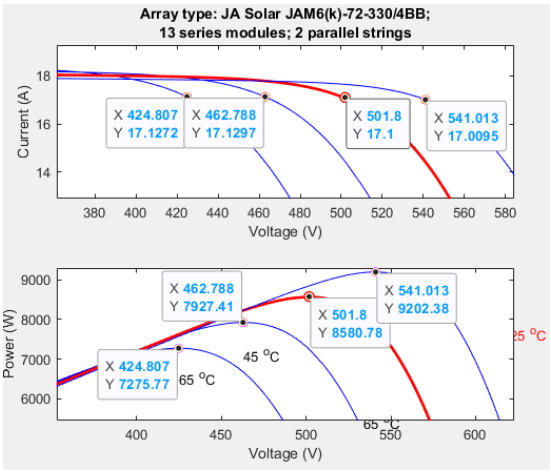


Fig. 1. I-V and P-V plots for different temperatures and irradiation environmental conditions for considered PV module type.

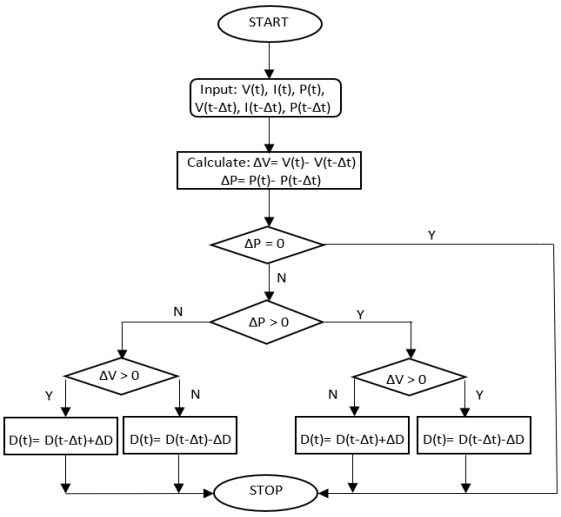


Fig. 2. MPPT Perturbation and Observe algorithm.

Development of PSpice Macromodel for Monolithic Single-Supply Power Amplifiers

Ivailo M. Pandiev
Department of Electronics, Technical University of Sofia, Sofia, Bulgaria
ipandiev@tu-sofia.bg

EXTENDED ABSTRACT

A. Macromodel Development

Several semiconductor manufacturers, such as Maxim®, Analog Devices®, Philips®, Sanyo®, Samsung®, SGS Thomson®, ST Microelectronics®, and Texas Instruments® offer commercially available various types of monolithic power amplifiers. One of the basic monolithic integrated power amplifiers is those of the ST Microelectronics from the TDA – series. In Fig. 1 is a simplified circuit diagram of a TDA2030 power amplifier is given. As can be seen, the electrical circuit is divided into three sections (or stages): input stage, intermediate (or driver) stage and output stage. In addition to the main amplifier stages, the chip also includes thermal protection and current limiting circuits.

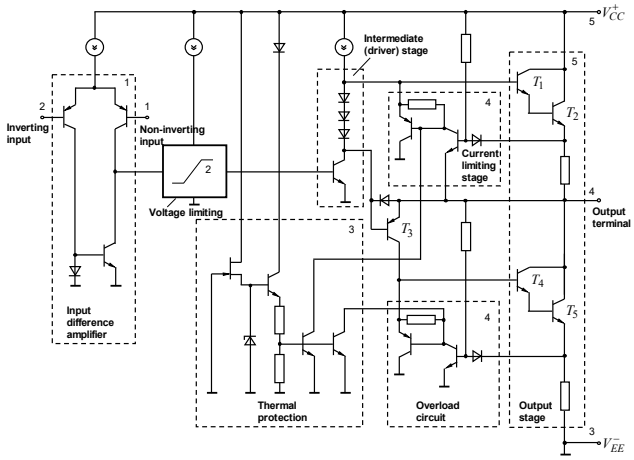


Fig. 1. A simplified circuit diagram of a TDA2030 from TDA – series.

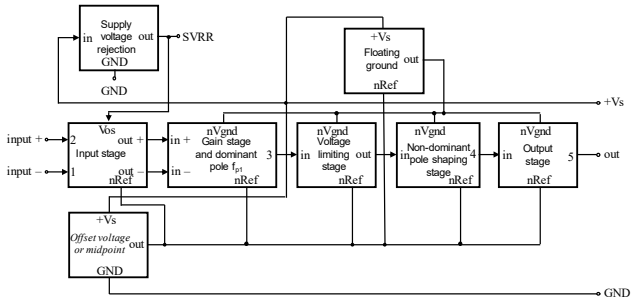


Fig. 2. Block diagram of the proposed macromodel for power amplifiers.

Based on the simplified circuit diagram in Fig. 1, a block diagram of the proposed model (Fig. 2) is developed. In Fig. 2 the block diagram includes an input stage, intermediate stage and output stage connected in a cascade structure. Additionally, three blocks are connected to the structure, providing the midpoint of the model, the floating ground and the supply voltage rejection ratio. According to the complexity of the amplitude-frequency characteristic of a concrete amplifier, the number of frequency-shaping stages can be increased, as well as it can be change the structure of the stage modeling the suppression of the pulsations of the supply voltage.

B. Pspice implementation

To develop PSpice macromodel for monolithic power amplifiers simplification and build-up techniques for macromodeling of operational amplifiers is used. Based on the block diagram, given in Fig. 2, the macromodel is implemented as a two-level hierarchical structure. The higher-level block diagram with the modeling parameters is defined as black box.

The equivalent circuit (lower-level) includes both standard PSpice components and analog behavioral modeling (ABM) blocks. The usage of ABM blocks, such as various controlled sources, provides the implementation of linear and non-linear mathematical functions in the PSpice program. The external interface terminals of the circuit are non-inverting input (*input+*), inverting input (*input–*), an output terminal (*out*), supply voltage ripple rejection terminal (*SVRR*), positive power supply (*+Vs*), and analog ground (*GND*).

C. Modeling Parameters and Verification

The proposed macromodel is developed using simplification and build-up techniques for macromodeling of operational amplifiers and simulates the basic static and dynamic characteristics, including input impedance, small-signal frequency responses at various voltage gains, output power versus supply voltage, slew-rate-limiting, voltage limiting, output offset voltage versus supply voltage ripples and output resistance. Further, the macromodel also takes into account ground reference voltage in the amplifier at a single power supply voltage.

The accuracy of the model has been verified by comparing the simulation results of the electrical parameters with corresponding measured values by experimental testing of sample circuits. The comparative analysis shows that the relative error for the modeled large-signal parameters is less than 15%. Moreover, an error of 15% is quite acceptable, considering the technological tolerances of the electrical parameters for this type of analog ICs.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Study of Nanowire Characteristics of a Junctionless Transistor Depending on the Gate Length

Rostislav Rusev[1], George Angelov[2], Ivelina Ruskova[2], Elitsa Gieva[2], Dimitar Nikolov[3], Mariya Spasova[2], Marin Hristov[2], Rosen Radonov[2]

[1] Department of Technology and Management of Communication Systems, Technical University of Sofia, Bulgaria
[2] Department of Microelectronics. Technical University of Sofia, Bulgaria
[3] Department of Electronics, Technical University of Sofia, Bulgaria
rusev@ecad.tu-sofia.bg, george_angelov@smartcom.bg, angelov@smartcom.bg, ruskova@ecad.tu-sofia.bg, gieva@ecad.tu-sofia.bg, dnikolov@tu-sofia.bg, m.spasova@tu-sofia.bg, mhristov@ecad.tu-sofia.bg, marin_hristov@smartcom.bg, rossen.radonov@ecad.tu-sofia.bg

EXTENDED ABSTRACT

To surmount the semiconductor device scaling limitations new device structures and new materials are being developed and implemented. One representative of the above solutions is the junctionless nanowire transistor invented by *J. P. Colinge* in 1996 [1]. This transistor is very perspective because it enables the best possible channel control by the gate and consequently, utmost control of short-channel effects [2] with maintaining compatibility with existing CMOS technology.

The transistor is junctionless because its channel is a nanowire [3]. The current in the channel is controlled by the gate voltage applied over the nanowire. The nanowire is highly doped to enable enough carriers for the channel current when the device is on and the nanowire is thin to enable full depletion of carriers when the device is off; depletion is caused by the work-function difference between the gate and the doped Si.

Technology modeling of junctionless transistor structures is carried out in commercial software suits such as COMSOL [4], Synopsis Sentaurus [5], etc. These models are based on the equations of Poisson and Boltzmann. The research focus so far is mainly on the impact of channel thickness and channel width upon charge distribution and carrier concertation [6]. These concentrations shape the *IV* characteristics of the transistor. Furthermore, the impact of the randomly distributed dopant in the nanowire is also studied [7].

The influence of the charge distribution along the nanowire over the *IV* characteristics of the junctionless transistor is not well enough studied. In this paper we investigate the influence of the channel length (under the gate) upon the charge distribution and carrier concertation in the nanowire.

For this reason, we constructed a simplified 3D model of the junctionless transistor consisting of highly doped Si-nanowire covered with SiO_2 layer with software defined terminals of source, drain and gate. In all simulations we have constant thickness, length and width of the nanowire as well as the oxide layer. We vary the gate length along the nanowire.

We modeled characteristics of a nanowire for 7 gate lengths: 10, 20, 30, 40, 50, 60, 70 nm. For each gate length we set V_{DS} = 0.05 V and we vary V_G between 0.1 to 0.8 V. A number of parameters such as carrier confinement, effects of parallel and transverse field-dependent mobilities, and carrier scattering due to Coulomb effects, acoustic phonons, impurity doping profile and surface roughness influence the transport process in the active regions.

The developed 3D model of a simple nanowire junctionless transistor is in a good agreement with the models presented by other authors. It demonstrates the quantum confinement effect for the silicon-oxide interface. These effects implemented in the model result in accurate description of transistor behavior. The analysis of the function of electron concentration versus gate length proved that it is desirable to use transistors with as small gate length as possible.

This paper is part of the research within the RADICAL project funded by the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement No. 899282.

REFERENCES

[1] J. P. Colinge, X. Baie, V. Bayot, E. Grivei, "A silicon-on-insulator quantum wire", Solid State Electronics, Vol. 39, Iss. 1, pp. 49-51. 1996. DOI 10.1016/0038-1101(95)00094-A

[2] C.-W. Lee, S.-R.-N. Yun, C.-G.Yu, J.-T. Park, J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs", Solid State Electronics, Vol. 51, Iss. 3, pp. 505-510. DOI 10.1016/j.sse.2006.11.013.

[3] J.-P. Colinge, C.W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, R. Murphy, "Nanowire transistors without junctions", Nature Nanotech, Vol. 5, pp. 225–229, 2010. DOI 10.1038/nnano.2010.15

[4] 3D Density-Gradient Simulation of a Nanowire MOSFET, Application ID: 73771, COMSOL. https://www.comsol.com/model/3d-density-gradient-simulation-of-a-nanowire-mosfet-73771

[5] Synopsis Sentaurus, https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html

[6] A. Nowbahari, A. Roy, M. N. Akram, L. Marchetti, "Analysis of an Approximated Model for the Depletion Region Width of Planar Junctionless Transistors", Electronics, Vol. 8, Iss. 12, pp 1-19 2019. DOI: 10.3390/electronics8121436

[7] N. D. Akhavan, G. A. Umana-Membreno, R. Gu, J. Antoszewski, L. Faraone, "Random Dopant Fluctuations and Statistical Variability in n-channel Junctionless FETs", Nanotechnology, Vol. 29, No. 2, 025203, pp 1-7, 2017.

Power Electronics

A Four-Phase Gain Control Method to Reduce the Ignited Current Spike of the Laser Diode Using in a Laser Headlight Power Supply Unit

Kai-Jun Pai
Undergraduate Program of Vehicle and Energy Engineering
National Taiwan Normal University
Taipei City, Taiwan (R.O.C.)
carypai@ntnu.edu.tw

EXTENDED ABSTRACT

In this study, a laser headlight power supply unit (LHPSU) was used to drive the InGaN-based laser diode for high-beam headlights. Due to an vehicle battery supplies power source to the LHPSU, the changeable battery voltage has to be considered. Therefore, the LHPSU employed a buck–boost converter (BCC) as the LHPSU power stage. This power conversion topology can achieve a buck or boost conversion for the ignition and driving of the laser diode. Otherwise, an LHPSU constant-voltage or constant-current (CC) output mode can be implemented using a voltage error amplifier (VEA) or current error amplifier (CEA) control, and the CEA with a four phase gain (FPG) control strategy can mitigate the ignition current spike when laser diodes are under the high ambient air temperature (AAT) and decreased forward cut-in voltage.

In Fig. 1, the LHPSU system possessed with the the BBC, an BBC controller, a voltage divider, a current detection shunt R_{shunt}, a voltage signal amplifier (VSA), and a CEA. The input side of the LHPSU can input the DC power from an on-board battery. At the LHPSU output side, three laser diodes collocated with condensing lenses can emit laser beams with a wavelength about 450 nm, which can be projected to a yellow phosphor for generating white light.

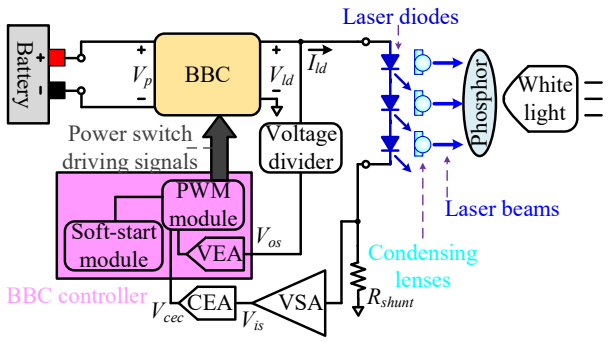


Fig. 1. LHPSU system configuration.

The output current stability of the LHPSU can be controlled through the CEA with the proportional-integral (PI) control, which can provide the high low-frequency gain, the phase margin of 45°-tolerance, and the small steady-state error. However, the LHPSU operates in the buck mode, the integral operation of the PI causes the ignition current spike. If the spike exceeds the maximum operating current of the laser diode, the semiconductor materials are damaged resulting in OOP decay. To improve the tardy defect of the CEA from the integral operation, this study proposes an FPG control. Using the FPG technology, the CEA can change control processes to implement the soft-start (SS), proportional (P), maximum low-frequency gain (MLFG), and PI controls.

Fig. 2 includes a control block diagram and control circuit. for the CEA with the FPG control. Fig. 1 indicates that the driving current of the laser diode can be detected using a R_{shunt} to become a voltage signal, which can be amplified using a VSA to obtain the output voltage V_{is}. Thus, the CEA can compare the V_{is} with a current reference voltage $V_{Ild(ref)}$ to generate an error signal V_{cec}, which can control the PWM module inside the BBC controller. In consequence, the PWM module outputs PWM signals to driver power switches, and then the LHPSU output voltage and current can be control by the PWM module.

This study proposes an FPG control process for the CEA operation. The ignited current spike was effectively suppressing.

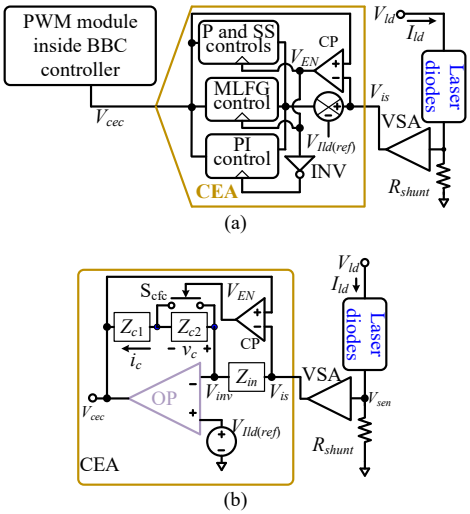


Fig. 2. CEA uses FPG control. (a) Control block diagram. (b) Control circuit.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Application of Thin Film Ultralow-Power Lead-Free Perovskite Solar Energy Harvesters in Power Management Systems

Mariya Aleksandrova
Department of Microelectronics
Technical University of Sofia
Sofia, Bulgaria
m_aleksandrova@tu-sofia.bg

Ivailo Pandiev
Department of Electronics
Technical University of Sofia
Sofia, Bulgaria
ipandiev@tu-sofia.bg

***Abstract*—Lead-free thin film perovskite solar cell is fabricated and characterized in terms of short-term stability at temperature and light exposure intensity variations. The performance of the proposed energy harvesting element is analyzed for its applicability to charge a supercapacitor. Two possible power management systems are studied and recommendation for using is given based on the charging rate. It is found that the combination of quantum dots with lead-free perovskites expands the absorption in the visible spectrum below 500 nm, which improves the spectral sensitivity of the cell and stabilizes its response at white light. It is found that the power processing system with discrete components exhibits maximum charging rate of 1.2 mV/min, vs. 53 µV/min obtained with monolithic DC-DC convertor, which results in faster reaching the full capacity of the supercapacitor for less than 5 hours (the typical charging time of the selected storage element). The temperature instability of the output electrical power during this time is 1.8 %/°C at maximum light intensity of 10 000 cd/m^2. This is superior, when compared to the non-perovskite thin film solar cells, exhibiting typical instability values of 2-2.2 %/°C.**

***Keywords*—solar energy harvesting; lead-free perovskites; thin film solar cell; DC-DC converters; power management**

Extended Abstract

Studies on the application of lead-free perovskite solar energy harvesters in power management systems have not been conducted yet. In this paper, both the temperature and the light intensity were varied and their effect on the short-term stability of the open-circuit voltage and electrical power, produced from novel LFPSCs was monitored. The cell was connected to a supercapacitor (SC) through a suitable power management system to demonstrate the short-term stability by charging it, and thus proving the applicability of the lead-free materials as thin film ultralow-power solar energy harvesters. The structure of the fabricated solar energy harvester is shown in Fig. 1. The proposed structure of low-power management system was experimentally tested, and the experimental setup is shown in Fig. 2. Block diagrams of the studied power management system, which can be used for the fabricated thin film solar energy harvesting device are shown in Fig. 3 and Fig. 4. Fig. 5a and 5b show the SC charging dynamics in the case of low-power management system from Fig. 3 and Fig. 4, respectively. The circuit with discrete components is simpler, and easier to implement. It can be used with a small number of solar cells, as the charging time is significantly shorter and can operate with a low current (up to several µA). However, for them the maximum charging voltage is limited and depends on the value of the input voltage and the voltage drops on the electronic elements used.

The work was funded by Bulgarian National Science Fund, grant No KP06-Inia-6 under bilateral cooperation program Bulgaria-India.

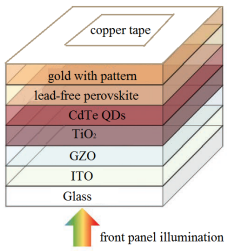


Fig. 1. The structure of the proposed LFPSC.

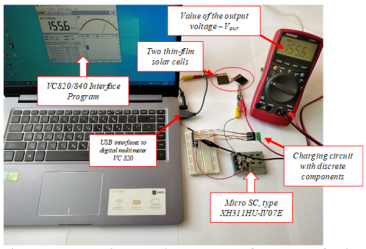


Fig. 2. Experimental setup of one of the proposed power management system for low-power solar energy harvesters.

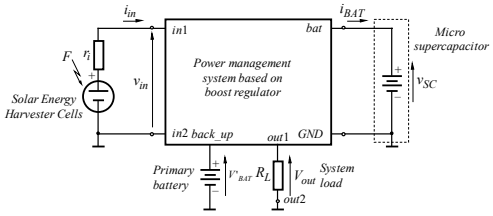


Fig. 3. Block diagram of a power management system intended for low-power solar devices with monolithic element.

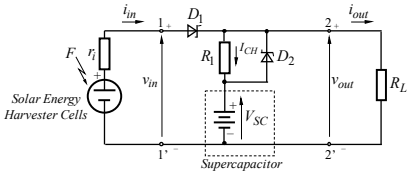


Fig. 4. Basic charging circuit with discrete components for low-power solar devices with discrete components.

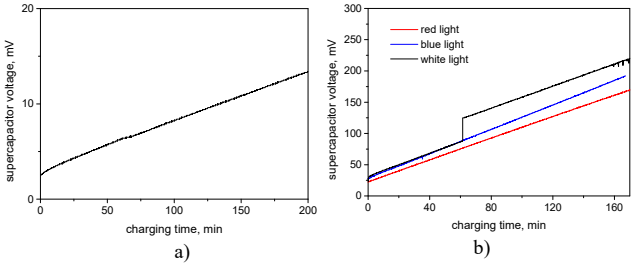


Fig. 5. Data extraction for the SC voltage as a function of the charging time using power processing system: a) with a monolhitic DC-DC converter; b) with discrete components.

Dedicated Multi-element Electronic System for Personalized Protective Thermally Active Clothing

Bartosz Pękosławski,
Paweł Marciniak, Łukasz Starzak, Adam Stawiński
Department of Microelectronics and Computer Science,
Lodz University of Technology
Lodz, Poland
bartosz.pekoslawski@p.lodz.pl

Grażyna Bartkowiak
Department of Personal Protective Equipment
Central Institute for Labour Protection - National Research Institute
Lodz, Poland
grbar@ciop.lodz.pl

Extended Abstract

The article presents the multi-element electronic system for the "Personalized Protective Thermally Active clothiNg (sPParTAN)" project carried out by the consortium of the Department of Microelectronics and Computer Science of the Lodz University of Technology, the Central Institute of Labour Protection and the PSA Małachowski company (mountaineering equipment producer). The project concerns personalised protective clothing for mountain rescuers, equipped with functions of automatic heating and harvesting energy from alternative sources, which is an innovative solution on a national scale. The obtained product integrates modern solutions from the field of electronics, IT, clothing and labour protection.

The mountain rescuers need special clothing which provides user's thermal protection. Traditional clothing is based on multilayer materials to achieve good thermal isolation. This approach is disadvantageous because of lower user's mobility and inconvenience. One can improve clothing thermal isolation by the application of active heating components. Such solutions are widely used in a wide range of commercially available electrically clothes. The described heating system is aimed to gather necessary data in real conditions for the automatic control algorithm development. This system is much more complex than competitive products of this type but may be simplified in a final version after analyzing the information obtained from in-field tests.

It is beneficial to achieve the system operation as long as possible with the use of just one set of batteries, also in unfavorable thermal conditions. The optimization of the heating system power consumption is achieved by an advanced control taking into account environmental conditions and body microclimate. This control requires the use of sensors and can considerably increase heating system effectiveness. The types and locations of the sensors need to be chosen carefully so that their output signals can be correctly read and interpreted by the control unit. The control algorithm is supposed to optimize the electric energy consumption and adapt to the user's preferences.

System optimization also requires the power loss in its main power converter to be minimized. This required a suitable model to be used at the design stage enabling power loss estimation in the particular components. An additional system operation time increase is to be brought by the use of flexible photovoltaic (PV) modules. The use of anthropomorphic measurements can be also useful for clothing template personalization and its optimization for a given user.

The system is composed of two main parts: the control unit with sensors and the power supply module with heating components, Li-ion battery pack and PV modules. The power supply module is responsible for power conversion and delivery to the heating components and to the control unit. The estimated maximum power requirement for the control unit is 106.1 mW and for the heating components up to 100 W. Thus the efficiency of the main voltage converter, which powers the heating components, is critical for the system operation time and its value ranges from 95.5 % to 97.0 % for the expected output currents. Characteristics of the main converter (Figure 1) measured on a prototype showed a high agreement with simulations. The resulting system operation time is from 52 min to 5 h 50 min and the increase due to the battery pack charging by the PV modules can reach 43 min.

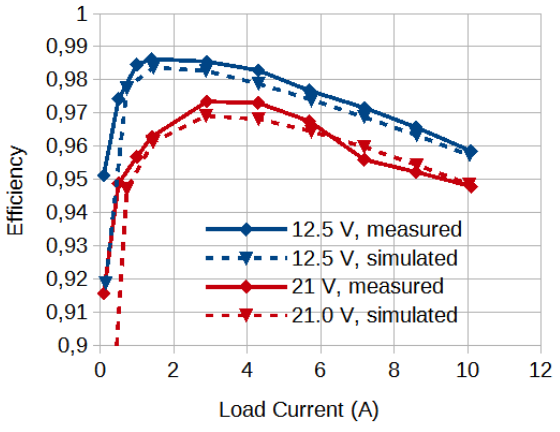


Figure 1. System efficiency measured as compared to the main converter efficiency estimated by simulation

Design of an Overcurrent Protection Relay Based on Electronics Technology

Babak Agheli, Arash Kalami
Department of Electrical Engineering
Urmia Branch, Islamic Azad University
Urmia, Iran
babakas2018@gmail.com, a.kalami@iaurmia.ac.ir

Abdollah Amini
Department of Electrical Engineering
Sina Bioelectronics Company (SBC)
Urmia, Iran
amini.sbc@gmail.com

***Abstract*—Protection relays are essential components in distribution networks that are used to protect the interphase faults and single-phase-to-ground faults. However, these relays do not assurance the protection due to the sharp growing short circuits. They may be the result of demanding more and more power usage by the commercial and residential users. Overcurrent relay (OCR) is the cost-effective and broadly used element in power system protection. In this paper, the design of an overcurrent relay in 0.18µm CMOS standard technology is performed for the protection of the 10-kilo-volts distribution system against the undesired currents. In this case, we have considered a time-reversed type relay where the operation time of the relay has a reverse proportion with its current. Firstly, crucial features of the relay are converted into digital data using electronic circuits including; encoder, analog to digital converter (ADC), multiplier, etc. In the next step, using an analog comparator leads to having the results of the comparison between the relay nominal-current and the actual line current. Finally, the value and the duration of the overcurrent are compared with the relay characteristics and the output results will ensure the circuit to continue the operation or not. Therefore, the proposed relay guarantees the protection of the system by overcurrent detection and cutting-off the system in the critical situations in a safe and fast way. Simulation results through Hspice can strongly prove the proper operation of the proposed overcurrent relay.**

***Keywords*—Overcurrent relay, current transformer (CT), CMOS Technology, Analog to Digital Converter, Comparator**

I. Proposed System

As shown in Fig. 1, the proposed OCR consists of five main blocks: an analog comparator, a timer, two registers, a digital comparator, and a relay time-current (standard inverse) characteristics extraction block. Each block of the proposed system is described in detail in the following subsections. The operation of OCRs depends on two conditions. Firstly, the passing current from the relay ($I\text{-}_{Line}$), measured by CTs, should be greater than the relay setting current ($I\text{-}_{Setting}$). Therefore, an analog comparator placed at the input of the system, which compares two input voltages together. To convert the currents into required input voltages for the comparator, two resistors should be employed. Hence, when I_L is larger than I_S, the comparator starts to work. Secondly, the permanent duration of the first condition should be greater than the relay activation time (for example, 20 seconds). For this reason, a timer has been utilized after the comparator. After comparison, when the comparator output changes from "0" to "1", the timer starts to count, and the registers 1 and 2 get the inputs by the specific clock pulse. The AND gates are responsible to drive the registers. The comparator output is directly connected to one of the inputs of each AND gates. When the comparator output is "0", AND gates are inactive, but when it becomes "1", the clock pulse activates the registers through the AND gates. Then, at the final stage, registers' output is compared together using a digital comparator. If the value of measured time by register 1 is greater than the value of register 2 (A>B), the output of the digital comparator becomes "1" and activates the circuit breaker.

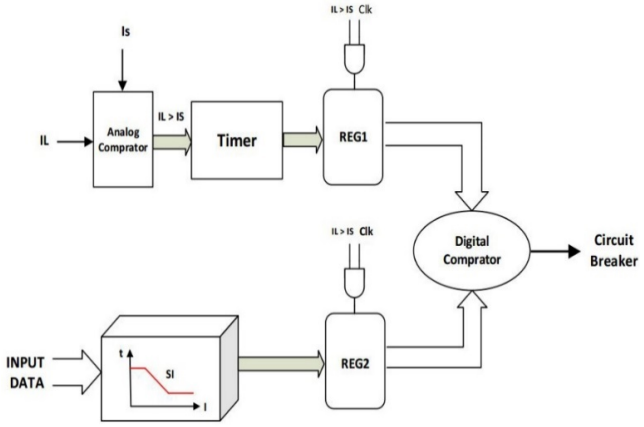


Fig. 1. Block diagram of proposed overcurrent relay

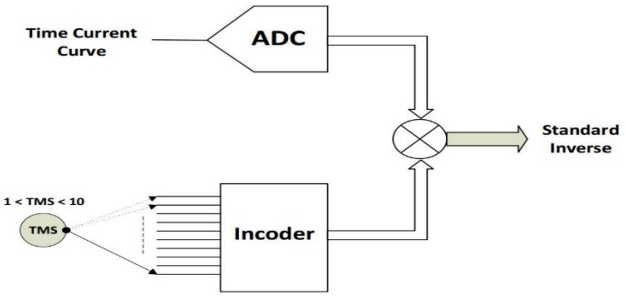


Fig. 2. Standard SI features extraction block

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

New Monolithic Multi-terminal Si-chips Integrating a Power Converter Phase-leg for Specific Applications

Amirouche Oumaziz[1,2], Abdelhakim Bourennane[1], Frédéric Richardeau[2]
[1] LAAS-CNRS, University of Toulouse, CNRS, UPS, Toulouse, France
[2] LAPLACE, University of Toulouse, CNRS, INPT, UPS
2 rue Charles Camichel, BP 7122, F-31071 Toulouse cedex, France

***Abstract*—The paper deals with the monolithic integration of a power converter phase leg. It focuses on the integration of a power phase leg consisting of a VDMOS and an IGBT. This association is suitable for monolithic power integration in silicon. Different monolithic chips integrating phase legs were proposed and discussed in this paper. Interesting advantages can be brought by the monolithic integration of the converter phase leg. These advantages include power chips realization simplification, control of gate transistors with respect to constant voltages.**

***Keywords*—P-IGBT; N-VDMOS; monolithic integration; power conversion; switching cells.**

I. INTRODUCTION

Currently commercialized conventional power modules are generally realized using 2D hybrid packaging technology in which two-terminal power dies such as IGBT and PiN-diode are soldered on their backside and interconnected using wire bonds. A power module is made of a great number of two-terminal dies that are interconnected by wire bonds. Power modules are therefore bulky and their mass fabrication is limited in productivity. Wire bonds require an expensive wiring operation and are a source of reliability problems [1]-[3]. Moreover, they are a source of stray inductance [4] that limits the frequency of operation of the power modules.

In this paper, new multi-terminal power chips were proposed for monolithic phase leg integration. The integrated phase legs are illustrated in Figure 1. The converter of Figure 1 is a current reversible DC/DC buck converter. In the case of Figure 1, the phase leg consists of a high side P-IGBT and a low side N-VDMOS.

II. PRINCIPLE OF THE APPROACH

By mutualizing the backside N^+ regions of a P-IGBT and an N-VDMOS, the monolithic chip of Figure 2.a is proposed. It consists of a vertical N-VDMOS and a vertical P-IGBT separated by deep but not through silicon trenches [5]. This latter can be filled by an insulator [6]-[7] (Figure 2.b). The same principle stands for a P-VDMOS and an N-IGBT by mutualizing the common P^+ backside region (full paper).

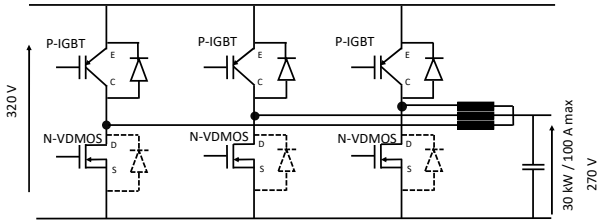


Figure 1. Converter leg typical applications for the DC/DC buck converter

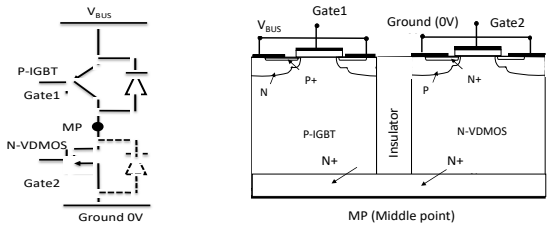


Figure 2. Cross-sectional view of the proposed monolithic chip integrating the phase leg P-IGBT (high side) and N-VDMOS (low side) (a), N-IGBT (low side) and P-VDMOS (high side) (b).

III. CONCLUSION

In this paper, original monolithic chips integrating converter phase legs were proposed. From the technology process realization point of view, these multi-terminal chips do not require the realization of through silicon deep trenches [6] and therefore their realization is not complex. The operating modes of the chips were validated in a boost converter application using 2D Sentaurus™ mixed-mode simulations. The design approaches were illustrated and validated in an a 100V, 48A application. An improved version of the multi-terminal chip was proposed. It uses a depletion mode P-MOS transistor in series with the P-IGBT in order to limit the current through this latter mainly in the case of a short-circuit condition and therefore prevents P-IGBT latch-up.

REFERENCES

[1] B. Weiss *et al.*, "Operation of PCB-Embedded, High Voltage Multilevel-Converter GaN-IC," 2017 *IEEE 5th Workshop on Wide Bandgap Devices and Applications (WiPDA), Albuquerque, NM,2017,pp. 398-403.* doi: 10.1109/WiPDA.2017.8170580

[2] S. QiN et al., "A High-Power-Density Power Factor Correction Front End Based On Seven-Level Flying Capacitor Multilevel Converter," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1883-1898, Sept. 2019. doi: 10.1109/JESTPE.2018.2865597

[3] S. Li, L. M. Tolbert, F. Wang and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," in *IEEE Transactions on Power Electronics*, vol.29, no.7, pp.3616-3624, July2014. doi: 10.1109/TPEL.2013.2279258

[4] A. K. Solomon, A. Castellazzi, N. Delmonte and P. Cova, "Highly integrated low-inductive power switches using double-etched substrates with through-hole viases," *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hong Kong, 2015, pp. 329-332. doi: 10.1109/ISPSD.2015.7123456

[5] A. El Khadiry, A. Bourennane and F. Richardeau, "Multiphase Power Converter Integration in Si: Dual-Chip and Ultimate Monolithic Integrations," in *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1977-1983, May 2016. doi: 10.1109/TED.2016.2537212

[6] L. Theolier, H. Mahfoz-Kotb, K. Isoird, F. Morancho, S. Assie-Souleille and N. Mauran, "A New Junction Termination Using a Deep Trench Filled With BenzoCycloButene," in *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 687-689, June 2009. doi: 10.1109/LED.2009.2020348

[7] Chanho Park, Jinmyung Kim, Taehoon Kim and D. J. Kim, "Deep trench terminations using ICP RIE for ideal breakdown voltages," *ISPSD,* 2003, pp. 199-202. doi: 10.1109/ISPSD.2003.1225263

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Spatial Radiation Patterns of Selected Solid State Light Sources

Krzysztof Górecki, Przemysław Ptak, Łukasz Bruski
Department of Marine Electronics
Gdynia Maritime University, Gdynia, Poland
k.gorecki@we.umg.edu.pl, p.ptak@we.umg.edu.pl, lukaszbruski1988@gmail.com

EXTENDED ABSTRACT

The main components of solid state light sources are LEDs. Manufacturers of these semiconductor devices provide information on the parameters of the LEDs they produce, including the value of the emitted luminous flux and spatial radiation patterns. However, the luminous flux emitted by a single LED has a low value. Therefore, in the construction of lighting systems, typically LED modules are used, containing from several to several dozen LEDs placed on a common base. For such systems, the emitted luminous flux is not equal to the sum of the luminous fluxes emitted by each of the used LEDs. Therefore, in order to determine the parameters of the emitted light, it is necessary to perform the appropriate measurements.

The classic method for measuring the luminous flux emitted by electric light sources requires the use of a photometric sphere and a radiameter. However, this method of measurement does not allow determining spatial radiation pattern. The way to measure spatial radiation patterns is to use a goniometer.

Spatial radiation patterns of power LEDs, LED modules and LED lamps were measured with the use of the goniometer constructed by the authors. As an example spatial radiation patterns of the rectangular LED module containing 8 LEDs is presented.

For rectangular modules, the arrangement of the module may have a significant influence on the measurement results. Fig. 1 shows the spatial radiation patterns of a rectangular LED module containing 8 LEDs arranged in two rows of 4 LEDs. Measurements are made with the tested module mounted in two perpendicular axes.

As can be seen, spatial radiation patterns measured by mounting the module along the short and long axes of the module differ from each other. This means that the photometric body is a revolving body. It can be seen that the characteristics measured along the short axis of the module are characterized by a greater beam angle. The differences in the luminous intensity values obtained for the selected viewing angles differ even twice and are particularly clearly visible for high values of the viewing angle.

Of particular interest are the results of the measurements carried out for solid state light sources containing a high number of LED dies. For example, in an LED containing 4 independently power supplied semiconductor dies and a common lens, spatial radiation patterns are obtained with the shape depending on the number of simultaneously power supplied diodes. The shift in the direction, in which the maximum radiation intensity is observed, is even 15°.

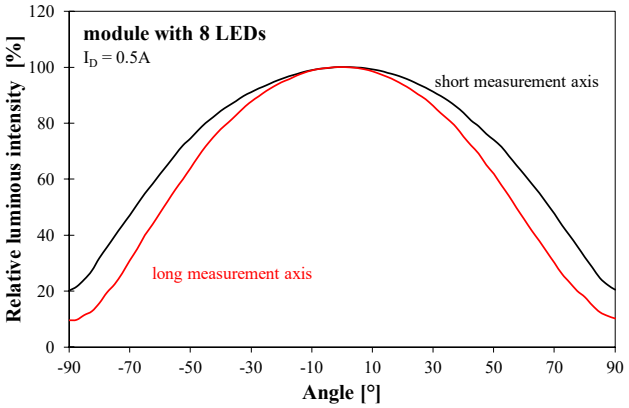


Fig. 1. Spatial radiation patterns for the LED module containing 8 LEDs

LED modules containing connected in series LEDs placed on the circle of the small diameter exhibit the same shape of spatial radiation pattern as the individual LEDs contained in these modules. In turn, rectangular shaped LED modules exhibit different shapes of spatial radiation patterns depending on the spatial orientation of the axis of this module. Such modules have a wider range of the viewing angle, in which the highest illuminance is observed, in relation to the LEDs used to construct these modules.

LED lamps, depending on their purpose, may be characterized by significant differences in the values of the viewing angle. Also, some of the LED lamps show differences in spatial radiation patterns measured when the goniometer arm is moved in different axes. These differences are slight and do not exceed a few degrees.

Based on the measured spatial radiation pattern and illuminance measurements, values of the emitted luminous flux were determined using the method described by us in. Comparing the obtained results with the values declared by the manufacturer, it was found out that this method allows obtaining the correct values of the luminous flux only when the photometric body of the emitted light is a rotating body. Thus, it can be used successfully for light sources containing individual LEDs or LED modules containing LEDs situated on a circle.

Signal Processing

Comparison of the Effectiveness of the Methods of Recording Physiological Signals Using Passive Electronic Sensors to Obtain Respiratory Parameters in People with Respiratory Dysfunction

Ilona Karpiel, Jakub Wołoszyn, Kamil Olesz, Maciej Mysiński, Mirella Urzeniczok, Daniel Feige, Aleksander Sobotnicki, Marek Czerw*
Łukasiewicz Research Network – Institute of Medical Technology and Equipment
Zabrze, Poland
ilona.karpiel@itam.lukasiewicz.gov.pl, marek.czerw@itam.lukasiewicz.gov.pl

EXTENDED ABSTRACT

Chronic respiratory diseases, including respiratory tract diseases - chronic obstructive pulmonary disease (COPD) and asthma - are leading in terms of morbidity, mortality, and consequently increased economic and social costs. COPD is a disease resulting from an abnormal response of the lungs to irritants in the air. It is a common disease that is preventable and, if it occurs, can be effectively treated.

The topic of air pollution has been intensively studied; infrom 2015 to 2021, more than 327,000 publications related to this topic were published in the PubMed database, which indirectly indicates the extent of the problem. In recent years, there have also been studies on the impact of pollution on the development of acute as well as chronic diseases. An analysis of 10 European cohorts showed an association between transport-related air pollution and pneumonia, and to a lesser extent otitis media in the first 2 years of life. The harmful effect of environmental factors is known in interstitial lung diseases (ILD) such as asbestosis and silicosis. Recently, also air quality has been indicated as a probable risk factor for the development, progression as well as exacerbation of interstitial lung diseases through oxidative stress, impaired fibrogenesis, and induction of inflammation. Among ILDs, air quality probably plays the greatest role in lung fibrosis itself.

The effects of poor air quality on the respiratory system are undeniable and multidirectional. Some conclusions should be approached with some caution, especially when results are inconclusive. Unfortunately, there are no studies that can be standardized because of the influence of many variables: different types of pollution (traffic, railroads, factories), climate, wind influence, population behavior (time spent away from home), the susceptibility of individuals (asthma, COPD). This topic requires a deeper local analysis, especially considering that in Poland air pollution contributes to 26,589 premature deaths per year. Various projects are currently being implemented to improve air quality - replacement of coal stoves, signs informing about current measurements, free public transport when levels are exceeded. Some countries predict that soon it will be possible to predict the occurrence of acute health events based on monitoring gas concentrations, and thus provide necessary medications, and prepare medical personnel.

The purpose of the work is to developed two sensors, based on piezoelectric and resistive elements, used to measure the respiratory signal from the thorax. As a result two innovative methods of monitoring respiratory parameters and cough incidents for patients with respiratory failure, caused by asthma or covid-19. The first sensor was made of the piezoelectric membrane, and the second uses conductive elastic rubber that changes its resistance when stretched. Both sensors were placed on the patient's chest using a specially designed for this purpose belt.

Simultaneous biomedical signals were recorded in laboratory conditions for various measurement methods, which showed chest movement during breathing in healthy people with the simulation of difficult measurement conditions, such as shallow and rapid breathing, slow deep breathing combined with apnea, and in the presence of motor disturbances. The obtained results for both measurement methods allow confirming a satisfactory immunity to movement disturbances and correct detection in extreme measurement conditions such as fast and shallow breathing and apnea while the piezoelectric method, enables recording with better resolution in conditions of fast and shallow breathing. Both piezoelectric and resistive methods are correct for creating sensors that monitor basic patients' respiratory parameters. Their additional advantage is the simplicity and low cost of production which may be important in examining geriatric patients and neonates however piezoelectric is cheaper and less burdensome during the long-term recording of respiratory parameters

ACKNOWLEDGMENT

This work was supported by the resources of the National Centre of Research and Development, Poland, within the framework of the Smart Growth Operational Programme, POIR.04.01.04-00-0060/19.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Safety Application Car Crash Detection Using Multiclass Support Vector Machine

Mike Schwarz [1,✠], Alexander Buhmann[2]
[1]NanoP, Technische Hochschule Mittelhessen - University of Applied Sciences, Germany
[2]Robert Bosch GmbH, Germany
✠mike.schwarz@ei.thm.de

***Abstract*—In this paper, the application of Support Vector Machine (SVM) on multiple car crash situations for improved decision of saftey applications, e.g. airbag control systems is presented. The intention of the paper is to show how state of the art products use ML for safety critical applications. It is the goal to avoid the deployment of an airbag. We use a (Multiclass) Support Vector Machine to account for an improved classification. Various multiclass classification methods are rated and the two methods One-Versus-Rest and One-Versus-One are benchmarked in terms of quantities as test error, training time, memory consumption and misclassified crashes. All methods are applied to real measurement data of car crashes for the type of full frontal crashes in various conditions. We will show that One-Versus-One performs best. The method is able to classify car crash situations and improve the detection possibility. This allows for active and passive occupant safety components in the automotive area.**

***Keywords*—Machine Learning, Support Vector Machines, Multiclass SVM, Car Crash Detection**

SUMMARY

Active and passive occupanty saftey systems allow a dramatic drop of traffic fatalities. An intelligent system has to take various steps of the sensor information of a car into account and decide if an airbag is fired or not. By doing so, the injury rate may be significantly reduced and many lives might be saved.

In this paper, it is the goal to avoid the deployment of an airbag. For this we evaluated a Multiclass Support Vector Machine (MSVM). The training of the MSVM is done offline using labeled data. The implementation takes place as an additional feature within the ECU (Electronic Control Unit), which then is checked for plausibility with other sensor signal inputs for a final decision.

Furthermore, a strategy for the continuous sensor signals into discrete decisions has to be considered, to perform classification with the required time of a decision making to fire the airbag. In the case of a firing event, this has to be done at a specific point in time, such that the airbag can inflate right in time to protect the passengers of the car. For this, the decision for not firing has to be done until this time.

The challenge is to distinguish between such crash types as visualized in Figure 1 with the constraint of a decision after a certain time. Such a decision of the overall system for fire has to be made within a few milliseconds. If one compares now the sensor signals as shown in Figure 1, the acceleration signals are hard to distinguish. Even the integrated signal is challenging to separate. Furthermore, one has to take tolerance into account, e.g. life time drifts of the sensors.

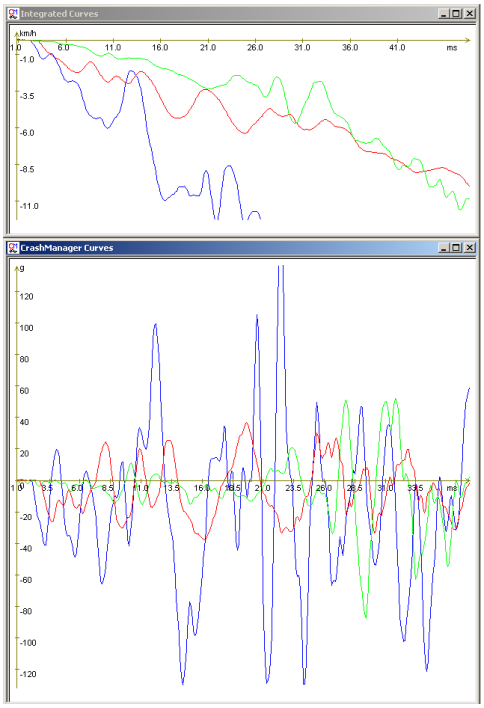


Fig. 1. Sensor signals (features [1], [2]) for the acceleration of AZT (green, no fire), FF56 (blue, fire) and ODB64 (red, fire) crashes.

We show, that it is possible to implement a MSVM with the One-Versus-One method into an ECU as additional feature to improve the classification for avoiding the airbag deployment and save costs. Furthermore, the amount of required Support Vectors is roughly half compared to the One-Versus-Rest method. This allows for realization into a micro controller system, considering memory and computation cycle time consumption.

REFERENCES

[1] I. Guyon, A. Elisseeff: *"'Feature Extraction, Foundations and Applications: Chapter "'An Introduction to Feature Extraction"'*, Springer Verlag, 2006
[2] C. Nello, J. S. Taylor: *"'An Introduction to Support Vector Machines and other kernel-based learning methods"'*, Cambridge Press, 2000

Structure and Software Elements of Enavi Radar for Large Drones

Grzegorz Jaromi
EUROTECH Sp. z o.o.
Mielec, ul. Strefowa 3
www.eurotech.com.pl
Email: g.jaromi@eurotech.com.pl

Dawid Sysak
Wrocław University of Science and Technology
Onboard Telecommunication Electronics for Spacecraft and Transportation Means Group
Wroclaw, W.Wyspiańskiego 27
Email: dawid.sysak@pwr.edu.pl

Paweł Kabacik
Wrocław University of Science and Technology
Onboard Telecommunication Electronics for Spacecraft and Transportation Means Group
Wroclaw, W.Wyspiańskiego 27
Email: paweł.kabacik@pwr.edu.pl

Ryszard Makowski
Wroclaw University of Science and Technology
Signal Processing Group
Wroclaw, W.Wyspianskiego 27
Email: ryszard.makowski@pwr.edu.pl

Extended Abstract

A growing number of flying devices such as drones, and the related increased probability of collisions, require equipping at least some of these devices with autonomous radars capable of signalling a possibility of a collision. It is of particular importance in the absence of optical visibility. Such radars must: (i) not interfere with other radars and telecommunication, (ii) be relatively inexpensive, (iii) be low in weight and (iv) be able to detect weak echoes cooccurring with strong reflections from large objects.

The construction developed by the Onboard Telecommunication Electronics for Spacecraft and Transportation Research Team of Wrocław University of Science and Technology is intended for Class 3 drones. In such drones, some hardware modules employed in motoring radars, with a range of a few hundred meters, can be used. In Class 3 drones, the radar range must enable its operator to correct the flight trajectory within 30 seconds. This implies that the range of such a radar must be longer than 1 km. Certainly, a longer range is desirable.

At the same time, it is a good assumption that such a radar should be able to detect, from a distance of at least 1km and with the probability of at least 90%, objects with the same RCS (Radar Cross-Section) as that of the object on which it has been installed. Moreover, detection of clutters from clouds and ground objects is also useful in this type of radars. The expected final result is also largely affected by an approach preferring the miniaturisation of the hardware component of the radar by using advanced digital systems such as FPGA, SoC or Integrated IF Transceiver 2x2 MIMO.

The paper presents the idea and the solutions for the construction of the above type of radar developed by the team. The principal hardware modules of the anti-collision Enavi radar are shown in Fig. 1

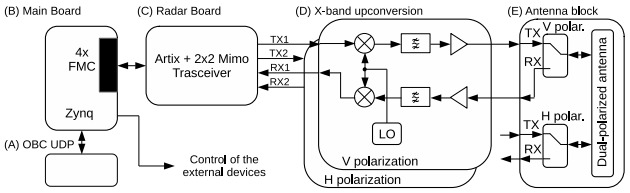


Fig. 1. The principal hardware modules of the Enavi radar.

Its vital element is software enabling flexible substitution of some elements of the solution depending on the changing environmental conditions. In order to choose the best-in-class solution, especially as regards the used probing signal, the algorithm of statistics determination on which echo detection will be based, and detection itself, a programming model of the radar has been prepared. It is meant to enable a quantitative assessment of radar performance. Based on measurements performed with the usable model of the radar, a number of real characteristics of the transmitter, telecommunication channel and the receiver can be included in the simulation software. A lot of characteristics of the Enavi radar are determined by the employed hardware. Nevertheless, there is significant flexibility when it comes to the emitted signals and the execution of the detection block.

The developed usable model of an anti-collision radar currently enables registering signals reflected from objects with the use of external recorders, and partially – detecting these objects. A considerable number of the obtained object detections are satisfactory. Although the conducted work is well advanced, it cannot be regarded as completed yet. Therefore the presented simulation results should be treated as an outline of possibilities rather than a description of the target properties of the radar.

Embedded Systems

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

A Microcontroller Based System for the Selected Gases Detection with Alert Feature

Marek Niewiński
Institute of Microelectronics and Optoelectronics
Faculty of Electronics and Information Technology
Warsaw University of Technology
Koszykowa 75, Warsaw, Poland
Email: marek.niewinski@pw.edu.pl

Wiktor Szczerek
Institute of Microelectronics and Optoelectronics
Faculty of Electronics and Information Technology
Warsaw University of Technology
Koszykowa 75, Warsaw, Poland

***Abstract*—The problem of measuring the concentration of gaseous chemical compounds in the air - especially these potentially dangerous to human life - is studied extensively. The main goal of this work was to design, build and test a cost-effective system that can measure the concentration of different gases and additionally notify the user when a specified threshold value is exceeded.**

***Keywords*—Gas sensors, Microcontrollers, GSM.**

I. Introduction

Any chemical, in either gas, liquid or solid form, has the potential to cause harm to humans. In this work we will focus on detecting potentially toxic gases that can be found in typical human living environments (e.g., homes, offices, factory spaces, and auto-mobiles).

Most gas monitoring systems permanently integrate sensor for specific gas.

In this work we present the concept of a portable gas detector which can use easily changeable gas sensor module.

The electrochemical sensors were chosen as basic measuring elements, because of their extremely low (almost zero) power consumption (flow of electric charges is the result of a chemical reaction inside the sensor).

II. System Design

The following assumptions were made during this work:

- the system will measure gas concentration, collect and analyse the obtained data and inform the user about exceeding the defined concentration level, if such a situation occurs,
- notification of exceeding the above-mentioned level should be transmitted quickly and over long distance; additionally, the system should inform about such an event directly, by means of light or sound,
- the system will be designed with low power consumption in mind, so that it can be powered by batteries or accumulators,
- the system will cooperate with sensors dedicated to different types of gases.

To fulfill all above requirements it was decided that the system will consist of two separate but cooperating units. The first, called base unit, measures and analyzes the signals sent by the sensor, transmits data inside and outside the system, has a power supply and a memory for a sufficient amount of configuration information to identify a given sensor. The second unit will contain a specific gas sensor and additional conditioning circuitry. This idea is illustrated in figure 1. Such a design makes it possible to use various gas sensors with the same measuring unit.

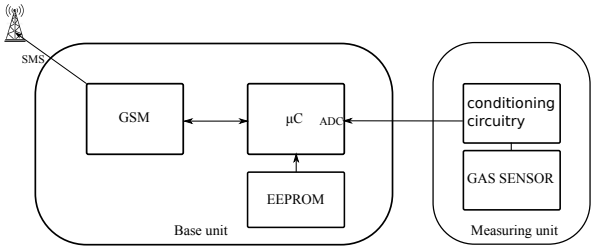


Fig. 1. Block diagram of the proposed portable gas detection system.

III. Tests and Measurements

To validate the correctness of a proposed solution two types of gas sensors where tested:

- Carbon monoxide
- Ethanol - C_2H_5OH

IV. Conclusion

The new concept of a microcontroller based system for monitoring gases was proposed, build and practically tested. It's main advantages:

1) portability due to low power consumption,
2) quick adaptation for work with electrochemical sensors for different gases.

The performed measurement tests for carbon monoxide and ethanol show sufficient accuracy, especially when the system is used as an alert device for notifying the user about exceeding the defined gas concentration level.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

A Study of Detection Probabilities and Real-World Testing of a Human Immunity Inspired Intrusion Detection System

Patryk Widulinski
Faculty of Electronics and Computer Science
Koszalin University of Technology
Koszalin, Poland
patryk.widulinski@tu.koszalin.pl

Krzysztof Wawryn
Faculty of Electronics and Computer Science
Koszalin University of Technology
Koszalin, Poland
wawryn@tu.koszalin.pl

I. Introduction

In this paper, a supplementation and further study of an intrusion detection system (IDS) proposed by us. The IDS monitors an area within the operating system to scan for modifications to the program files. It is based on the negative selection algorithm and it utilizes a random method and modified template methods to generate the receptors. In the paper, the anomaly detection probability impact of the addition of a second 16-bit "helper" receptor set is discussed. New experiments have been conducted to show the effectiveness of the system with regard to real infections, and have been analyzed.

II. The Proposed IDS

The intrusion detection system is a solution designed to detect modifications of files in the operating system. An illustration of the general construction of the IDS is shown in Fig. 1.

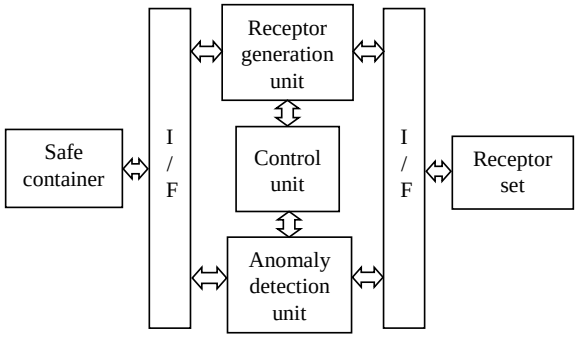


Fig. 1. A diagram of the IDS.

The IDS monitors a specific location in the operating system, as per the user's configuration, and scans the files contained within to check for possible intrusions in the form of program modifications. The control unit (CU) is responsible for directing the work of the two main system blocks: the receptor generation unit (RGU) and the anomaly detection unit (ADU). When the system is launched, the CU utilizes the RGU unit first. The RGU is responsible for generating the sets of receptors that the files will be checked against afterwards. After generating the receptor sets, the CU utilizes the ADU to scan the monitored files for anomalies.

III. Detection Probabilities

In the previous papers, we investigated the worse-case-scenario practical detection rates for the proposed IDS. The methods that have been used were the random generation method and variants of template-driven techniques. As a follow up to these experiments, a statistical approach is applied and the results are discussed.

IV. New Experimental Tests And Analysis

To supplement the previous research on the proposed IDS, new experimental tests have been conducted and analyzed. Whereas the previous work focused on clinical worst-case-scenario tests of the proposed system with anomaly sizes of 1 B to 12 B, this time real-world tests in a virtual machine have been carried out. The research includes testing the system's detection rate for 15 real malware samples.

V. Concluding Remarks

The detection probabilities and the detection rate for the experimental tests are concluded. Further work can be carried out to experiment with infections that are not 8-bit bound placement wise to observe how the system effectiveness would be affected.

Comparative Analysis of Methods and Tools for Formal Modelling and Verification for Embedded Systems. Probabilistic Approach

Marek Zbigniew Golonka
AGH Doctoral School
AGH University of Science and Technology
Krakow, Poland
E-mail: mgolonka@agh.edu.pl
ORCID:0000-0002-5961-1303

EXTENDED ABSTRACT

Analysis and design process of systems is time consuming and require to have knowledge about appropriate software tools. One option is to create additional tools to ease process of design, but in this case you are unlikely to get better results than using the existing ones. Relying on existing software tools usually burdens researcher to get accustomed to them. Additionally process of configurations can be problematic.

This paper is result of my research which is focused on approximation modeling and analysis of software correctness. Part of research include gathering informations about methods such as Markov Chain, Markov Process, stochastic Petri net, Probabilistic Timed Automata and software tools which allows to presents formal modelling for embedded systems examples.

Main goal of creating this paper was to explain basics of formal modelling and introduce existing software tools to ease process of analysis and design for such methods as Markov Chain, stochastic Petri Net and Propabilistic Timed Automata. Software tools presented in this article is not only limited to aforementioned methods and can be used also to their variations and extensions.

Researcher responsible for creating this paper observed few problems with gathered informations. One of the problem is that different scientist had different definitions of the same formal method of the timed automata but diagram scheme was the same. Another problems which occurs in articles of different scientist is that methods are not fully described in articles. Lack of good exemples can cause incomprehension of algorithms.

Section II of the article contains simple explanation of theory by showing examples of graphs or calculations. It explain in simple manner abou markov property, markov chain, stochastic petri nets, probabilistic automata (PA) and probabilistic timed automata. This section can be useful for student or scientist which want to learn basics regarding probabilistic formal methods.

Section III of the article contains short introductions and comparison of software tools which are considered useful from perspective of my research focused on formal modelling. During testing of software and gathering information, researcher responsible for this paper observe few things. One of them is importance of software version. For example GreatSPN in version 1.6 is multi platform and is also available on windows, but in version 3.0 it is limited to linux and MacOS only. Additionally researchers responsible for software development depending on software also attach scientific publication regarding theirs tools (Best examples are Prism and UPPAL web pages).

This article describe short introductions to probabilistic formal methods and software tools which are intended to help researchers during process of analysis and design of real time systems. Additionally article describe recent state of art of few example articles for formal modelling usage.

Comprehensive Information System for Management of Personalized Protective Thermally Active Clothing

Rafał Kotas, Marek Kamiński, Wojciech Tylman, Sebastian Woźniak, Michał Wojtera
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
rafal.kotas@p.lodz.pl

Anna Dąbrowska
Department of Personal Protective Equipment
Central Institute for Labour Protection—National Research Institute
Lodz, Poland
andab@ciop.lodz.pl

***Abstract*—The goal of this article is to present the IT platform that was designed and developed for control and monitoring of the thermally active clothing. It consists of several independent components: mobile application, web application, server with a database and data analyzer. First part of the article presents structure and functionalities of the components as well as the communication protocol. Following part of the article presents conducted experiments, preliminary conclusions and future challenges for system authors.**

***Keywords*—distributed control and monitoring system, thermally active clothing, thermal control**

I. Overview of the System

The work of mountain rescuers is very often performed in difficult conditions. The terrain and remote nature of rescues resulted in the development of many specific equipment. The basic element of equipment is clothing. Mountain rescuers currently are using passive, general-use hiking clothing. Taking into consideration the characteristic of rescue conditions (long hours of action at low temperatures and high humidity) it requires personalized and specialized thermally active protective clothing. The first idea that comes to everyone's mind is that the clothing should be heated so that it will improve the user's thermal comfort.

The authors of the article are conducting the research on "Personalized Protective Thermally Active clothiNg (sPParTAN)" financed by Polish National Centre for Research and Development. The system under development consists of: the electronic part (embedded microprocessor system, textile heaters, intelligent power supply circuit, additional photovoltaic power supply) – subject of a dedicated publication and comprehensive IT platform that allows for full control and monitoring of the intelligent clothing.

The aim of this article is to describe in detail the IT part of the project.

The core element of the platform is the database. It is used by two separate modules: data analyser and thermal model generator and backend application. The later serves as an entry point for Frontend application and Mobile application.

Mobile application controls the experiments and at the same time serves as a hub that gathers data from four data sources: Smartwatch, GPS sensor, Weather API and finally Embedded System with 5 types of sensors (under clothing temperature and humidity sensor, external temperature sensor, accelerometer, gyroscope, magnetometer, pressure sensor). Mobile application includes a module for automated control of the heaters in clothing. The module contains subsequent versions of the algorithm that is successively developed in the other component of the system (Data analyzer and thermal model generator).

The next element of the IT system is the web application. The functional description of the application includes the following elements: enabling stable collection of data, enabling validation and correction of transmitted data and making data available to authorized users;

II. Results

So far, about more than 600 laboratory experiments have been carried out. The longest experiment lasted 2 hours and the shortest one several dozen seconds.
Research objectives were limited to posing a few issues:

- assessment of the possibility of using selected sensors during typical physical activity in a Sppartan clothing;
- evaluation of the stability of temperature readings;
- evaluation of correlation of temperature readings between sensors;
- assessment of correlation between humidity reading and user comfort.

Initial system tests showed that all the planned functionalities were successfully implemented. The performed experiments are recorded on the mobile device, then transferred to the database and made available to the data analyzer and thermal model generator. Initial measurements showed, however, some disturbing trends that will become a field for active research in the future.

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Implementation of Coprocessor for Integer Multiple Precision Arithmetic on Zynq Ultrascale+ MPSoC

Tomasz P. Stefański
Faculty of Electronics, Telecommunications and Informatics
Gdansk University of Technology
Gdansk, Poland
tomasz.stefanski@pg.edu.pl

Kamil Rudnicki
Department of Reconfigurable Systems
Brightelligence Sp. z o.o.
Lodz, Poland
publications@brightelligence.com

Wojciech Żebrowski
Gdansk Office
Aldec Inc.
Gdansk, Poland
wojtekz@aldec.com

Extended Abstract

The scientific literature predicts the growth of importance of computations in precision higher than the standard 32/64 bits, i.e., in multiple-precision arithmetic (MPA). MPA can be considered as a way to tackle numerically difficult problems (refer to [1], [2]). Unfortunately, MPA requires large computing resources in terms of central processing unit (CPU) time and memory consumption. Hence, the development of parallel MPA accelerator is now crucial for the progress of this branch of scientific computing. This is the direct motivation for our research aimed at the development of coprocessor for integer MPA [2]. The coprocessor is developed using the very high speed integrated circuit hardware description language (VHDL) as an intellectual property (IP) core. Hence, one can implement it on field-programmable gate arrays (FPGAs) of various scales, e.g., on multi-processor system on chip (MPSoC) platforms combining CPU cores and FPGA within a single chip as well as on PCIe acceleration cards.

Despite the passage of time, none of the MPA processors presented in the literature gained popularity and worldwide success. Furthermore, none of solutions is freely available as an open-source IP core of a parallel coprocessor for MPA. Therefore, we have recently released the code of our integer MPA coprocessor [3], which is available to the public and licensed under the Mozilla Public License. To the best of the Authors' knowledge, this is the only recent integer MPA coprocessor which is both presented in the scientific literature and open sourced. In this contribution, we extend these results by presenting the implementation of our MPA coprocessor on Xilinx Zynq UltraScale+ (ZU7EV-FFVC1156) MPSoC. It includes quad-core ARM Cortex-A53 high-performance energy-efficient 64-bit application processor (based on ARM8-A architecture) and FPGA. In this paper, we focus on the acceleration of scientific computations of the discrete Green's function (DGF) in computational electromagnetics [1]. The choice of this benchmark stems from possible applications of DGF in electromagnetic simulations. Although such a function can facilitate electromagnetic simulations, it requires MPA for computations. Furthermore, DGF computations remain the current problem of computational electromagnetics. Therefore, the choice of DGF should enable benchmarking of the developed coprocessor in realistic and future-perspective computational scenarios for MPA.

In Fig. 1, measured runtimes are presented for the MPA coprocessor and the ARM Cortex-A53 core for DGF parameters $k = 0$ and $k = 99$ and its varying length n approaching 2000. To compute DGF for $n = 2000$ and $k = 0$ ($k = 99$), a single core of ARM Cortex-A53 processor needs 15,156 μs (14,949 μs) whereas the MPA coprocessor needs 3,403 μs (3,352 μs). For these parameters, the developed MPA coprocessor is around 4.5 times faster than a single core of ARM Cortex-A53 processor within the same MPSoC. Currently, for resources available on Zynq UltraScale+ MPSoC, the implementation of thirteen MPA cores is possible in this chip assuming 80% utilization of FPGA resources.

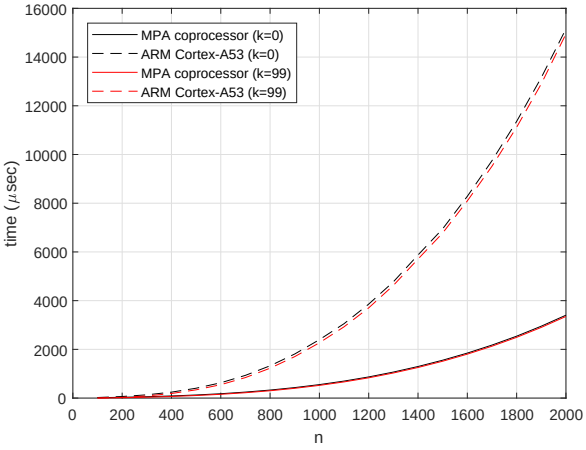


Figure 1. Runtimes for DGF computations. MPA coprocessor results overlap for $k = 0$ and $k = 99$.

References

[1] T. P. Stefański, "Electromagnetic problems requiring high-precision computations," *IEEE Antennas Propag. Mag.*, vol. 55, no. 2, pp. 344–353, 2013.

[2] K. Rudnicki, T. P. Stefański, and W. Żebrowski, "Open-source coprocessor for integer multiple precision arithmetic," *Electronics*, vol. 9, no. 7, p. 1141, 2020.

[3] K. Rudnicki, T. P. Stefański, and W. Żebrowski, "Integer-MPA-Coprocessor," https://github.com/stafan26/integer-MPA-coprocessor, 2020, [Online; accessed 19-May-2021].

Book of Abstracts of the 28th International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 24-26, 2021, Łódź, Poland

Logging Debug Data from IoT Embedded Devices over the GSM Network

Lubomir Bogdanov
Department of Electronics, Faculty of Electronic Engineering and Technologies
Technical University of Sofia
8 Kliment Ohridski blvd., 1000 Sofia, Bulgaria
lbogdanov@tu-sofia.bg

EXTENDED ABSTRACT

The paper discusses a specialized low-power embedded system that records any debug output over the UART interface of IoT devices. The acquired data is buffered locally and sent to a central server over the GSM network, at a predefined period of time. This logging device is battery powered and solar charging is applied to it. Certain parameters of the logger can be configured remotely.

Debugging an embedded system in a laboratory differs from debugging it in the field. Little or no helping devices exist for those purposes. That is why the author proposes a universal data logger for IoT embedded systems. Debugging output is transferred over the UART interface of the target microcontroller, then written to an SD card, and finally uploaded to a custom TCP/IP server at a fixed period of time. The logger is controlled through text commands sent over the GSM network with the help of short message service (SMS) or TCP/IP sockets. The required SIM card must provide an Internet connection with enough purchased packets to satisfy the target device logging requirements.

In theory the system should be thoroughly tested before deployed in the field. But practice has shown that some effects of the environment itself might lead to abnormal system behavior that wouldn't be noticed in the laboratory otherwise. Such effects include the decrease in battery voltage due to low temperatures, failure of components due to leaked enclosures, excessive power consumption due to weak network signal, delays in the data transmission due to overloaded network, or even network absence due to maintenance. All those events usually are witnessed in the field, after many hours of operation. A separate, independent device that logs the behavior of the target system would be of great help to the developer.

The logger sends its data with the TCP/IP protocol over the GSM network. To keep it universal and flexible, a lot of the parameters could be configured by the user, namely through three types of interfaces – UART, SMS (GSM) and TCP/IP (Internet). This makes the device triple-secured in the event of problems with the input/output, e.g. if the Internet of the SIM card has been used up (no more available packets have been purchased), the short message service could be used for commands, and vice versa. The worst case is that both of the above-mentioned methods are not available, then the user could visit the device in the field and upload all of the logs through the wired UART interface to a backup device. To make the device robust, two batteries and two solar panels have been included. This increases the overall device price but the idea behind it is that such loggers would be produced in small quantities and would be installed on some, but not all, target IoT systems.

The hardware of the logger is made so that it doesn't interfere with the main system's operation. This requires separate power supply and separate energy harvesting module. It has two solar panels and two batteries. Those components are paralleled together to increase the overall energy capacity of the logger. A single battery charger with hysteresis is provided for 18650-type battery. For GSM network connection an A9G module is used. The module is manufactured by the company Ai-Thinker and implements a 2G connection. The price of the module compensates for the double-redundancy of the power supply and makes the total cost of the logger acceptable. The charging voltage increases up to 4.2 V which is exactly the main rail requirement of the A9G module. For the UART input/output an on-board 3-volt regulator is used that supplies the pins' circuitry. This type of voltage is compatible with most of the modern microcontrollers in the IoT field and the user should not be worried about level-shifting circuitry. Direct connection is acceptable.

The A9G module contains a SoC with a 32-bit RISC processor capable of running up to 312 MHz, 4 kB of instruction and data caches, 4 MB SRAM, on-board radio, and external 4 MB Flash. The module uses an RTOS and the logger's firmware has three important tasks that carry out the main functionality – a timer, an SD card and a command task.

The GSM logger supports a set of commands that are accessible by the user from any of the three possible interfaces – UART, TCP/IP and SMS. By the writing of this paper the firmware revision is 1.8 and its respective command set comprises of 21 commands. Some of the commands have queries, i.e. the same syntax of the command, followed by a question mark. By receiving an SMS, the logger is synchronized with local time which is a part of the SMS format.

The Comparison of Native and Hybrid Mobile Applications for Android System

Aleksander Kaczmarczyk, Wojciech Zabierowski
Department of Microelectronics and Computer Science
Lodz University of Technology
Lodz, Poland
wojciech.zabierowski@p.lodz.pl

EXTENDED ABSTRACT

It is incredibly difficult to imagine current world without mobile devices. Quick growth of mobile networks and technologies had a significant impact on starting using mobile devices instead of personal computers by its users. Mobile applications started to be more and more popular. A big part of them is native and can be used only on given mobile systems such as Android or iOS. Due to this problem, the idea of hybrid applications started to be more appealing to publishers who wanted to distribute their application on many systems.

Android has become Google's one of the most important projects and the most popular mobile system. Many updates were published in over ten-year-old history of Android. Each of them offered some new features in many aspects – user interface, functionalities, security.

Native software is developed for a specific platform. In case of two most popular mobile systems, such applications are implemented using Java or Kotlin (Android) and Swift or Objective-C (iOS). The most important pros of native applications are: fast running, high efficiency, easier access to modules and sensors of mobile devices (e.g. camera and GPS), better usage of user interface elements, easy distribution in application stores.

Hybrid applications are a combination of native applications and web applications (those which can be run in an internet browser). They use an option of displaying websites in a WebView component. Hybrid applications can be run on many platforms, which eliminates necessity of implementing more than one version of an application.

Java 8 can be used to build mobile applications which can be run on Android 7.0 version or newer ones. New features in Java 8 are generally appreciated by programmers. Due to those changes, building applications in this language seems to be much easier. This update is considered as the most important in the history of Java.

Ionic is a web user interfaces framework and its applications are based on modular project structure. Ionic uses Apache Cordova, especially its plugins which may access mobile device modules and sensors such as camera, battery status, vibrations. Programmers can also use third-party plugins.

In order to compare native and hybrid applications for Android system, there was a mobile application created in two versions. The first one was implemented in Java 8 and the second one was built using Ionic framework. The main idea of the designed application was publishing and an overview of promotions observed in stationary and online stores.

In order to compare native and hybrid mobile applications for Android system there were conducted several tests concerning both implementation and efficiency of those applications.

Building process in case of a mobile application for Android systems describes compilation of source code and generating APK (Android Package Kit) file which is used to install an application on a mobile device. Building a native application on average was at least half as fast as building a hybrid application.

Speed of running is an extremely important factor in case of mobile applications. The hybrid application starting time was slower what might be an effect of loading a big number of scripts.

Additionally, time of application fragments transition was checked. Quick moving between tabs helps achieve an effect of smoothness. In both applications transitions were rapid. However, in case of the hybrid application they were slightly faster as a result of scripts being loaded already during application launch.

Moreover, the author of this article tested times of processing data loaded from REST API which is generally a key factor to build a responsive mobile applications. Times were counted from the moment of sending a request to the ending moment of loading full data in an emulator. Efficiency of native applications was clearly higher. In case of hybrid applications, the bigger data is, the much longer it is processed.

Usage of hardware resources was also tested. Both applications took low amount of disk space and RAM. In both cases the hybrid application was using it more than the native application.

Analysis of connection with mobile device modules was based on access to localization data. Both native and hybrid applications could read such data. In case of the second one the data was less precise but obtained more easily.

Comparison of native and hybrid mobile applications for Android system based on conducted tests indicates that the first ones have higher efficiency and the second ones should be easier to build and maintain. In terms of speed of running, both applications were really fast, however times of processing data from REST API responses show clear advantage of native applications. In many cases the hybrid application was not worse than the native application. The option of designing mobile applications with Ionic for many mobile systems should be considered by publishers despite slightly worse statistics. Companies which would like to have very efficient mobile applications ought to develop native applications for Android or iOS.

Index of Authors