Book of Abstracts of 29ᵗʰ International Conference
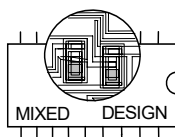
MIXED DESIGN

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

MIXDES 2022
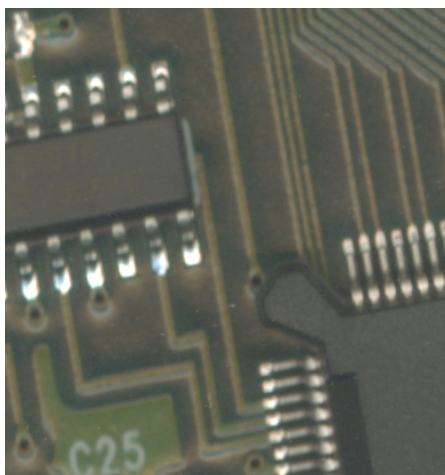
Wrocław, Poland
June 23 – 24, 2022

Edited by
Andrzej Napieralski

Preface

For 28 years the MIXDES Conference is a forum devoted to recent advances in micro- and nanoelectronics design methods, modelling, simulation, testing and manufacturing technology in diverse areas including embedded systems, MEMS, sensors, actuators, power devices and biomedical applications. This year the International Conference "Mixed Design of Integrated Circuits and Systems" celebrates its 29th edition. After coronavirus (COVID-19) pandemic restrictions we can meet again in Wrocław, the capital of Lower Silesia region.

The program of the conference consists of two days of sessions starting each day with invited talks. The following invited talks will be presented:

- *IC Masks - The Challenges of the Newest Technologies*
  Mariusz Niewczas (Design2Silicon Inc., USA)

- *Nanoelectronic Challenges and Opportunities for Cyberphysical Systems*
  Maria Helena Fino (Nova School of Science & Technology, Portugal)

- *Ultralow Power Stretchable TFT Electronics*
  Arokia Nathan (University of Cambridge, UK)

The program of MIXDES 2022 also includes 2 special sessions:

- *Compact Modeling of Heterogeneous Devices and Systems*
  organised by Dr. D. Tomaszewski (Łukasiewicz - Institute of Microelectronics and Photonics, Poland)
  and Dr. W. Grabiński (GMC, Switzerland)

- *Special Session in Memory of Professor Wojciech P. Maly*
  organised by Prof. W. Kuźmicz and Prof. A. Pfitzner (Warsaw University of Technology, Poland)

In addition to the technical sessions, the conference attendees will have an opportunity to participate in an IEEE Distinguished Lecturers' session organized by Łukasiewicz - Institute of Microelectronics and Photonics, Poland in collaboration with IEEE ED Poland Chapter.

Number of accepted papers and authors by country

Country	Number of		Country	Number of		Country	Number of	
	papers	co-authors		papers	co-authors		papers	co-authors
Austria	1	3	France	2	12	Singapore	0	1
Belgium	0	1	Germany	3	17	Slovakia	1	1
Brazil	1	6	Iran	0	1	Spain	0	3
Bulgaria	1	7	Italy	1	2	Sweden	1	5
China	1	3	Poland	27	67	Switzerland	2	4
Czech Republic	1	2	Portugal	3	2	UK	2	2
						USA	2	4
						Total	**49**	**143**

Number of Authors by Country
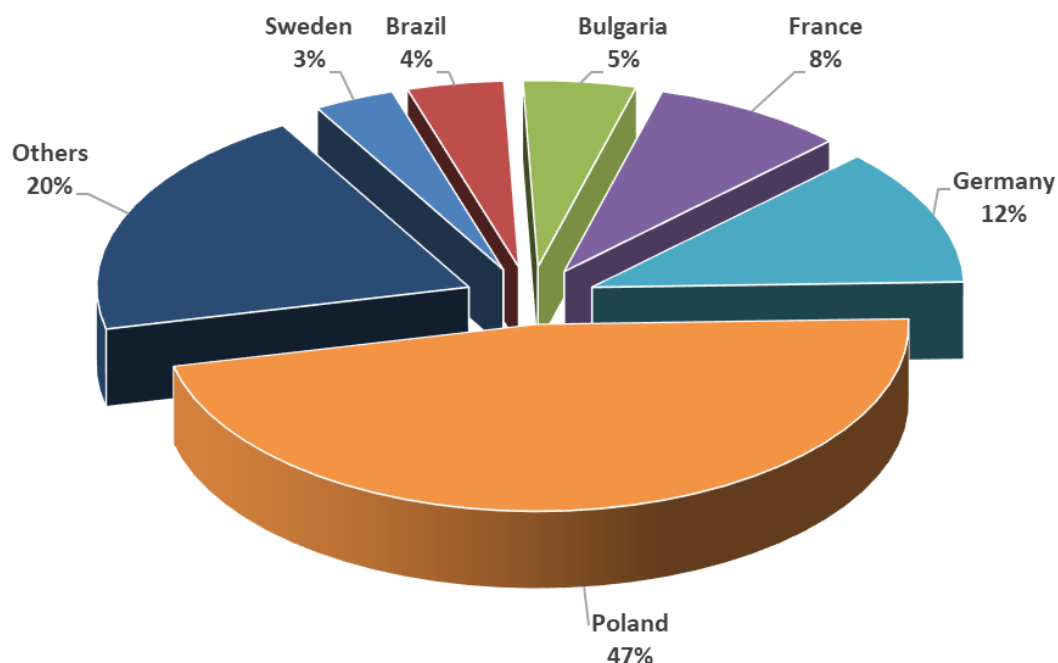
All regular papers were reviewed and selected from submissions from 19 countries. The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing contributed papers.

We hope that you are safe and healthy and remain so, and we will meet together next year in Kraków, (June 29 – July 1, 2023), the most beautiful city in Poland to celebrate the 30th edition of the conference.

Łódź, June 2022   *Andrzej NAPIERALSKI*
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                                               Lodz University of Technology, Poland
                                               General Chairman of MIXDES 2022

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General Invited Papers

IC Masks - The Challenges
of the Newest Technologies

Mariusz Niewczas

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Abstract—**We review major problems and technical challenges related to mask making A.D. 2022. This overview is addressed to engineers dealing with physical design of ICs. Two significant advances have been just introduced to the volume manufacturing in transition from 7nm to 5nm process nodes: EUV lithography and multibeam mask writing. Combined, they improve accuracy, process margin and wafer throughput. However, they introduce various challenges and opportunities that we discuss here. Moreover, on the software side, two critical issues are being addressed currently, the data volume explosion and tremendous computational requirement. These are being addressed with the move to new data formats, curvilinear geometry and new algorithms utilizing supercomputing on GPU clusters.**

Keywords—**EUV; MultiBeam writing; Mask Data Preparartion; OPC;**

I. Introduction

The mask technology for the 5nm node and below, has become more complex and expensive. This is because two significant advances were unavoidable. The introduction of the EUV lithography scanners allowed to create smaller shapes on wafer comparing with the 193i lithography. The arrival of Multi-Beam Mask Writers (MBM) allows to write more complex masks than the Variable Size Beam (VSB) machines.

First, we will describe the construction of the EUV mask and the principles of operation of EUV scanner and MBMW. Second, we will review various topics that the mask industry deals with today: modeling of mask and lithography processes, mask inspection and repair, data volume explosion. Third, we will zoom in onto what happens between the design tape-out and writing of the mask. The process is composed of two parts: Optical Proximity Correction (OPC) [4] and Mask Data Preparation (MDP). Fourth, we will discuss the coming transition to curvilinear masks [3]. Comparing with Manhattan or octagonal shapes, it can lead to smaller layouts, better performance, and superior process window.
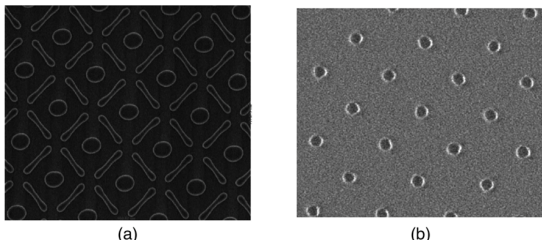
Fig. 1. (a) D2S ILT [2] curvilinear mask patterns written by the NuFlare multibeam mask writer MBM 1000 (b) the corresponding wafer prints (Source Micron)
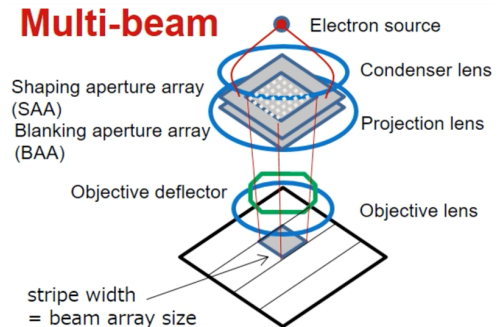
Fig. 2. The multibeam maks writer (Source: NuFlare)
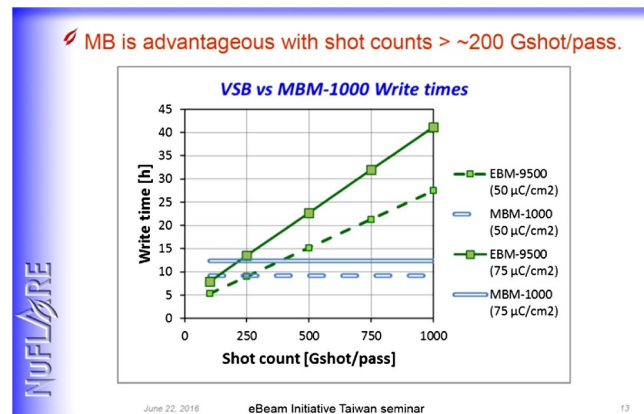
Fig. 3. Comparison of mask write time per mask shout count. For MBM-1000 the write time is theoreticvally constant so it is much fater for complex masks. (soure: NuFlafre)

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Nanoelectronic Challenges and Opportunities for Cyber-Physical Systems

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Abstract—**Over the last decades nanoelectronics have face an unprecedent evolution. Not only have the so-called conventional devices faced the development of new Mosfet device structures enabling the implementation of ever smaller device sizes operating at higher frequencies, but new unconventional devices have emerged as well. Also, the possibility of integrating intelligent nano sensors and actuators yields the possibility to modify our everyday life through cyber-physical systems. On the other hand, the application of these cyber-physical systems to a wide range of application domains, is also fueling the development of new devices with ever demanding specifications. This paper deals with the opportunities and challenges for nanoelectronics in their application in Cyber-physical systems**

Keywords—**Nanoelcetronics, compact modeling, prameter extraction, VerilogA, Cyber-Physical Systems**

I. INTRODUCTION

During the last decades the evolution of nanotechnologies has yielded the development of advanced components enabling the implementation of electronic equipment with increased capabilities, better performance, lower power consumption, and smaller form factors. Applications have moved from being stationary to becoming portable and wearable by people. More recently, the possibility for designing intelligent nano actuators/sensors that can be integrated in communicating objects, capable of generating, exchange, and consume data with minimum human intervention, has made possible the "Internet of Things." More recently the evolution of nano technology has made possible the birth of Cyber-Physical (CPs) systems involving other physical objects such as wearable devices, vehicles, homes, buildings, and even energy systems, in which continuous sensing and computing takes place[1].

The innovation and development of CPs relies on the input of many disciplines, and Nano Electronics is expected to be a key enabling technology (KET) to sustain the development of future smart sensing systems and/or Cyber-Physical Systems. In this paper the challenges for nanolectronics arising from the increased domains of application of CPs is addressed. Starting from an overview of nanoelectronics evolution, from

conventional MOSFET transistors, different MOSFET structures for CMOS devices till what is usually referred to as non-conventional Nano devices, the need for developing advanced modelling techniques at different abstraction levels is pointed out. For the different levels, challenges for the development of the models are identified. In particular, the automatic evaluation of model parameters given data resulting from measurement of devices characteristics, is analysed and a working example considering the automatic determination of TFT model parameters is illustrated[2]. The high accuracy of results obtained is demonstrated by comparing the output characteristics of a TFT with W/L=50/20 [μm] obtained with the model, against those obtained from measurements (in doted), as illustrated in Fig. 1. Finally, the specificity of using VerilogA in the development of device models to be integrated into electrical simulators is considered. The case for a nonconventional device, i.e. a memristor, model is presented, and results illustrating the transient simulation in spectre of the device in both soft and hard regimes are presented.
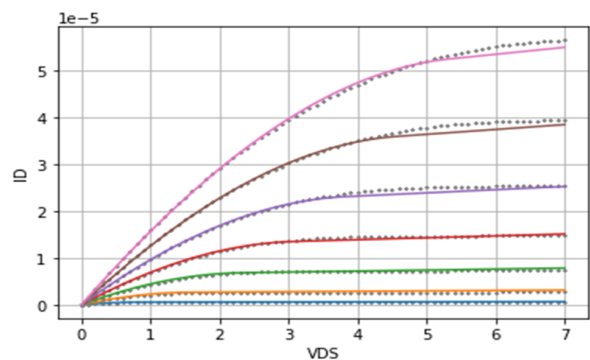
Fig. 1. TFT Output characteristics.

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Ultralow Power Stretchable TFT Electronics

Arokia Nathan[1], Chen Jiang[2], Jun Yu[3], Hanbin Ma[4]

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[2]Department of Electronic Engineering, Tsinghua University, Beijing, China
[3]School of Information Science and Engineering, Shandong University, Qingdao, China
[4]SIBET, Chinese Academy of Sciences, Suzhou, China

Abstract—**This paper reviews design considerations of flexible thin-film transistors and sensor interface circuits operating in the deep sub-threshold regime for ultralow power consumption. The devices and circuits are layered on fiber, and by using strip-helix-fiber coiling architecture, high extrinsic stretchability is achieved without causing electrical performance degradation.**

Keywords—**organic thin film transistor; stretchable electroncs; deep-subthreshold operation; ultralow power**

I. INTRODUCTION

Advances in low temperature, large area, and low cost process integration technologies hold great promise for thin film transistor (TFT) electronics for a new generation of applications beyond displays. In particular, there is growing interest for realisation of wearable devices that can monitor the physiological state of the human in real time, for continuous healthcare monitoring [1,2]. For TFT electronics to be deployed in wearable devices as sensor interfaces and signal processors, new circuit architectures for high stretchability and ultralow power operation are needed. Ultralow voltage/current operation is especially important so as to achieve a high resolution of the sensory signal. This talk will review current state-of-the-art in thin film electronics, and demonstrate examples of TFT operation for sensor interfacing, along with circuit-system architectures for high stretchability. The approaches considered are fully-compatible with display processes. A new concept for an integrated, highly stretchable system will be demonstrated based on a strip-helix-fiber coiling architecture.

II. DEVICE FABRICATION

The OTFT devices and circuits presented here were layered on strip fibre using an all-ink-jet-printing process. Using a FUJIFILM DIMATIX inkjet printer, silver ink was printed to form electrode contacts, polyvinyl cinnamate (PVC) cross-linked by UV for the dielectric, C_8-BTBT blended with polystrene for the semiconductor, and CYTOP as the encapsulation (Fig.1). The substrates used were trimmed polyethylene naphthalate (PEN) Teonex strips of 1mm width and 25μm thickness. To enable high extrinsic stretchability without compromising the TFT's electrical performance, a strip-helix-fiber coiling architecture was used (Fig.2), whereby the strip was wrapped around by a 875-μm-radius polyurethane (PU) core carrier-fiber. This provided strain compensation of the coiled helix by allowing change in the coiling angle. The inkjet-printed TFTs and circuits operate in deep-subthreshold providing the crucial benefit of ultralow power and high gain [3,4], with stretchability attributes that allow the circuits to be weaved or knitted into smart textiles/fabrics.

III. RESULTS AND DISCUSSION

The devices and circuits were characterization using the Keithley 4200 Semiconductor Parameter Analyzer. The characteristics shown in Fig.1 were measured with test OTFTs printed on a glass substrate. The devices yield a low threshold voltage and a steep sub-threshold slope by virtue of low interface state density at the semiconductor-dielectric interface. Stretchability tests were carried out with the strip helix OTFT coiled around a stretchable PU fiber at a helix angle of 59° to allow for precise control of the strain during electrical measurements. The transfer characteristics shown in Fig.2 are for a carrier-fiber strain varying from 0 to 50%, as well as after it was relaxed to its original state. No changes were observed in the electrical characteristics.
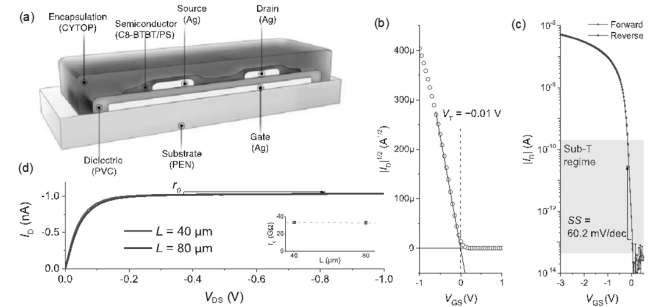
Fig. 1. Device cross-section of printed OTFT and its current-voltage and transfer characteristics on linear and log scales.
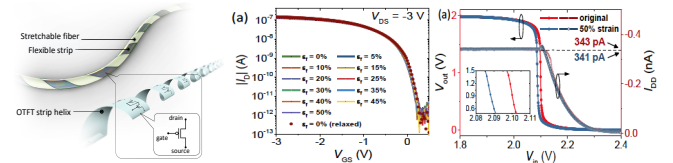
Fig. 2. Schematic illustrating the OTFT strip helix coiled around a stretchable fiber. Transfer characteristics of the strip-helix-fiber OTFT under different strains. Output voltage (V_{out}) and operating current (I_{DD}), under relaxed and 50% strain conditions.

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Special Session in Memory
of Professor Wojciech P. Maly

Professor Wojciech Paweł MAŁY

January 5, 1946 - December 20, 2021

an outstanding academic teacher
of Warsaw University of Technology
and Carnegie Mellon University in Pittsburgh,
a world-class scientist in the field of microelectronics

For almost half a century he was associated with the Institute of Microelectronics and Optoelectronics (IMiO) at Warsaw University of Technology, and simultaneously for about 35 years with Carnegie Mellon University in Pittsburgh, where he worked at the Department of Electrical and Computer Engineering as the Whitaker Chair Professor, and as co-director of the SEMATECH Center of Excellence CMU.

Professor Mały was a pioneer in the field of design for manufacturability. He created the concept of statistical simulation of microelectronic manufacturing processes, many new ideas for design and test of circuits, in conjunction with the analysis of economics of integrated systems production. His best-known works concerned the disturbances of manufacturing processes in microelectronics: the influence of random disturbances of process parameters, dependence of production yield on defects, yield optimization, testing of systems in terms of the observability of defects. His work, however, covered a much wider area. He dealt with, among others, automation of integrated circuit layout design, foresaw the development paths of microelectronics towards large-scale systems (wafer scale integration), 2.5D and 3D systems. For several years he had been working on the innovative technology of VESTIC integrated circuits (Vertical-Slit Transistor based Integrated Circuits), he was the author of.

Publication achievements of Prof. Mały are impressive: ground-breaking articles in the most prestigious magazines, invited plenary papers at the most important conferences, as well as patents and books. His outstanding achievements were recognized by invitations to program and steering committees of many top-level symposia and conferences and invitations to editorial committees of IEEE and other journals.

Prof. Mały was honored with many awards and prizes. He received awards of the Rector of the Warsaw University of Technology and the award of the Ministry of Higher Education for research achievements, the Technical Excellence Award granted by Semiconductor Research Corporation. He received a Fellowship from the Deutsche Forschungsgemeinschaft and was also elected an IEEE Fellow and a member of the IEEE Awards Board Committee, IEEE Circuit and System Society Representative in IEEE Solid State Council, IEEE Circuit and System Society VLSI Committee.

Prof. Mały, as internationally recognized expert, was appointed as an advisor and consultant to a number of leading research laboratories, both at universities and leading microelectronic companies. In particular, he cooperated with the Technical University of Munich, Technical University of Eindhoven, Fraunhofer Gesellschaft, Siemens Corporate Research and Development, VLSI Research Lab. National Semiconductor, NPCP Warsaw, Fairchild Research Lab. He was an advisor to Philips Semiconductor R&D in Nijmegen, consultant for National Semiconductor, Knights Technology, Inc. (Palo Alto CA). He was the member of the Advisory Board of Advantest Inc., Cadence Design System and chaired the Advisory Board of PDF Solutions, Inc.

Prof. Mały was an outstanding academic teacher, tutor of several generations of electronics engineers and scientific staff. His lectures, projects and care for graduate and doctoral students were recognized by numerous awards, such as the prestigious Aristotle Award from Semiconductor Research Corporation in recognition of pioneering teaching methods and ground-breaking research in the semiconductor industry.

In the opinion of students and colleagues, the contribution of Professor Wojciech Mały to the development of semiconductor technology and the impact he had as a teacher and mentor of many people in the microelectronics community cannot be overestimated. His vision and ideas are part of the essence of this field today.

With deep sorrow we said goodbye to the Great Scientist and to a Friend of many of us. This session is dedicated to his memory.

Estimating and Improving IC Manufacturing Yield
Past, Present and Future

Wieslaw Kuzmicz

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Abstract—**IC manufacturing yield has been the crucial technical and economical issue since the beginning of the microelectronic industry. This presentation gives an overview of the methods and tools helping to estimate and improve yield, including current challenging problems.**

Keywords—**manufactiring yield; process variability; spot defects; statistica process simulation; critical area**

I. INTRODUCTION

In the first years of IC manufacturing "trial and error" was the only design methodology, supported by an early version of Spice, the only available EDA tool. Although many ICs have been successfully fabricated, yield was unpredictable, and it was unclear what to do to improve it. Two main "yield killers" are: variability of the components' parameters (leading to unacceptable spread of circuit parameters) and spot defects (causing shorts and opens and resulting in nonfunctional circuits). Methodologies and EDA tools intended to understand and mitigate them appeared [1-4]. Research in the area later named "Design for Manufacturability" started and later was combined with economic considerations [6]. With rapid increase of complexity of manufacturing technologies and size of VLSI circuits early versions of EDA tools soon became obsolete or even unusable. New methodologies and tools were needed. This presentation shows the evolution of these methodologies and tools starting from the era of "10 mm feature size" ICs up to sub-10 nanometer VLSI circuits.

II. VARIABILITY

Well known and still routinely used methodology to estimate variability effects on IC performance and yield are: circuit simulation at process corners and statistical Monte Carlo circuit simulation. Simulation at process corners often overestimates variability effects and leads to overdesign. Monte Carlo simulation gives more realistic results if local and global variations are correctly accounted for. However, link to manufacturing process is missing. The statistical data needed to carry out such simulations come from experiment. The idea of statistical Monte Carlo simulation of manufacturing process [1] was introduced in 1982 and later extended and improved by adding link to layout. Unfortunately, it turned out that this kind of EDA tools is impractical for two reasons: (1) state-of-the-art processes are too complex to allow realistic statistical simulation in reasonable time, and (2) process settings are treated as strictly confidential, not available to circuit designers. TCAD tools for numerical process simulation do exits, but they are used for process development, and are not applicable to circuit design.

This paper is dedicated to the memory of Professor Wojciech Mały.

III. SPOT DEFECTS

A key link between circuit layout and density of spot defects is the concept of critical area [2,3]. It allows to estimate yield limited by spot defects. It can also be used to find layout areas that can be improved to reduce sensitivity to spot defects, and to determine some of the DRC rules. Critical area-inspired considerations were also used to propose methods of generating better test sequences for digital circuits [5,7]. However, critical area estimations for large layouts with millions of transistors is computationally expensive. Moreover, critical area concept is less applicable to deep submicron and nanometer ICs, which require OPC, multiple patterning etc. to avoid unacceptable layout distortions.

IV. CURRENT CHALLENGES

New device structures (FDSOI, FinFET, GAA) and EUV lithography make yield estimation even more difficult. Many more physical factors increase variability and affect yield. New EDA tools, such as e.g. photolithography simulators, improve yield by reducing process-related variability, reducing of distortion of layout shapes etc. These tools are for manufacturers, not for circuit designers. The "good old" simple methodologies (simulation at process corners, Monte Carlo simulation) are still in use. Post-layout circuit extraction and Monte Carlo simulation can provide fairly realistic picture of variability of circuit parameters and help to reduce it.

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VESTIC: A New IC Manufacturing Paradigm

Present Status and Future Plans

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Abstract—**The VESTIC (Vertical-Slit Transistor based Integrated Circuit) technology is an innovative way to implement very large-scale nanoelectronic integrated systems. The simulation and experimental feasibility studies performed so far indicate that this novel paradigm is an extremely attractive alternative to the existing most advanced technologies based on the structure of the MOS transistor**

Keywords — **VESTIC, Vertical-Slit Transistor based Integrated Circuit, VeSFET, Vertical-Slit Field-Effect Transistor, junction-less transistor, twin-gate transistor, regular layout, dynamic reconfiguration**

SUMMARY

The key concept of VESTIC, proposed by W. Mały [1, 2, 3], is the original, three-dimensional architecture of active elements, ensuring full regularity of the circuit topography and defining the structure of transistors by simple shapes based on circles (Fig. 1). The electrical contacts are vertical, evenly spaced columns that constitute the canvas of the system and, at the same time, the passages through the silicon layer (via) between the upper and lower layers of electrical connections, thus enabling vertical communication for electrical signals and creating an efficient heat distribution network.
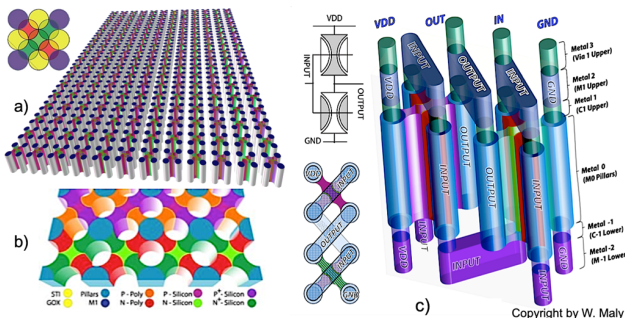
Fig. 1. VESTIC architecture: a) standard and b) densiest matrix of elements, c) inverter - electrical connections above and below the silicon layer.

The VESTIC technology has the potential to achieve ultra large scale of system integration with reduced implementation and production costs of new products due to: regularity of the system topography, reduction of the area occupied by individual transistors (scaling even beyond 7-nm node [8]), improved heat dissipation, full 3D integration possible and integration of various types of transistors (both field and bipolar) while maintaining the layout regularity.

This article is dedicated to the memory of Professor Wojciech Mały.

Further benefits arise from the use of the new junction-less transistor: VeSFET (Vertical-Slit Field-Effect Transistor) as a base component (Fig. 2).
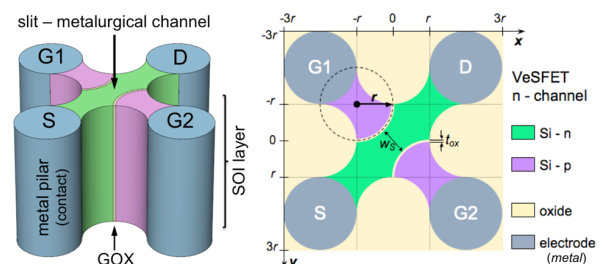
Fig. 2. VeSFET structure: 3D geometry and top view.

The attractive electrical properties of VeSFETs (such as very slight leakage currents, excellent ratio of the on-to-off current, almost perfect subthreshold characteristic) predicted on the basis of physical analyses [2, 4], were confirmed by measurements of test structures performed at IMO A*STAR Singapore [3, 6], EPFL Lausanne [5] and ITE Warsaw [7].

The VeSFET has two electrically symmetrical independently biased gates, which enables the effective control of its properties, a dynamic reconfiguration of the system functionality [9] and designing logic gates with a reduced number of elements. Moreover, a simpler structure and a different principle of operation make it possible to further reduce of production costs of circuits composed of VeSFETs in comparison with modern CMOS technologies.

Future plans for feasibility studies and production of innovative systems in VESTIC technology for various applications will mainly focus on low-power and reconfigurable circuits as well as sensors and non-volatile memories using 3D integration.

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Compact Modeling of Heterogeneous Devices and Systems

Advances in Qucs-S Schematic Capture for SPICE and Verilog-A Device Modelling and Circuit Simulation

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EXTENDED ABSTRACT

This paper introduces a schematic capture technique for generating and extracting two or more hardware description language (HDL) netlists or code modules from a single circuit diagram or device model drawing. Conventional schematic capture acts as a circuit simulator front-end for drawing circuit or device model diagrams on a high resolution computer graphics workstation. Output is normally a text file listing component types, values, and connections plus commands to control the circuit simulation process. The de facto industrial netlist format for circuit simulation is based on Berkeley SPICE. The current generation of FOSS (Free Open Source Software) circuit simulators, either derived from SPICE, for example Ngspice [1], or developed separately, for example Xyce [2], have adopted the de facto SPICE netlist format with additional simulation commands and device models. Due to the growing complexity of semiconductor compact device models there has in recent years been a move from compact model coding in C or C++ to Verilog-A HDL [3]. In parallel to semiconductor device modeling with Verilog-A the long established techniques of model construction using behavioural modeling or macromodeling [4] are still popular and significant. The nature of SPICE behavioural modeling allows device models and circuits to be constructed in stages and tested using simulation "on-the-fly". However, on successful completion and testing of a model the translation of its netlist to a Verilog-A module code has normally to be done manually. This can be both complex and error prone. The simulation front-end technique reported here introduces a new approach to schematic capture where one, or more, HDL are combined with behavioural SPICE modeling. This paper outlines the details of a new schematic capture process that has been implemented with the Qucs-S/Xyce simulator [5]. To demonstrate the application of the advances in schematic capture, particularly in compact device modeling, the construction of a GaAs MESFET TriQuint Own Model (TOM3) [6] [7] is presented. Fig.1 illustrates a typical TOM3 S-parameter two port test bench and simulation data.
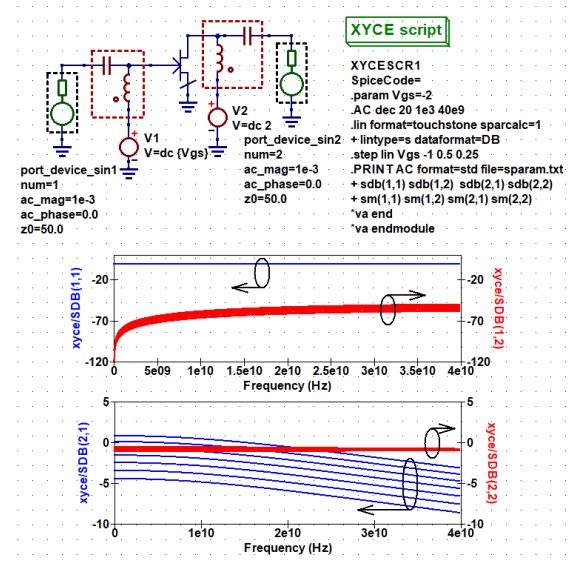
Fig. 1. N-channel TOM3 MESFET S-parameter two port test bench and simulation plots: SdB(1,1), SdB(1,2), SdB(2,1) and SdB(2,2) against frequency.

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Compact Modeling of Channel-Resistance Effects in Reconfigurable Field-Effect Transistors

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EXTENDED ABSTRACT

In [1] we introduced a compact model that is applicable on reconfigurable field-effect transistor (RFET) and calculates the injection currents over the Schottky barriers of these devices. Unlike standard metal oxide semiconductor field-effect transistors (MOSFETs), the RFET has two independently controllable gates [2]. The control gate (CG) is used to control the current flow through the device as in regular MOSFET application, while the program gate (PG) is used to determine the device's polarity [2]. A cross section of an RFET is shown in Fig. 1. For devices with long channel lengths (up to a few micrometers) or with longer gate-to-gate distances (L_{ung}) the current blocking mechanism of its channel (demonstrated as R_{ch} in Fig. 1b) becomes more dominant compared to the Schottky barrier injection of the source and drain side (demonstrated as $R_{\mathrm{SB,s}}$ and $R_{\mathrm{SB,d}}$ in Fig. 1b), leading to deviations in the injection model from [1] for some bias conditions (demonstrated in Fig. 2 as brown dotted lines).

In this work we present a closed-form and physics-based compact model that combines the injection-based current calculation from [1] with a MOSFET model that represents the channel resistance (R_{ch} of Fig. 1b) of such devices, in order to obtain the total device current. The results are demonstrated in Fig. 2 as solid red lines compared to measurements from [3] (green markers). It shows a good agreement between model and measurements and demonstrates the functionality of the model addition presented in this work.

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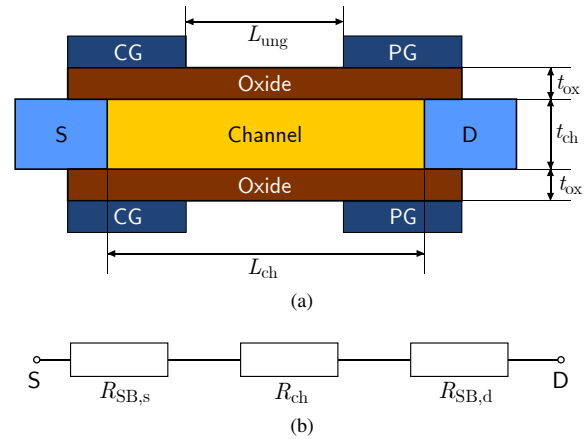
Fig. 1. (a) Schematic cross-section of an RFET showing the relevant geometric parameters for the compact model. (b) Simplified equivalent circuit, showing the resistances of the source and drain side Schottky barriers, as well as the resistance of the (ungated) channel, that carriers have to pass.
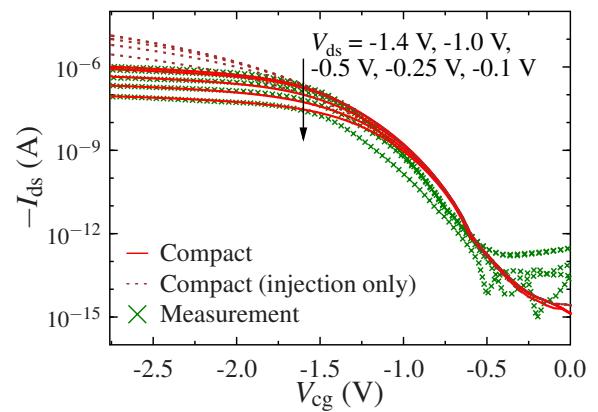
Fig. 2. P-type transfer characteristics calculated from the compact model (red) compared to measurements from [3] (green) and to the injection-based compact model model results of [1] (brown dotted lines). During the transfer characteristics measurement the PG was fixed to $V_{\mathrm{pg}} = -2.8\,\mathrm{V}$. The device has a channel length of $L_{\mathrm{ch}} \approx 2.1\,\mu\mathrm{m}$ and a gate-to-gate distance of $L_{\mathrm{ung}} \approx 0.7\,\mu\mathrm{m}$.

Comprehensive Design-oriented FDSOI EKV Model

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Abstract—**The work presents the comprehensive design-oriented EKV model for FDSOI technologies, including the back-gate effects. Despite its simplicity, the model correctly captures not only the dependency of the threshold voltage versus the back-gate, but also the changes in the slope factor and mobility. This results in a normalized transconductance efficiency that becomes independent of the back-gate voltage over a wide range. The model is validated thanks to the use of the Python-based automated parameter extraction tool on the advanced FDSOI technology.**

Keywords—**FDSOI, G_m/I_D, back-gate effect, inversion coefficient, low power, analog design**

Extended Abstract

To continue the scalability of the CMOS technologies, the Fully-Depleted Silicon-On-Insulator (FDSOI) technologies overcome the short-channel effect mainly thanks to its ultra-thin body. The latter, with the buried thin oxide layer, makes the FDSOI transistor an efficient four-terminal device. The so-called back-gate voltage (V_{back}) allows additional freedom to the device performance. In the static mode, the threshold voltage has the significant back-gate dependency [1], and subthreshold swing and mobility [1] are slightly influenced by V_{back} due to the gates coupling and front- and back-channel formation. However, the comprehensive transconductance efficiency (G_m/I_D) considering the velocity saturation and back-gate effects has not been discussed yet [2]. Therefore, the work shows the simplified EKV model adopted on a $22\,\mathrm{nm}$ FDSOI technology [3]. By using the open-source Python-based parameter extraction tool [4], the model presents the consistency of the normalized G_m/I_D over a wide V_B range.

The charge-based transfer characteristic I_D-V_G in saturation is given by [5]

$$\frac{V_G - V_{T0} - nV_S}{nU_T} = 2q_s + \ln q_s \tag{1a}$$

$$q_s = \frac{\sqrt{4IC + (1 + \lambda_c IC)^2} - 1}{2} \tag{1b}$$

with long-channel threshold voltage V_{T0}, source voltage V_S, thermal voltage U_T, slope factor n, inversion coefficient $IC = I_D/I_{spec}$, specific current $I_{spec} = I_{spec\square}W/L$ and velocity saturation parameter λ_c. Thanks to the log-linear inversion charge relation [6], the device bias point can be optimized within the range from weak to strong inversion. Fig. 1a shows a nice agreement between the model from (1) and transfer characteristics for a short nMOS FDSOI at different V_B. It should be noted that the parameters for the sEKV model are extracted independently from the different I_D-V_G at given V_B. The significant change in the threshold voltage is well
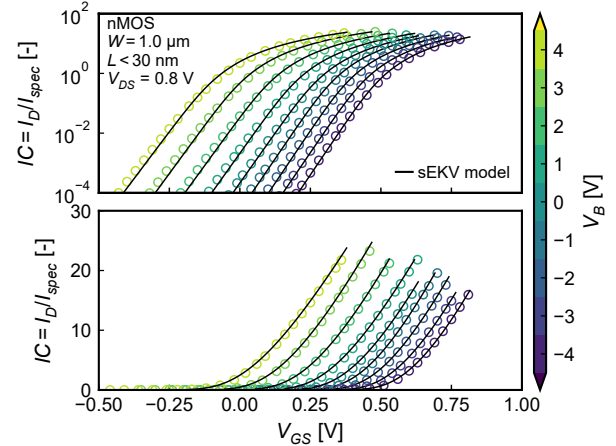
(a) Transfer characteristics with various V_B.
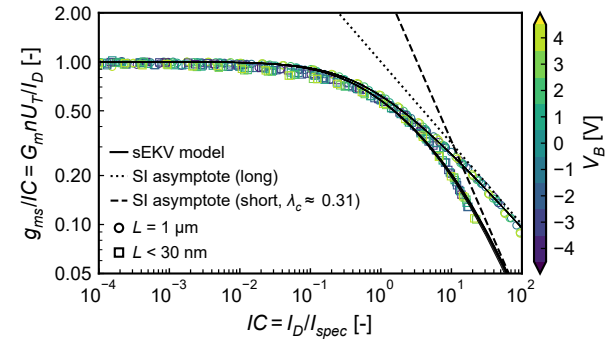
(b) Transconductance efficiency with various V_B for long and short devices.

Fig. 1. Simplified EKV model on the devices in saturation ($V_{DS} = 0.8\,\mathrm{V}$) by a $22\,\mathrm{nm}$ FDSOI process [3].

characterized by the extraction tool. Besides, the back-gate-dependent subthreshold swing and mobility are accounted by the n and I_{spec}. Consequently, as shown in Fig. 1b, the normalized transconductance efficiency ($g_{ms}/IC = G_m nU_T/I_D$) versus IC are consistent over the V_B from -4 to $4\,\mathrm{V}$ for long and short devices, respectively. Despite the simplicity of the sEKV model, the g_{ms}/IC versus IC normalizes the back-gate effects and provides a reliable G_m/I_D design methodology.

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Impact of Mechanical Bending on the Performance of Organic Thin-Film Transistors and the Characteristic Temperature of the Density of States

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EXTENDED ABSTRACT

The electrical performance of organic TFTs fabricated on flexible substrates can degrade under mechanical stress that may arise from bending, twisting or stretching of the substrate. In the current paper, the effect of bending (Fig. 1) on the electrical characteristics of organic thin-film transistors is studied, using experimental data obtained from a large number of discrete organic transistors fabricated on a flexible polymeric substrates, in the coplanar device architecture. By adapting a physics-based compact model [1]–[4] to the measurement results, conclusions regarding the impact of bending on the device physics are drawn.

The transistors under bending-stress presented a significant drain-current degradation that can be mainly attributed to the respected reduction of the effective carrier mobility value. By correlating a power-law mobility model and the basics of percolation theory, the observed mobility degradation could be attributed to a decrease of the characteristic temperature that describes the shape of the Gaussian density of states in the utilized organic semiconductor (Fig. 2).

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(a)

(b)
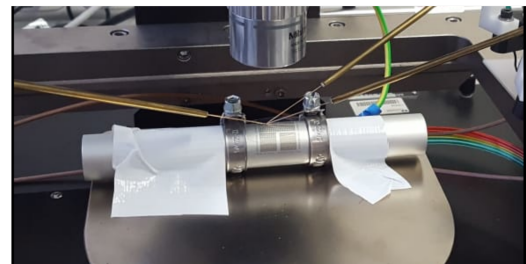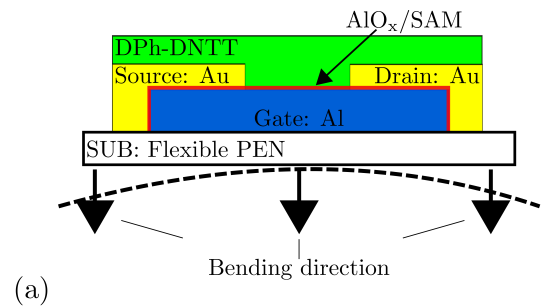
Figure 1. (a) Schematic cross-section of organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) device architecture on a flexible polymeric substrate. Mechanical bending is performed in the direction perpendicular to the path of the electric current in the transistor channel. (b) Photograph of the bending experiment. The substrate is attached to the outside of a cylindrical tube with a diameter of $20\,\mathrm{mm}$.
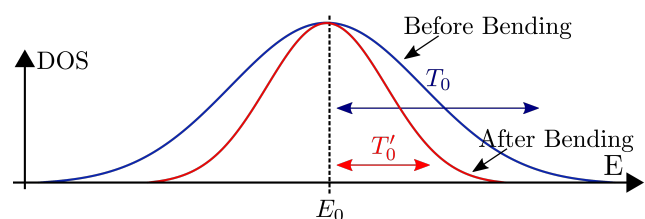
Figure 2. Narrowing of the tails of the Gaussian DOS due to the bending of the flexible substrate. The characteristic temperature T_0 (prior to bending) is decreased to T_0' upon bending.

Multidomain Modeling for Reliability Evaluation of Devices and Microsystems Using Verilog-A

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EXTENDED ABSTRACT

With the continuous increase in integration density induced by technology scaling and chip stacking, the dissipated power density has reached a critical level and thermal issues are now a major concern. Currently, evaluating the thermal behavior of a chip is generally done either thanks to finite element method (FEM) software coupled to a SPICE simulator or thanks to a strongly coupled electrothermal simulation in FEM software. However, these approaches are complex, time consuming and sometimes even not feasible. In addition, coupling circuit simulation and thermal FEM simulation is generally a complex task. Thereby, the need for a user-friendly tool designed to evaluate the temperature distribution inside an integrated system through standard circuit simulation arises. Analog hardware description languages such as Verilog-A offer the opportunity to manipulate thermal quantities thus allowing to perform electrothermal simulation of devices and systems in a standard microelectronics CAD environment. Taking advantage of the capabilities of these hardware description languages, a general methodology consisting in layout driven meshing and thermal modeling of the chip associated to electrothermal compact modeling of devices has been developed at ICube laboratory (Fig.1). This approach allowed us to develop a tool able to generate an electrothermal netlist of an integrated circuit suitable to SPICE-like simulators [1]. This tool which is fully integrated in the Cadence environment enables the SPICE electrothermal simulation of integrated circuits. To address large system simulations, a high-level
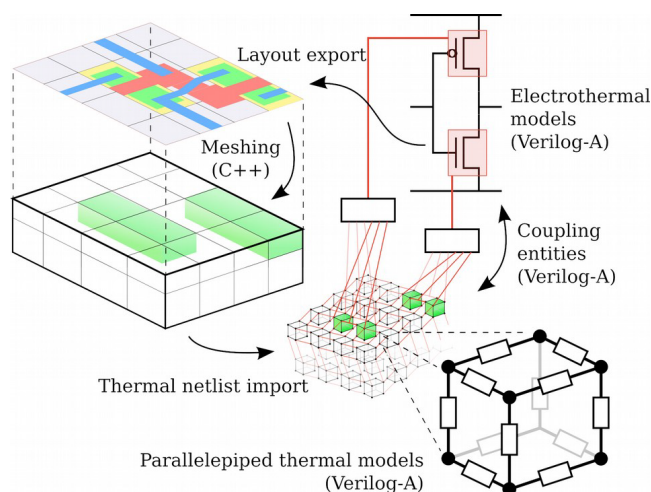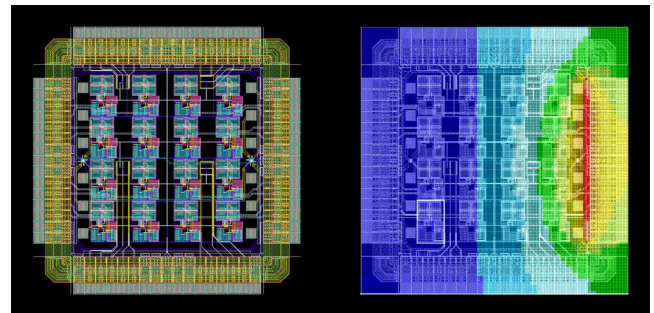
Fig. 2. Full chip electrothermal simulation. The original layout is shown on the left while the temperature map superimposed to the same layout is shown on the right.

electrothermal modeling method has been developed [2]. It consists in simulating the functional blocks (amplifier, ADC, filter, …) subjected to specific thermal gradients in order to determine how average temperature and temperature gradients affect their behavior. From the obtained data, one can develop accurate behavioral models of the functional blocks of a large integrated system, allowing to perform fast full-chip electrothermal simulations (Fig.2). Recently, our tool has been adapted to power electronics industry for discrete device simulation [3]. Finally, the possibility of implementing other physical effects has been demonstrated. In particular, the thermal induced mechanical stress has been successfully simulated. This approach leads to a powerful and versatile tool able to address reliability issues such as overheating, hot spot detection, thermal drift of the performances or even thermal induced delamination [4].

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Fig. 1. Layout driven electrothermal netlist construction

Optimization-based Determination of TFT contact Resistances in Python

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Abstract—The paper presents an optimization-based methodology for the determination of thin-film transistors contact resistances. The implementation of the proposed methodology in Python is presented. The validity of results obtained against devices characteristics is demonstrated. The advantage and limitations of the proposed methodology is also discussed.

Keywords—TFTs, compact model, contact resistances

I. INTRODUCTION

Due to the wide spread use of thin-film transistors (TFT) in a wide range of applications e.g., displays, radio-frequency identification tags (RIFID), or flexible electronics [1] a strong effort has been paid to the development of TFT compact models, [2]. In [3] a model-oriented methodology for the determination of TFT parameters and its automatic implementation in Python is presented. This paper considers an extension of this previous methodology, where the TFT contact resistances are also evaluated.

II. THIN FILM TRANSISTOR MODEL

Although the transport characteristics of TFTs are very different for the different active materials, the current-voltage characteristic of these was initially evaluated using the Mosfets Schokley model. In [4] a more accurate expression is proposed for TFT in saturation, and is given by:

$$I_D = \frac{W}{L_{eff}} \cdot \frac{\mu_0}{V_{AA}{}^\gamma} C_{ox} \alpha_s \left(V_{gs} - V_t\right)^{2+\gamma}, \tag{1}$$

where μ_0 is the carrier mobility at low bias, γ is the mobility enhancement factor, V_{AA} is a fitting parameter and α_s is also a fitting parameter that relates the saturation voltage overdrive. Should the contact resistances be considered, then the analytical expression for the drain current should reflect its dependence on the intrinsic voltages between the gate and source, V_{gs} and between the drain and the source, V_{ds}. These intrinsic voltages may be obtained with

$$V_{gs} = V_{GS} - I_D \cdot R_s \tag{3.a}$$

$$V_{ds} = V_{DS} - I_D \cdot (R_D + R_S) \tag{3.b}$$

where V_{GS} and V_{DS} are the externally applied voltages between gate and source and between drain and source respectively. By combining 3.a) with (1) an implicit function for the drain current evaluation is obtained

$$I_D = K(V_{GS} - I_D R_S - V_t)^m, \tag{4}$$

In this paper, two methodologies for the automatic evaluation of TFT parameters are implemented in Python and results obtained are compared. In the first case the methodology proposed in [3] is applied for the determination of the TFT parameters, where the contact resistances are neglected. Then, the solution obtained is considered as an initial point for the automatic determination of the gate resistance. In the second case the methodology proposed in [4] is implemented.

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Design of Integrated Circuits and Microsystems

8-bit Low-Power, Low-Area SAR ADC for Biomedical Multichannel Integrated Recording System in CMOS 40nm

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Abstract—**This paper presents the design and postlayout simulation results of 8-bit analog-to-digital converter (ADC) dedicated to multichannel biomedical integrated recording system. The integrated circuit is implemented in CMOS 40 nm process and has been recently received from fabrication. The proposed ADC is based on charge redistribution technique utilizing only two capacitors. The designed ADC converts analog signals provided from eight chopper based amplifiers, achieves sampling rate up to $1MS/s$ and occupies only $0.0033mm^2$ of silicon area. The peak DNL and INL are -0.6 and -1.4 LSB respectively. This paper presents particular blocks' detailed analysis as well as their postlayout simulation results.**

Keywords—**SAR ADC, analog-to-digital, low-power, low-area, charge redistribution, successive approximation register**

Extended Abstract

In this paper the ADC based on Successive Approximation is presented. It is dedicated to multichannel integrated recording system, implemented in CMOS 40nm, therefore it is focused on power and area efficiency. The overall system architecture utilizes eight chopper based amplifiers followed by the sample and hold blocks (S/H), the analog multiplexer (MUX) and the ADC. All of these blocks require their own clock signal that is locally generated and distributed by the on-chip RC based oscillator.
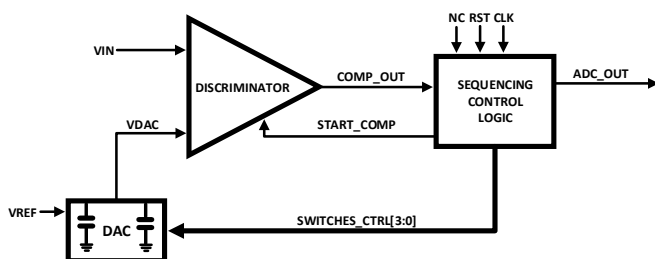
Fig. 1. Block diagram of the designed ADC.

Considering that the project application required low die area for analog-to-digital (A/D) conversion, while conversion speed was not critical, SAR architecture based on charge redistribution has been chosen, as illustrated in Fig. 1. It consists of Sequential Control Logic, discriminator and digital-to-analog converter (DAC).

Sequential Control Logic is a fully digital block, realized in $Verilog$ language. It manages the whole conversion by controlling Successive Approximation Register (SAR) and switches in DAC at the correct intervals.

Voltage discriminators are one of the most common elements in analog and mixed-signal designs and also one of the most critical ADC components due to their finite accuracy, speed, and power consumption. In this approach, clocked discriminator, which performs an operation at a specific clock controlled time, is used to reduce the power consumption. Detailed simulations have been performed to verify how the input transistors affect the discriminator's voltage offset, speed, current consumption, voltage noise, and voltage gain.

To build the most important block in the design, the DAC, charge redistribution technique was used. Compared to common charge redistribution techniques based on weighted capacitors, which exploits large numbers of unit capacitors, this approach utilizes only two equal capacitors, avoiding large area issues.

In the following sections, postlayout simulations are described. Based on the transfer characteristic, integral nonlinearity (INL) and differential nonlinearity (DNL) have been determined. Also, the power consumption for each block has been obtained. The parameters summary of the designed ADC is presented in the paper.

The circuit has been successfully tested with a clock signal from the on-chip oscillator and the preliminary measurements will be presented soon.

A 50 MHz, 46 μW, 0.28% Accuracy, 67 ppm/$^\circ$C Relaxation Oscillator in 40nm CMOS Process for Multichannel Integrated Biomedical Recording System

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Abstract—**This paper presents design of a high accuracy relaxation oscillator immune to the operating conditions and process variations. Presented oscillator is a part of multi-channel integrated system for biomedical recordings fabricated in the 40nm CMOS technology. By utilizing precision current reference source the 67 ppm/$^\circ$C temperature coefficient in the -20°C to 120°C temperature range and low sensitivity to the supply voltage in the range of 1V to 1.2V were achieved. With the use of digitally trimmed capacitors the 0.28% accuracy over process variations was also achieved. Additionally, to ensure self-sufficiency and reliable operation the oscillator was equipped with a power-on reset circuit.**

I. INTRODUCTION

Clock signal is required in almost every integrated circuit. The most common clock source are crystal oscillators. They are known to have the best accuracy and temperature stability, but these come at the expense of relatively large dimensions and high current consumption. Due to the mentioned factors on-chip clock sources are preferred in integrated circuits used in biomedical applications. One of the most popular clock generation solution is a ring oscillator, but usually its accuracy is greatly affected by voltage and temperature conditions. Due to the above, relaxation oscillators are the best choice as the clocking solution for biomedical ICs. With the use of digital calibration and high stability integrated reference current source, they can provide low power operation, low area, good accuracy and stability over PVT conditions ([1], [2], [3]). The most critical drawback of this circuits category is relatively high phase noise. However, this is often not of a concern in the low power applications.

II. OSCILLATOR ARCHITECTURE

Presented relaxation oscillator architecture idea [2] is based on two alternately charged capacitors, two schmitt triggers comparing voltage on the capacitors and a SR latch to control charging and discharging of the capacitors (Fig 1). The Q output of the SR is also used as the generator output.

The output frequency can be expressed as

$$f_{osc} = \frac{I_{REF}}{2CV_{TH}} - \frac{1}{2T_{delay}} \tag{1}$$

where I_{REF} is the value of the reference current, V_{TH} is the threshold voltage of schmitt triggers and T_{delay} is the delay between capacitors reaching V_{TH} and change in the switches state. T_{delay} will be further referenced as oscillator's loop delay.
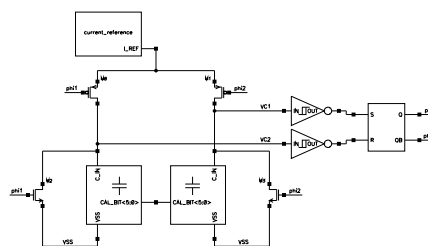
Fig. 1. Schematic idea of the relaxation oscillator.

From (1) can be derived that the oscillator's stability over voltage and temperature conditions is defined by the stability of the reference source and the accuracy depends on the V_{TH} of schmitt triggers, capacitors and the loop delay time variations. To reduce delay of the oscillator's loop skewed schmitt triggers were used instead of comparators. High stability across voltage and temperature changes is ensured by the reference generator immune to the operating conditions. Furthermore, process variations are compensated by digitally trimmed capacitors.

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A Flexible CMOS Test-Pixel Readout System

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EXTENDED ABSTRACT

The typical development cycle of image sensor pixel design starts with schematic and layout design followed by manufacturing of experimental silicon wafers based on a best-guess-simulation approach and ends in electro-optical characterization of the test pixels. Characterization of fabricated pixel variants is an iterative step which can not be avoided in pixel optimization. To allow for reliable results from measurement of various designs, usually a readout system is specifically developed which starts from capturing charge within the pixel which is then processed in a low-noise fashion keeping signal integrity as clean as possible to achieve desired pixel performance. This leads to high demands on the pixel readout circuitry, at the same time a large degree of universality of the readout platform, as the one proposed must be flexible enough to allow characterization of different pixel topologies.

Herewith we describe a flexible pixel readout system with a resolution of 256 x 256 pixels, tailored towards the characterization of charge-domain Global Shutter (GS) or Rolling shutter (RS) CMOS pixels based on a combination of column-parallel CDS and programmable gain amplifier (PGA) stage and a digital readout achieved with the deployment of a single on-chip ramp ADC. Digital input signal sequencing is controlled entirely through an field-programmable gate array (FPGA), which makes it possible to control the demands of various types of pixel architectures, such as 3T, 4T, 5T, 7T amongst others.

The system is composed of column analog signal processing, and row and global-level drivers for operation control of the pixel array. The column circuitry listed in order of the signal passage includes a low-noise current source, a column PGA with CDS capability, a column driver, a 12-bit ADC, and an analog video output driver. The row and column pixel modules are comprised of flexible slew-rate controlled voltage drivers with an external power supply for increased tuning range and external charge injection capabilities. Globally, the chip relies on simple local bias references based on the beta multiplier technique and a digital serial configuration interface. The video signal is fed out in both digital and analog formats using standard 12-bit Digital Video Parallel (DVP) and video outputs.

The design of the pixel test chip involves tailoring the readout circuitry to the specifics of the pixel array. The current implementation uses a 7T vertically shared charge domain global shutter pixel whose schematic and control sequence is described in this paper. The row driver is connected horizontally to the pixel which has an $N/2$ readout control lines in the vertical direction for an array with N resolution. To allow for better flexibility and re-use of the readout in non-shared arrays. On the upper side of the pixel array global control signal sequence is generated from the global driver module.
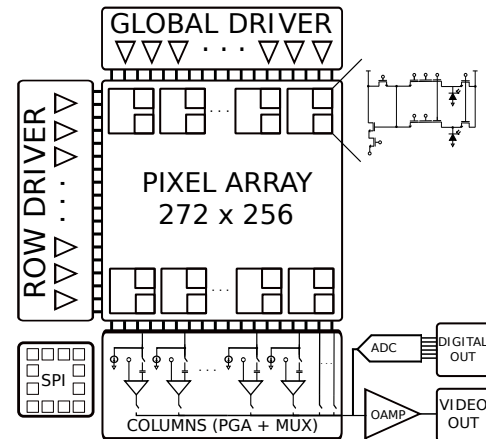
Fig. 1. Block diagram of the presented readout system

The readout signal from the pixel must be conditioned in a way that allows for the cancellation of 1/f and kTC noise from the pixel while allowing additional gain early in the signal path for better pixel noise performance characterization. A column-level PGA with two gain settings was chosen which allows a characterization coverage in high and low-light illuminations, respectively covering high and low pixel conversion gains.

Due to the column-parallel signal processing nature, by design, variation between individual columns can be present, which is mostly dominated by non-idealities of the PGA. Correlated Double Sampling was employed to suppress FPN from the pixel array which results of CFPN to be less than 1 %. An addition low-offset high-gain amplifier architecture was used. This reduced PGA offset errors to about 1 LSB on the 12-bit ADC, or measured under typical operating conditions to be about 350 uV RMS.

The column-parallel output of the PGA is serialized owing to ring-counter-controlled transmission gates, which multiplex the output column to a serial voltage bus. Having a serial column bus imposes high parasitics on the signal path which limit the readout bandwidth significantly. An effort must be put towards coupling optimizations to achieve the fast settling. The video information from the serial bus is being delivered off-chip via both analog video and parallel 12bit DVP digital output.

The characterisation results and acquired test images show good column uniformity over a wide input signal range. A flexible pixel row and global driver scheme using external voltage control were introduced to allow all possible testing conditions of the pixel. Due to the complete freedom in pixel array control signaling and variable voltage level control, this sensor makes a preferable pixel test vehicle for research purposes in designing new pixel architectures which will be used in end-products as a line scan image sensors.

A New FPGA-based Architecture of Task Scheduler with Support of Periodic Real-Time Tasks

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EXTENDED ABSTRACT

Real-time task schedulers are usually implemented in software, but software-implemented task schedulers are very limited in task scheduling algorithms that are being used because of the requirement for constant and low amount of CPU time spent for task scheduling. As a result, these software-implemented schedulers are mostly based on priorities, not the actual deadlines of real-time tasks. This leads to lack of robustness and efficiency in scheduling itself. A possible solution to these problems is hardware acceleration. Real-time task schedulers can be implemented in hardware, which allows to use deadline-based scheduling algorithms, to minimize the time spent for scheduling and make it constant too. The existing task schedulers that are implemented in hardware are mostly applicable for very simple systems that consist of aperiodic hard real-time tasks only. These solutions are not suitable for more complex, robust real-time systems with higher number of tasks and bigger variability of task types. Therefore, a more robust and complex task scheduler with a support of various types of tasks is required. Furthermore, real-time systems often contain periodic tasks in addition to aperiodic tasks too. Even though periodic tasks can be handled by task schedulers the same way as aperiodic tasks, adding a dedicated support of periodic tasks directly inside the HW-based scheduler improves the overall system performance due to reduced CPU overhead.

This paper presents a new FPGA design of a task scheduler that supports not only aperiodic hard real-time tasks but periodic tasks too. Whenever a period of a periodic task is elapsed, the task is automatically restarted with no need of software intervention. The proposed scheduler is using Earliest Deadline First (EDF) algorithm. For inter-task synchronization, the scheduler also supports temporary suspension of tasks with automatic resumption of tasks after the specified time elapsed. The proposed architecture is based on priority queues used for time management and decision-making processes. Thanks to FPGA implementation of the scheduler and its priority queues, the scheduler operations are always performed in two clock cycles regardless of the current number of tasks and regardless of the maximum possible number of tasks too. The proposed solution was verified using simplified version of Universal Verification Methodology (UVM) and applying millions of test instructions with randomly generated deadline and period values.

The proposed scheduler is designed in a form of a coprocessor unit that is getting instructions from CPU and providing instruction results back to the CPU. This means that the scheduler is expected to be wrapped by / integrated into an existing CPU, similarly as arithmetic coprocessors or any other coprocessor units. Figure 1 shows a top module of the proposed scheduler that consists of 7 components: Semaphore, Control Unit, Running Tasks, Tasks Memory, Idle Queue, Waiting Queue and Ready Queue.
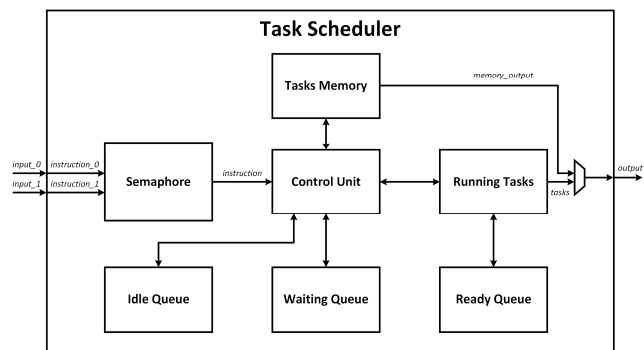
Fig. 1.   Top-level module of proposed scheduler

The proposed scheduler is suitable for robust real-time systems that can contain aperiodic hard real-time tasks, periodic hard real-time tasks and best-effort (non-real-time) tasks. The proposed solution uses an approach that is based on the priority queues. The priority queue structure is used not only for sorting of ready tasks but for periodic idle tasks and blocked/waiting tasks too. Thanks to these priority queues, handling of periodic idle tasks and blocked/waiting tasks is efficient and simple. The handling of periodic tasks and waiting tasks is fully autonomous, requiring no software intervention apart from the initial configuration of Tasks Memory. Thanks to that, the proposed scheduler is very efficient in managing periodic tasks and is very suitable for further software extension containing task synchronization and inter-task communication. The proposed scheduler can be used for CPUs that can execute two tasks in parallel. All instructions that are supported by the proposed scheduler require only 2 clock cycles to perform, regardless of system configuration and actual or maximum number of tasks in the system.

Analytical Calculation of Inference in Memristor-based Stochastic Artificial Neural Networks

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Abstract—**The impact of artificial intelligence on human life has increased significantly in recent years. However, as the complexity of problems rose aswell, increasing system features for such amount of data computation became troublesome due to the von Neumann's computer architecture. Neuromorphic computing aims to solve this problem by mimicking the parallel computation of a human brain. For this approach, memristive devices are used to emulate the synapses of a human brain. Yet, common simulations of hardware based networks require time consuming Monte-Carlo simulations to take into account the stochastic switching of memristive devices. This work presents an alternative concept making use of the convolution of the probability distribution functions (PDF) of memristor currents by its equivalent multiplication in Fourier domain. An artificial neural network is accordingly implemented to perform the inference stage with handwritten digits.**

Keywords—**artificial intelligence, memristor, stochasticity, framework, modeling, simulation, neuromorphic computing**

I. INTRODUCTION

Neuromorphic computing aims to solve the von Neumann bottleneck in the implementation of Artificial Neural Networks (ANN). The structure of an ANN is based on the neurons and their connections in the human brain. Here, those connections, namely, the synapses, are built of memristors. Memristors are electronic circuit components that have the ability to switch their resistance depending on the amplitude and the polarity of the voltage that is applied to them. They were predicted by L. Chua in 1971 as the fourth elemental circuit component that defines the relation between flux and charge [1].

The efficacy of the synapses depends highly on the neural activity of the respectively coupled neurons. This results in a flexible and adaptive interconnection between neurons, leading to a phenomenom called synaptic plasticity [2], [3]. A similar phenomenom is observed in memristive devices [4]. Considering the memory paradigm, memristors are usually switched into two different states, namely HRS and LRS by means of the reset and set operations, respectively. However, the multilevel-cell (MLC) capability allow memristors to switch their conductance into intermediate levels, mimicking the multiple synaptic states of a neuromorphic system.

For the implementation of a neural network, a HfO_2 based memristor crossbar array consisting of 1-Transistor-1-Resistor (1T1R) cells is investigated. Their usage is of extreme interest because of their ability to operate at a very low power while still being very efficient and fast [**?**]. In its design process the statistical variation of modulation of the conductive filament has to be considered.

In particular, the pattern recognition of the MNIST dataset will be taken into focus in this work. In this work, a reduced dataset consisting of 42.000 samples that contain pictures of handwritten digits from 0-9 is used. They have a size of 28x28 pixels. Each pixel inhibits a grey level between 0-255. An offline training of a software based neural network is performed to extract its predicted classification and compare it to the simulation using the analytical model.

The inference delivers fixed numbers as output values and does not consider a statistical variation of synaptic elements while calculating the classification by the "winner takes all" method. However, the model in this work determines the resulting Gaussian distribution function of each column inside of the memristor matrix and computes a probability that can be compared to the output values of the software based solution. This approach allows a deeper analysis in terms of optimization of devices, architectures and more.

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Clock Signal Phase Alignment System for Daisy Chained Integrated Circuits

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Abstract—**Phase difference of the clock signals is a critical factor in high precision synchronization of interconnected integrated circuits. In order to synchronize a daisy-chained set of individual systems, a novel concept of clock signal phase alignment circuit as well as calibration algorithm were developed. The work describes a high-level analog circuit and the calibration procedure implemented in the digital control module. The high-level implementation was tested using Verilog HDL language and conclusions are presented. Moreover, the required features and recognized restrictions are also discussed.**

Keywords—**clock signal; synchronization; daisy chain; phase synchronization; phase alignment; modular arithmetic.**

I. INTRODUCTION

Synchronization of multiple individual systems is a major issue. Its importance increases with the demand for higher precision, reliability and speed. Over the years, multiple synchronization methods were invented, but most of the current approaches cover only the high-level synchronization with the accuracy of one microsecond or better [1] – even when a custom ASIC has to be designed [2]. Typically, IEEE 1588 (PTP) standard [3] is implemented in such cases.

However, for some applications the time synchronization is not sufficient, and the phase of the clock signals needs to be aligned as well. Very few papers approach the problem of clock phase alignment independently [4] [5] [6]. Current approaches focus on aligning each device with the same reference clock signal.

For applications where time synchronization with precision below a single clock period value, a White Rabbit protocol was developed [7]. This standard has various advantages, but is complicated and requires additional equipment (e.g., WR switches), which makes it a good solution for relatively big or compiled networks. For small and simple networks, such as daisy-chain connection of induvial ASIC chips, the White Rabbit protocol might be excessive.

II. MOTIVATION

The motivation of this work is to develop a clock signal phase alignment system for a for system composed of individual ASIC devices. One of the use cases for the ASIC (therefore the described system as well) is a vacuum chamber actively cooled down to cryogenic temperature. Due to other requirements, multiple units of the designed ASIC system will be connected using as few signals as possible, hence a daisy chain connection topology [6].

III. CONCLUSION

The proposed circuit for clock signal phase alignment together with the calibration algorithm was presented. All the original assumptions and requirements listed in the article were met. The calibration algorithm was determined to work correctly and may be further improved in the future works. The general idea was implemented with Verilog HDL language and functionally verified by presented simulation results. The presented concept is an on-going work and will be researched and developer further using a FPGA-based prototype as well as a dedicated ASIC system afterwards.

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Comparative Analysis of CMOS Latch-Driver Circuits for Current-Steering Digital-to-Analog Converters

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EXTENDED ABSTRACT

With higher demands for channel bandwidth in current-steering (CS) digital-to-analog converters (DACs), faster and less power-hungry latch-driver circuits are needed to maintain data synchronization and counteract for augmented power consumption with increased sampling frequency, f_s. Moreover, as differential CS DACs are mainly implemented, they require rapid and symmetric complementary control signals to drive the switch transistors in the differential pairs to mitigate distortion at the output [1]. To illustrate, Fig. 1 shows the voltage variation in the common-node (S) for different complementary voltage transitions of the control signals sw and $\overline{sw}$ with the mid-point inducing less voltage excursions and representing a close optimum operating condition.

Different complementary CMOS latch-driver circuits have been implemented in CS DACs, and this become more relevant as the design requirements are more stringent to energy-efficient CS DACs [2]. Implementations of latch-driver circuits typically employ complementary CMOS and current-mode logic (CML), respectively. Although high-speed operation can be achieved with CML circuits [3], the utilization of current sources add a static power consumption component, which is also subjected to increase if higher switching speeds are required along with larger device dimensions. An intermediate solution is the utilization of both CML and complementary CMOS logic as CML-to-CMOS logic circuits [4]. Yet, down-scaling of device dimensions in CMOS with reduced parasitic capacitance suggest the utilization of complementary CMOS with increased speed and reduced power consumption.

Therefore, in this paper a comparative analysis of single- and dual-phase-clocked CMOS latch-driver circuits aimed at current-steering (CS) digital-to-analog converters (DACs) is presented. The analysis considers the design metrics of power consumption, propagation delay as well as the introduction of the time delay between complementary switching transitions referred to as switching-delay. Furthermore, an alternative latch-driver is proposed with the intent to sustain low-power consumption and rapid switching transitions, i.e., a short switching-delay. An industrial 65 nm CMOS process is used
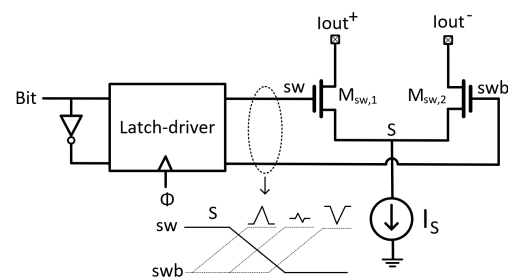
Fig. 1. Latch-driver and N-type differential pair with common-node (S) voltage variations for different sw and $\overline{sw}$ transitions.

for the comparison and the results are obtained from post-layout simulations, respectively.

From the analysis, the single-phase-clocked circuits are the less power hungry and report the largest switching-delay between complementary transitions. On the contrary, the dual-phase-clocked circuits report $5.9\times$ shorter switching-delay while consuming about $2.4\times$ more power with respect to the single-phase-clocked circuits. On the other hand, the proposed latch-driver consumes about $1.6\times$ more power with a switching-delay response approximated to the dual-phase-clocked solutions instead. Further on, the normalized product between the switching-delay and power consumption is presented, where the proposed latch-driver reports the smaller product within 1.0 and 1.57, which accounts for about 70% and 30% reduction with respect to the single- and dual-phase-clocked circuits in the supply voltage that ranges from 0.8 to 1.2 V.

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Design Optimization of a New Nanostructured P-GaN Gate for Normally-off GaN HEMTs

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Abstract—**A new AlGaN/GaN heterostructure is proposed to achieve a normally-off behavior for GaN HEMTs. It relies on multiple P-GaN wells epitaxial regrowth along the gate. Simulation results are presented by focusing on the physical and geometrical parameters of the P-GaN wells. The normally-off behavior of the novel HEMT is demonstrated.**

Keywords—**HEMT; P-GaN gate; normally-off; TCAD simulations**

I. INTRODUCTION

GaN HEMT transistors are promising devices for power applications due to their superior material properties, such as electron saturation speed and high carrier density in the two-dimensional electron gas (2DEG), which allows them to operate at very high current densities and frequencies. E-mode (or normally-off) devices are required to simplify system architectures and improve safety when control circuit failure.

In this paper, we propose a novel gate structure for normally-off AlGaN/GaN HEMTs as described on Fig. 1.a. It requires a nanostructuring of AlGaN and GaN layers by dry etching and a localized epitaxial regrowth of P-doped GaN wells in the resulting nanotrenches. Here an accurate control of the gate recess is not required, the well etching going through the AlGaN layer until it reaches the underlying GaN layer. The introduction of P-GaN wells induces the 2DEG depletion of the channel without gate bias. Design and optimization of the P-GaN wells are described. The simulated electrical characteristics of the novel AlGaN/GaN HEMT highlight its normally-off behavior.

II. RESULTS

2D and 3D simulations were performed with Sentaurus TCAD tools in order to evaluate the lateral depleted area extension in the gate channel region at thermodynamic equilibrium for different technological conditions : P-GaN well size (depth e_T and width L_T), P-GaN doping, thickness and aluminum content of the AlGaN layer (Fig. 1.b).

It was determined that a 100 nm depth is necessary to obtain a maximum depletion area extension whatever the physical parameters of the P-GaN wells. The minimum well width increases when P-doping decreases and is poorly dependent on the aluminum content in the AlGaN barrier for doping concentrations higher than 5×10^{18} cm^{-3}. For a P-doping concentration of 10^{19} cm^{-3}, the minimum width value required to develop the depletion zone is 26 nm. For a P-doping concentration of 2×10^{18} cm^{-3}, this value varies from 75 nm to 100 nm for an Al content ranging from 15 % to 25 % respectively.

The depleted area extension increases by decreasing the 2DEG density, i.e. by reducing the AlGaN layer thickness and by decreasing its Al content, and also by increasing the P-GaN doping.

Simulations of half a HEMT cell with a 20 nm barrier, a 20% aluminum content and 10^{19} cm^{-3} doped wells were performed. Positive threshold voltages are obtained with a Schottky contact on the wells with different well spacing D_T, validating the normally-off functionality (Fig. 2). The off-state simulations will be also presented.

This novel structure paves the way for the integration of advanced power functions.
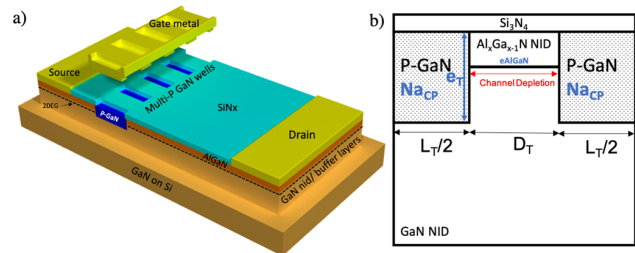
Fig. 1. 3D view of the proposed HEMT structure (a) and schematic cross sectional diagram of the simulated gate cell (b)
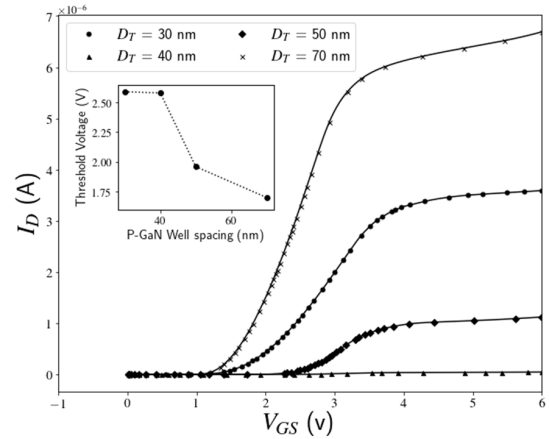
Fig. 2. Simulated ID(VGS) characteristics and threshold voltage variation (inserted curve) for different cell spacing for half a HEMT cell at VDS=1V

Design of 1.55 NEF, 2μA, Chopper Based Amplifier in 40nm CMOS for Biomedical Multichannel Integrated System

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ABSTRACT

We present a design of a low-noise chopper based amplifier for biomedical recordings. It is a part of a multichannel integrated system fabricated in $40nm$ CMOS technology. It features a DC stabilizing loop for compensating electrode offset and positive feedback for input impedance boosting. The first stage uses double current reuse. Design consumes $2\mu A$ per channel under $1V$ supply voltage and occupies only $0.044mm^2$ of silicon area. A novel input stage presented in this work combines a low noise performance of a stacked input pair with the high DC gain of the folded cascode amplifier. The simulated input-referred noise is $0.96\mu Vrms$ in the 0.5–100Hz frequency band and $2.8\mu Vrms$ in the 100Hz–10kHz frequency band, respectively, leading to a noise-efficiency factor of 5.29 (0.5–100Hz) and 1.55 (0.1–10kHz).

Fig. 2. Measured noise with DSL switched off.
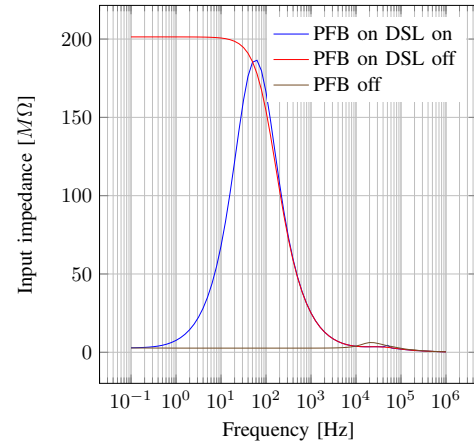
Fig. 3. Simulated amplifier input impedance.

Fig. 1. Dual current reuse Gm_1 stage of the chopper amplifier.

$$Gm_1 = 2\alpha(gm_{1,3} + gm_{2,4}) \tag{1}$$

$$\alpha = \frac{ro_{1,3}||ro_{2,4}}{(ro_{1,3}||ro_{2,4}) + X_c + 2R_{in\_cas}} \tag{2}$$

$$V_{ni\_Gm1}^2 \approx 2\gamma kT\left(\frac{1}{Gm_1} + \frac{gm_{19} + gm_{13}}{(Gm_1)^2} + \frac{1}{(gm_{14} + gm_{20}) * (R_{in\_cas})^2 * (Gm_1)^2}\right) \tag{3}$$

Observation of Readout Temperature Dependence and Its Variability for the MEMS and ASIC System Specimens and Their PCB Testbenches

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EXTENDED ABSTRACT

The presented work provides results and discusses implications for introductory comparison of test results of temperature dependence of the integrated semiconductor system designed as a part of a system for imbalance disorder monitoring. Two types of test chips are taken into account, each of them mounted on two PCB versions, provided by different manufacturers. These are the ROIC and MEMS&ROIC setups. They consist of the ReadOut IC (ROIC) and MEMS and ROIC (Fig. 1) structures, respectively.
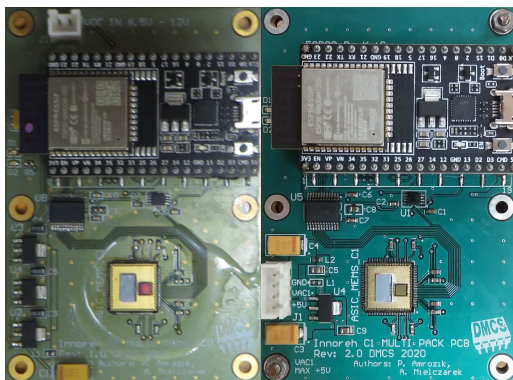
Fig. 1. The MEMS&ROIC chip on the PCB of the original (left) and modified (right) design

An extensive comparison of results of several test sessions was carried out. The main type of measurements taken into account is the temperature dependence of the mean readout value [1, 2]. Several observations have been made. Among the most important ones is that the dominant share of the measurement temperature dependence of mean readout values is caused by the MEMS structures [1].

Moreover, the ratios of temperature dependence for the MEMS&ROIC and ROIC-only setups are all comparable, provided that both setups taken into account utilize PCBs from the same manufacturer. Fig. 2 shows this effect especially in case of M&R.1 and M&R.2 setups that utilize PCBs provided by different companies.
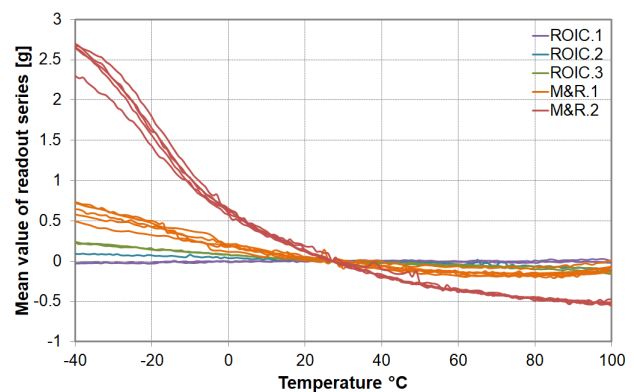
Fig. 2. Temperature dependence of mean readout values for all ROIC-only (ROIC.1 to 3), and MEMS&ROIC setups (M&R.1 to 2).

Finally, it was found that the temperature dependence for the test setups based on the original version of PCBs is several times smaller than that in their corresponding setups based on the redesigned PCBs provided by a different manufacturer.

Due to the possible significance of the comparison results, challenged by a very limited number of available test setups, the decision was taken to prepare the new version of the MEMS&ROIC test setup with a specialized test socket.

The socket-based PCB has been prepared, manufactured and fully fitted with all necessary components, including the test socket. Tests are about to begin. They should provide further insight into the causes and extent of the temperature dependence and its variability encountered in the measurement results, so as to provide knowledge to minimize these effects.

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SPAD Mixed-Quenching Circuit in 0.35-μm CMOS for Achieving a PDP of 39.2% at 854 nm

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EXTENDED ABSTRACT

This paper presents a fully-integrated optical sensor with SPAD and mixed quenching/resetting circuit with sensing stage based on a tunable-threshold inverter optimized for the standard 0.35-μm CMOS technology. The presented quencher features a controllable detection threshold voltage and an adjustable total dead time. The quenching circuit 5QC achieves 16.5 V excess bias voltage (five times the supply voltage). The dead time ranges from 7.5 ns to 51.5 ns. The quencher is optimized for SPADs with a capacitance ranging from 50 fF up to 400 fF. Using our published measured photon detection probability (PDP) results and extrapolating them, a peak PDP of 75.6% at 652 nm and a PDP of 39.2% at 854 nm is estimated for $V_{EX} = 16.5$ V.

The proposed quenching circuit consists of the following blocks: quenching/resetting switch, sensing and current-cutting stage, dead-time control stage, voltage translators, and quenching MOSFET disabling circuit
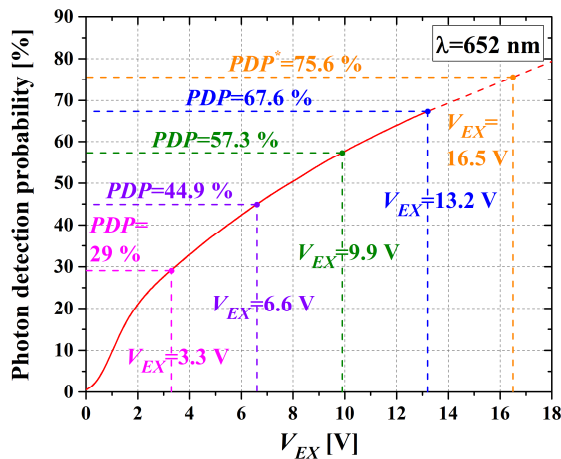
Fig. 1. Measured and estimated (*) red spectrum PDP (λ=652 nm).

Figures 1 and 2 show the measured and extrapolated PDP for the red (λ = 652 nm) and NIR (λ = 854 nm) spectrum. The authors have performed an extrapolation in MATLAB for the PDP based on the spectral PDP measurements from the previous tapeouts in the same technology, where two quenching circuits, AQRC99 [1] and AQRC132 [2], have been fabricated. The solid line represents measured results (up to 13.2 V) and dashed line represents extrapolated results (up to 18 V) for the same CMOS technology. So far, the highest peak PDPs for integrated SPADs of 71%, 67.6%, and 62.2% were reached in [3], [2] and [4], respectively.
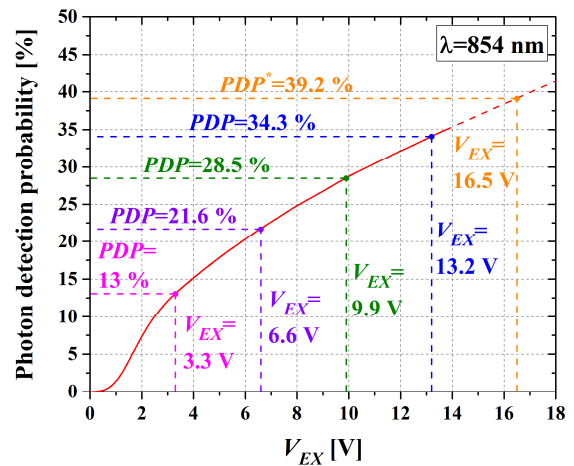
Fig. 2. Measured and estimated (*) NIR spectrum PDP for λ=854 nm.

The estimated peak PDP of 75.6% is even higher than reported in [5] for an external SPAD wire-bonded to a circuit fabricated in a high-voltage 0.35-μm Bipolar-CMOS-DMOS (BCD) process. To the authors' best knowledge, the presented PDP result has never been reached before for a fully-integrated SPAD sensor in standard CMOS technology.

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Ultra Low-Power, Area-Efficient Multiplier Based on Shift-and-Add Architecture

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Abstract—**Shift-and-add multipliers have a simpler structure than other types of multipliers and, at the same time, have a lower operating speed. They are suitable for applications where speed is not the first design priority. In this paper, we present a low-power, low-area multiplier with a simplest possible structure based on shift-and-add which can be a good choice for portable applications and medical devices such as a pacemaker, where power reduction and chip occupation are core issues. The main idea of the article is to use multiplexers and appropriate timing signals. By applying these signals to the multiplexer selection lines, it is possible to achieve the correct output with an n-bit adder and input-output registers during (2n+1) clock pulse. Simulation results of proposed 16*16-bit multiplier using HSPICE in standard 0.18μm CMOS technology demonstrate that it has 129ns propagation delay while the corresponding power consumption is 467μW.**

Keywords— **Shift-adds multiplier, timing signal, multiplexer, CMOS technology**

I. PROPOSED STRUCTURE

Figure 1 shows the proposed multiplier structure based on shift and addition. The designed multiplier consists of an n-bit adder, n logical gates (two input AND gates), two n-bit registers, and a shift register with a length of 2n bits, which is designed with the least possible hardware. There is always a direct relation between the speed and hardware. The lower the hardware the lower the speed. Hence our proposed structure is appropriated for low-speed and low-power applications as well. Here we look at an 8-bit structure that can be easily extended to higher number of bits.

Fig. 1. Proposed shift-add multiplier structure

TABLE I.
PERFORMANCE COMPARISION

Ref.	Technology (nm)	Width (Bit)	Delay (ns)	Power (mW)	Number of transistors or (Area (μm²))
[3]	130	16	9.76	4.97	3903 (μm²))
[5]	180	16	2.5	35.8	13444
[6]	180	16	1.5	37	7268
[7]	350	16	7.4	33.7	12349
[8]	180	32	2.1	41	53700
[9]	180	16	5.7	2.65	52414 (μm²)
This work	180	16	129	0.467	1520
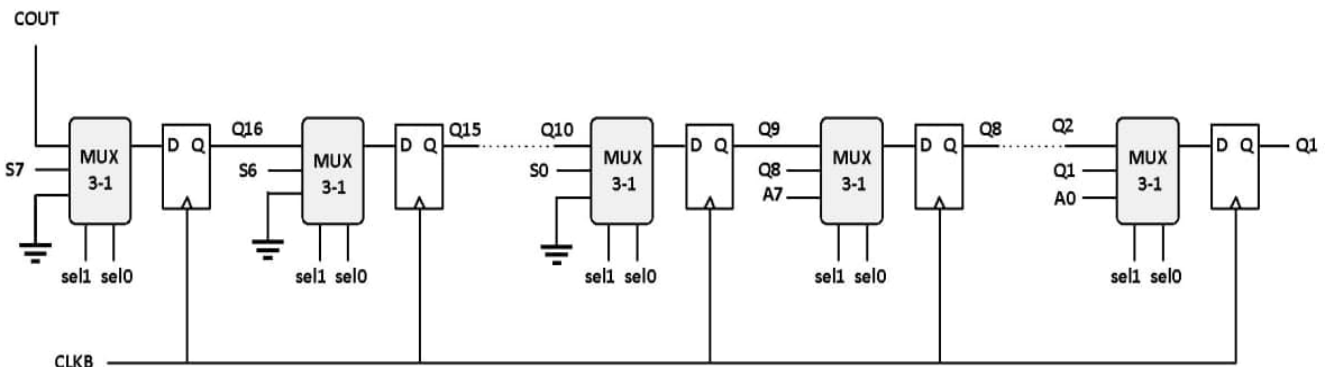
Fig. 2. Internal structure of the register shift

Power Electronics

Comparison of Photovoltaics System Response with Constant and Variable Step MPPT Algorithm

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EXTENDED ABSTRACT

The basic foundation for obtaining maximum power is reaching the maximum operating point (Maximum Power Point), which makes it the highest possible power produced by the panel in the given solar and temperature conditions. Achieving this power requires adjusting the voltage in the work cycle, which unfortunately requires a kind of "search" by "sampling" the value of the instantaneous power at a given voltage. However, it takes a certain time to reach the maximum power, which implies power losses. One of the best known and quite simple MPPT algorithms is P&O (Perturb and Observation). Its operation, however, has a certain disadvantage related to the abrupt change of parameters, which in certain situations does not allow to obtain the optimal operating point. The paper compares the results obtained from the model with the P&O algorithm used at a constant and variable step.
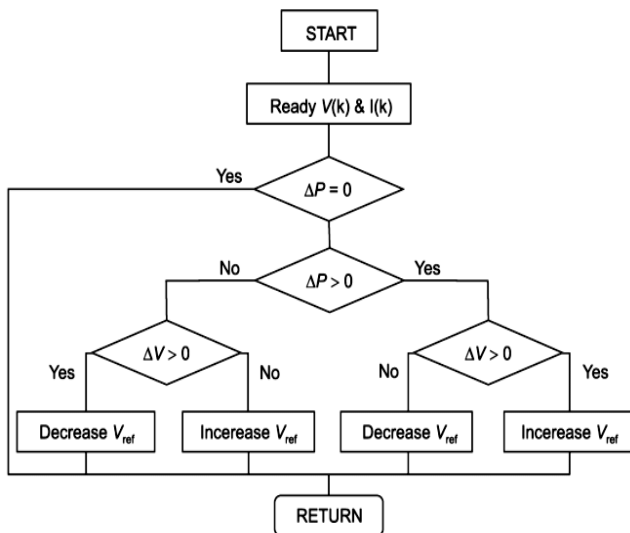
Fig. 1. MPPT algorithm.

MPPT (Maximum Power Point Tracking) is one of the key elements of photovoltaic systems - the controller, which is an electronic "intelligent" DC / DC converter. It optimizes the match between PV panels and the power grid (in the case of an on-grid system). It is essentially the interface between the load and the PV cells - it controls the duty cycle to get the maximum power of the PV cell taking into account environmental conditions such as grid demand.

The analysis of the functionality of the MPPT algorithm is carried out on the basis of the model created in Matlab / SIMULINK.

Fig. 2 show example power plots as a function of time for four levels of irradiance for the applied P&O algorithm (335W panel) with a fixed step (blue) and a variable step (red) for a temperature of 25 ° C. At first glance, you can see that the time to reach the maximum power in the case of the variable step algorithm is much shorter than in the case of the fixed step (in some cases even twice). It can also be noticed that the oscillation amplitude with a variable step is significantly smaller.
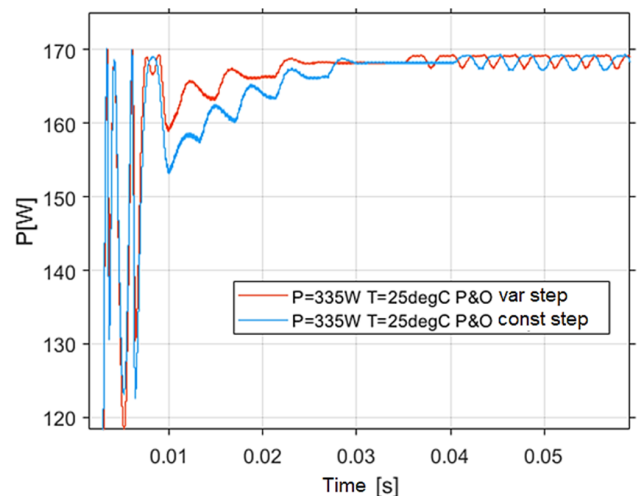
Fig. 2. Characteristics for Ir=500W/m^2.

During the individual levels of irradiance, it was clearly visible that the time courses of the instantaneous power values differ from each other, which is quite interesting - for irradiance 800 W / m^2 for example, the waveforms started to vary depending on the previous level of irradiance. In the case when the previous level of irradiance has a lower value, the upward trend in power is more pronounced and has much smaller oscillations than in the case when the value preceding irradiance is higher.

DC/DC Buck Converter Soft-Start Methods

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Abstract—**Startup issues of DC/DC converters can be problematic, and even cause malfunction of the whole system. In this paper selected problems encountered during the DC/DC converter design process are described and solutions are provided. The first solution uses a modified driver, which limits the loading current during startup. The second solution uses a modified passive switch soft start [1], which based on linearly charged capacitance and output voltage detector with D flip-flop. The described solutions have been designed and fabricated using CMOS 110 nm technology.**

Keywords—**DC/DC converter, inrush current, soft-start, parasitic inductance, CMOS, feedback loop.**

I. INTRODUCTION

Limiting power consumption is becoming an increasingly important topic these days. In order to decrease losses due to power conversion, high efficiency power supply converters are necessary. That makes switching mode DC/DC regulators key blocks in portable devices, therefore their reliability, accuracy and cost are a significant problem. Although the basic diagram of the converter is quite simple, in practical applications many additional phenomena should be taken into account.

II. PRACTICAL ASPECTS OF DESIGN

A. General design specification

The designed DC/DC converter should work with a 2.5–4.3 V input battery voltage. The processor supplied by requires a 10–300 mA load current, and 2.2 V output voltage. The basic design goal was to achieve maximum energy efficiency in a wide range of operating parameters. Converter is controlled with driving based on PWM circuit using voltage mode control has been designed in CMOS 110 nm technology. Due to the presence of other systems in this integrated circuit, the operating frequency is in the range of 800–900 kHz. The frequency and the inductance of the coil have been selected in order to simultaneously limit the physical size of the inductor and its resistance. Apart from the inductance and output capacitance all the operating elements were integrated into a single chip. The output capacitor (50 µF) and inductance (4.3 µH) are placed off chip due to their dimensions. This work is a continuation of the research described in [2].

B. Inrush current

The general schematic shown in Fig. 1 is similar to the one presented in the previous work. The main difference is the load current, which was increased twice. As a consequence the width of the driving MOS transistors (T0, T1) had to be increased. This change significantly increased the inrush current. The simulations showed that it could reach even 4–5 A, which is unacceptable in the selected technology. This large current had to be limited in order to protect the system from damage.

C. Parasitic serial inductance

The bonding inductance of the integrated circuit turned out to be the second major problem. After taking into account the parasitic inductance of 700 pH in series with the input voltage (VDDH), a number of undesirable effects appeared in the simulation results. When the input current of the converter changes, a voltage drop across the parasitic inductance is generated, which can be described by the following formula:

$$V = \frac{\Delta i}{\Delta t} * L.$$

Assuming that $\Delta i \cong 3$ A, $\Delta i \cong 1$ ns, and L = 700 pH, the voltage drop due to the parasitic inductance is significant (2.1 V) and must be taken into consideration. The situation is even worse if the feedback loop is powered from the same pad, which reduces the supply voltage of the loop circuit.

III. CONLUSION

In this paper, the DC/DC buck converter has been presented. To verify its operation, circuit simulations were performed in Cadence SPECTRE.

Problems related to starting the converter are described in this article. Most of theme resulted from the effect of bonding inductance. Two different solutions have been proposed, i.e. a modified driver and a modified passive switch soft start . The use one of the two proposed solutions avoids unwanted effects, namely the influence of the series bonding inductance and the resulting interference of the sawtooth voltage or the driver voltage. The first solution i.e., a system using the modified driver has been fabricated and measured. The measurements showed that the converter works properly.

Influence of the IGBT Module Thermal Model Form on the Accuracy of Electrothermal Computations

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EXTENDED ABSTRACT

IGBT modules are often used in power electronic systems. They contain power semiconductor devices, often connected into one branch of the inverter, situated in a common case. During the operation of these devices, their junction temperature increases due to thermal phenomena.

An increase in the junction temperature of semiconductor devices causes changes in the values of their parameters, changes in the course of their characteristics and shortening of their life time. Therefore, it is important to accurately compute the junction temperature of these devices during their operation. To compute non-isothermal characteristics, taking into account the influence of thermal phenomena on the relationship between the currents and voltages of the device, electrothermal models are used.

The aim of modelling is to obtain the most accurate description of the properties of the actual device with the least computational effort. In the case of the electrothermal model of the IGBT module, it is necessary to use electrical models and heat generation models of all its components and the thermal model of the module. This work is devoted to an IGBT module containing 2 IGBTs, 2 diodes and a thermistor.

In the paper an influence of the form of the applied thermal model of the IGBT module on the accuracy of computing the DC characteristics of the components of this module operating under various cooling and power conditions is investigated. The investigations are carried out using the electrothermal model of the IGBT module. This model uses the form of electric models of transistor, diode and thermistor as well as the heat generation model and various forms of a thermal model. Three forms of the compact thermal model of the considered module are considered. Model A takes into account only self-heating in each component of the module. Model B additionally takes into account the mutual thermal couplings between the components of the module. Model C additionally takes into account the dependence of thermal parameters on the power dissipated in the module components.

In order to illustrate the influence of the form of the applied thermal model on the DC characteristics of this module, computations are carried out with the use of an electrothermal model of the considered module, in which thermal models A, B and C are successively applied.

As an example, Fig. 1 shows the output characteristics of transistor T_1 at voltage $V_{GE1} = 6.6$ V for the module operating without any heat-sink. The investigations were performed at different values of the power p_{T2} dissipated in transistor T_2. In this figure, points denote the results of measurements, and lines

- the results of computations with the use of model A (blue), model B (green) and model C (red). In addition, black dashed lines represent the results of isothermal computations.
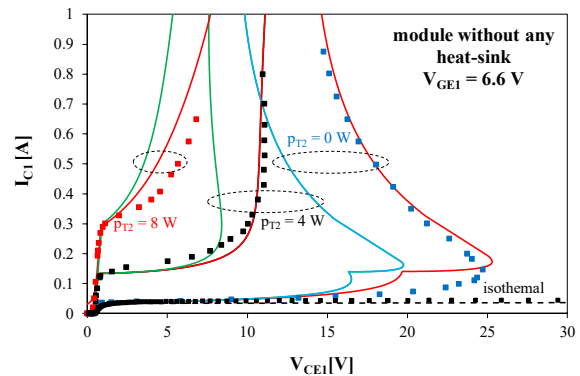
Fig. 1. Computed and measured output characteristics of transistor T_1 at different values of the power p_{T2} dissipated in transistor T_2

The shape of the presented nonisothermal characteristics visibly differ from the isothermal characteristics. The nonisothermal characteristics are not any functions in a mathematical sense. We can see on them the point of the electrothermal breakdown, in which a sign of inclination of this characteristic changes. The value of voltage V_{CE1}, at which appears the point of electrothermal breakdown decreases together with an increase of the power dissipated in transistor T_2. As a result of thermal phenomena the value of the collector current of the examined transistor increases at an increase in the power dissipated in the other component of the module. It is also proper to notice that changes of the shape of characteristics $I_{C1}(V_{CE1})$ are accompanied by the essential changes in it temperature equal to even 80°C.

As can be seen, model C ensures the best agreement between the computation and measurement results for all the considered operating conditions. Model B allows obtaining a satisfactory agreement between these results only in the range of low values of the power lost in transistor T_1. With an increase in this power, the discrepancies between the results of computations and measurements increase. In the range of high values of current i_{C1}, voltage v_{CE1} is lowered even by 30%. On the other hand, model A does not take into account the influence of the power lost in transistor T_2 on the characteristics of transistor T_1 and has the same course for all supply conditions. As a result, in the case of power dissipation in the transistor T_2, the computed characteristic differs significantly from the measured one. For example, the collector current i_{C1} values are lowered up to 13 times.

Influence of the Measurement Method and the Cooling System on the Obtained Values of the Junction Temperature of Power MOSFETs

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EXTENDED ABSTRACT

The value of the junction temperature of a semiconductor device cannot be measured directly because the semiconductor chip is contained in an airtight case. Therefore, this temperature is measured using indirect electrical methods, optical methods and contact methods. In electrical methods, the value of the junction temperature T_j of a device is determined on the basis of the measured value of the electrical parameter of this device with a known and unambiguous dependence on the temperature. On the other hand, optical and contact methods make it possible to measure temperature T_C on the surface of the device case, which is lower than temperature T_j.

This paper presents the results of investigations illustrating an influence of the used measurement method on an error occuring while determining the junction temperature of the power MOS transistor. The tests are carried out for power MOS transistors operating in different cooling systems. The influence of the design of the cooling system and its operating conditions on the considered measurement error are discussed.

The tests were carried out for two power MOS transistors of the IRF840 type mounted in the TO-220 case. The tested transistors are placed on the PCB and they cooperate with different cooling systems. During the measurements, the power is dissipated only in transistor T_1. The temperature of transistor T_2 increases only due to mutual thermal couplings.

In system A transistors operate without any additional cooling components. Systems B and C use a fan. In system B transistors are placed on the intake side of the fan, whilst in system C transistors are placed on the exhaust side of the fan. In system D, the transistor is mounted on an heat-sink made of extruded aluminum. In system E a fan was added to components of system D. In system F heat pipes with the aluminum heat-sink are used. In system G there are heat pipes with the aluminum heat-sink cooperates and two fans in the push-pull configuration. System H includes a liquid cooling system.

The junction temperature of both transistors (T_{j1} and T_{j2}) and the case temperature T_{C1} of the tested transistors operating in the mentioned cooling systems were measured. The measurements were carried out for different values of the power dissipated in the tested transistors and different values of the air flow velocity in the considered cooling systems.

As an example, Fig. 1 illustrates the dependence of the considered temperatures on the power dissipated in transistor T_1 for the tested transistors operating in system B.
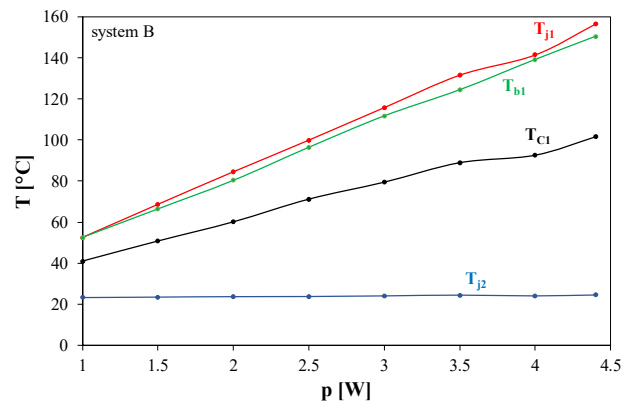
Fig. 1. Measured dependences of the junction and case temperatures of the transistors on the power dissipated in transistor T_1 operating in system B

The values of the temperature of the base of the case T_{b1} of transistor T_1 measured with the optical method are slightly lower than the junction temperature T_{j1} measured with the electrical method. The difference between them does not exceed 4 ºC at power p = 4.4 W. It means the thermal resistance between the junction and the base of the case R_{thj-b} = 0.9 K/W. In turn, the plastic part of the case T_{C1} has the temperature even 60 °C lower than the temperature T_{j1}. This means the thermal resistance between the junction and the case R_{thj-c} = 13 K/W. Temperature T_{j2} is practically constant, which corresponds to the zero value of mutual thermal resistance between the transistors.

Of course, the use of different cooling systems allowed the tested transistor to operate at different maximum values of the power dissipated. According to the classic model of heat transport in semiconductor devices, the temperature of its junction is always higher than the temperature of the case. However, it was observed that these differences can reach even 30ºC with low values of the power dissipated in the tested transistor. In particular, it is worth pointing out that the temperature of the metal base of the case is very close to the junction temperature when the tested transistor operates without any heat-sink. This is due to the fact that R_{thj-b} is much lower than R_{thj-a} characterizing the heat flow from the semiconductor chip to the surroundings.

By taking into account the presented research conclusions, it will be possible to more accurately monitor the properties of these devices in specific operating conditions.

Signal Processing

A Comprehensive Study of Optical Character Recognition

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Abstract—In recent decades recognition of characters has become a most important research topic for computer vision researchers or scientists. One of the major techniques for character recognition is optical character recognition (OCR) which plays a vital role in recent years in the development of various methodologies for the recognition of characters of several languages alphabets. Currently, OCR technology is utilized by most of the applications of scanning documents and makes them readable for the users such as google translate, which has been developed for translating the language from one language to the other language. But the rate of accuracy and timing to perform the specified task is still a problem. This paper presents a brief description of the OCR technology, the timeline of its development, some major applications of this technology, and its future perspective in our daily life. Moreover, this article provides an overview of this fascinating research topic for the early-stage researchers of computer vision.

Keywords—OCR; Artificial Intelligence; Computer Vision; Pattern Recognition; Character Recognition.

I. INTRODUCTION

Optical character recognition is the mechanical or electronics transformation of images of handwritten, printed, and typed text into the text of machine-encoded type whether from a photocopy of the document, a scene-photo, a scanned document, or from a subtitle text which has been written on any image. It is mostly used as a data entry operator from typed, printed, and handwritten paper data records such as bank statements, business cards, mail, computerized receipts, static-data printouts, invoices, passport documents, or any other suitable documentation which is a common technique of digitizing printed, handwritten, or typed texts so that they might be electronically stored more compactly, searched, displayed online, edited, and utilized in the processes of machine such as text to speech extraction, machine translation, key data, cognitive computing, and text mining [1]. OCR technology is an area of research in artificial intelligence, machine learning, pattern recognition, and computer vision.

II. MAJOR STAGES OF OCR TECHNOLOGY

OCR technique performs the recognition by following the steps such as preprocessing, segmentation, feature extraction, classification, and post-processing respectively [2]. This technique is very helpful to digitized into readable-text for machine across multiple language from huge number of datasets for paper-based documents, which will make machine eligible to store huge dataset. Fig. 1 demonstrates every step taken by the OCR to perform their recognition tasks.
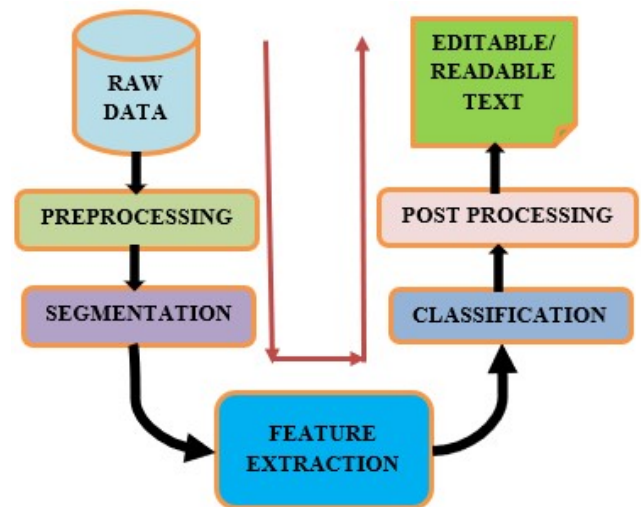
Fig. 1. Process of recognition by OCR technology

III. CONCLUSION

This paper is providing important and deeper insights about OCR technology to the researchers or technologists who are going to start their careers in the fields of computer vision, machine learning, artificial intelligence, and deep learning. A wide range of literature survey on the development of this technique and some major applications of this technique has been discussed in this paper. The major issues related to OCR are the rate of accuracy and time of operation, which means accuracy should be higher and time of operation should be lesser. This article provides the principle of working of OCR technology and future perspectives of this technique have been also provided. Further research is required which should be focused on the rate of accuracy and time by mostly focused on the quality of data.

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Analog Quadrature Modulator and Coupling Circuit for Narrowband Power Line Communication

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Abstract—**An analog quadrature modulator-demodulator for narrowband power line communication (PLC) together with an adaptive grid coupler have been developed. They have been integrated in a PLC communication device and tested both in a laboratory benchmark and in a real channel. Bit error rates low enough for transmission speeds of up to 14400 b/s were achieved. The proposed solution has the advantages of low cost, limited microcontroller load as well as high versatility with respect to the modulation used and transmission parameters.**

Keywords—**narrowband power line communication; modulator-demodulator; grid coupler; analog circuits**

I. INTRODUCTION

Power line communication (PLC) is attractive in that it uses an existing transmission medium. However, the latter exhibits low impedance, high attenuation and high noise levels which all depend on frequency, environment and time. Therefore, a communication modem should have adaptive features.

II. SOLUTION PROPOSED

The advantage of quadrature modulators/demodulators (QMDs) is the possibility of implementing any digital modulation scheme without requiring high speed digital signal processing. QMD integrated circuits (ICs) are only available for radio communication while PLC transceiver ICs offer limited adjustment options and provide little or no information on channel parameters. Therefore, an own QMD was designed (Fig. 1), where the I and Q data signals are multiplied with an analog mixer. The quadrature carriers are generated with a microcontroller using a timer and then filtered. The coupling circuit with access impedance adaptation is based on a transformer with switched primary windings and its optimum impedance range is 0.38 Ω to 6.2 Ω.
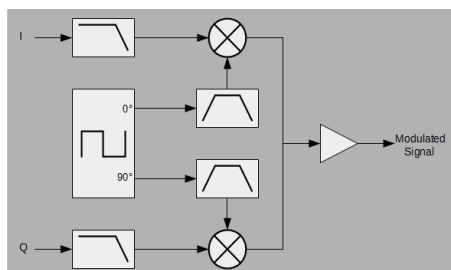
Fig. 1. Block diagram of the quadrature modulator

III. TESTS

Bit Error Rate (BER) versus the Signal-to-Noise Ratio (SNR) characteristics measured were compared against those obtained by simulation for an ideal modem employing the differential quadrature phase shift keying (DQPSK). They matched up to an SNR of 10 dB. At higher SNR, a residual BER is probably introduced by a symbol synchronization block outside the QMD. A test was also carried out in an office location. With the most favorable carrier frequency, a minimum BER of 0.074% was obtained with DQPSK at the baud rate of 7200 bd, yielding a bit rate of 14400 b/s (Fig. 2). Such an amount of error may be corrected using a correction code. BER of less than 0.001% is possible when the binary PSK is used at the bit rate of 4800 b/s.

IV. CONCLUSIONS

If the carrier frequency is properly selected, bit error rates are sufficiently low. Thanks to the use of an analog multiplier, the proposed solution has a low cost and limited requirements for the microcontroller. Its versatility makes it easy to implement PLC systems where any transmission parameters are adjusted to the momentary parameters of the highly varying medium. Both laboratory and real channel measurements have proven that such adjustments are a necessity in narrowband PLC to use the transmission medium efficiently.
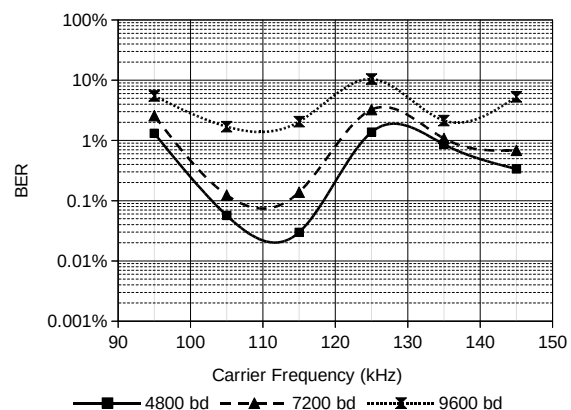
Fig. 2. BER measured in an office environment for various carrier frequencies and baud rates

Data Analysis and Mining
Using Logical Synthesis Methods

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I. Abstract

The article describes the possibilities of using selected logical synthesis methods in data mining processes.

The data mining process is about extracting meaningful data from data systems that have enormous amounts of it. This allows the creation of information systems. Depending on the quality of information, the direct result of which is the correct selection of data, information systems with greater or less substantial substantive value are created. Having information allows for inference or decision making. The information is used to create knowledge bases enabling the automation of decision-making processes.

Logical synthesis is one of the ways to explore data. Its basic methods are argument reduction and functional decomposition. The literature describes many algorithms for reducing attributes (data selection). Most of them concern fully defined binary data systems. The paper presents an algorithm for the reduction of attributes based on the division calculus, which enables the analysis of systems built on multivalued data. By using the definition of r-partition, it also includes systems containing indeterminacy. A comparison of the effectiveness of the popular Rough Set Exploration System RSES software with the attribute reduction algorithm based on the division calculus is presented. For the extended KAZ function consisting of 21 attributes, the same result was obtained in both cases. However, the results when analyzed with the RSES software were obtained within 39 minutes, while using the above-mentioned algorithm - within 2.5 seconds. Comparing the "Trains logistic database" the algorithm generated 689 reducts, while the RSES software (for the "Don't discern with missing values" option) only 333. With the "Don't discern with missing values" option, RSES was unable to perform the calculations.

The purpose of the rules induction is to enable the decision system to make a decision in the event of a new case emerging, defined by a new combination of attribute values. The article aims to discuss the methods that can be used to search for decision rules that meet the user's needs.

II. Summary

Data mining enables solving classification problems, that is, discovering the relationships between attribute values and object classes that exist in a collection to determine a predicted decision for a new case. Decision support is an essential task of data mining. However, it is worth emphasizing, that the generalization of knowledge (information) represented in huge databases may be hampered by unnecessary (redundant) information. In such situations, information redundancy processes can help. The degree of indeterminacy, and the number of attributes describing reality, require the use of formalized methods of logical synthesis. Only such procedures can meet the challenges of extracting the right data from a mass of unnecessary data. The ideal method that allows simplifying the decision-making system is the method known as attribute reduction [1] from the point of view of the minimum set of attributes that retain the classification ability of the system. The review of data classification systems shows that the attribute reduction algorithms used in them are ineffective. This assumption is confirmed by the experiments carried out with the well-known and commonly used Rough Set Exploration System RSES. It has been shown that this system cannot cope with data arrays with a large number of unspecified attributes. Apart from classification accuracy in a rapidly changing environment, decision time is a very important factor. Research shows that the attribute reduction algorithm using the division calculus is a very effective solution for classifying data in terms of time and quality.

It is worth emphasizing that the methods presented in the article are universal, as they can be successfully used in "hardware" issues related to equally or more important applications in the so-called index generation functions [2].

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Different Techniques for Human Activity Recognition

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Abstract—**Human activity recognition (HAR) in live videos has become an essential and important research topic in computer vision. RHA is widely used in different fields such as healthcare, robot learning, intelligent surveillance system, human-computer interactions (HCI), and many more. Recognition of activities in live or normal videos includes a huge amount of data are required to be processed that is why it is a tough task. In recent decades, researchers have developed various models using artificial intelligence and especially deep learning (DL) with multiple input sensor paradigms. This paper provides a comprehensive review of recent models of deep learning for HAR based on input sensor paradigm, dataset, feature extraction from the dataset, preprocessing of data, classification of input data, and accuracy.**

Keywords—**Deep Learning; Artificial Intelligence; CNN; SVM; Human Activity Recognition.**

I. Introduction

Recognition of human activity is a type of pattern recognition task which learns to identify different physical activities of human gathered by multiple sensor paradigm. The areas of application include surveillance-based security, human behavior analysis, context-aware computing, and ambient assistive living [1]. Although various research is going on in HAR, yet it is an interesting and important topic of study and research because of several difficult problems such as viewpoint of camera, variable conditions of lightening, variations of viewpoint, jumbled backgrounds, varied shapes and size of human, and occlusion [2]. HAR is a basic technique famous in surveillance and healthcare domains. Generally, HAR based on sensor signal of wearable physical type has been widely implemented to predominant applications and extremely changed our society, thanks to its very powerful resistance to the variation in environment without remarkably violating the privacy of individual [3].

II. Deep Learning Model of Human Activity Recognition

Model of a deep learning algorithm for the recognition of human activities has mainly five steps which are data acquisition, preprocessing of data, segmentation of data, feature extraction, and classification or recognition respectively. Fig. 1 illustrates the deep learning model for the recognition of human activities. This is a complete flow-chart of working principle of DL- methodology.

III. Conclusion

This paper presents an overview of different approaches of recognition of human activity based on deep learning methodology. Various programming framework such as
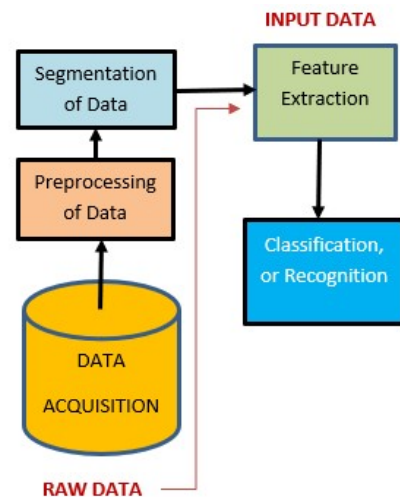

Fig. 1. Deep learning model of activity recognition

PyTorch, TensorFlow, Keras, etc. utilized for deep learning modeling has been also discussed in detail. An introductory approach for several source of data and future research prospective of human activity recognition has been discussed too. We have presented the major research carried out in this field in last decade through literature survey. This short survey of HAR will provide an overview to the researchers and technologists who are going to start their career in this field. Application of HAR technique in different area and deep learning model for this technique has been discussed in this survey. This review provides an insight that for the recognition of human activity a huge number of datasets is required. Deep learning approach is the best one for the activity recognition.

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Model of Two Current-Source-Coupled Resonant Circuits with Chaotic Behavior

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EXTENDED ABSTRACT

Chaotic systems are a subset of dynamic systems that exhibit behavior known as deterministic chaos. There is no random element in their mathematical description, but their behaviour is unpredictable. Chaotic behavior can be found in many areas of human research. A large chapter is chaos in electronic systems, with which it is even possible to model systems specified only by their mathematical description. Existence of robust strange attrac- tors has been observed in traditional harmonic oscillators, such as Collpits [1], in filter structures as KHN filter [2] and many others.

This paper deals with hypothetic construction of two resonant circuits which are coupled by controllable current sources with nonlinear transconductance. Analyzed system, based on cross-coupled transistor pair circuit, can be described by four differential equations

$$C_1 \frac{dv_1}{dt} = -i_{L1} + \hat{a}v_2^3 + \hat{b}v_2, \qquad L_1 \frac{di_{L1}}{dt} = v_1,$$
$$C_2 \frac{dv_2}{dt} = -i_{L2} + \tilde{a}v_1^3 + \tilde{b}v_1, \qquad L_2 \frac{di_{L2}}{dt} = v_2 \qquad (1)$$

where $\hat{a}$, $\tilde{a}$, $\hat{b}$ and $\tilde{b}$ are adjustable parameters and state vector is $x = (v_1, i_{L1}, v_2, i_{L2})^T$. This system was subjected to numerical analysis, which confirmed chaotic behaviour using structurally stable attractors (fig. 1) and also Lyapunov exponents analysis (fig. 2). Subsequently, a circuit based on integrator synthesis was built to simulate mathematical model 1. The oscilloscope screenshots (fig. 3) shows that in the continuous time the system generates strange attractors with dense non-periodic orbits.

ACKNOWLEDGMENT

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(a) (b)
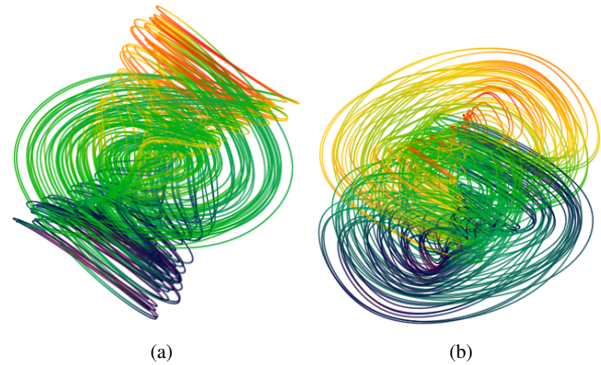
Fig. 1. Typical strange attractor generated by nonlinearly coupled resonant circuits, different 3D projections:
a) v_1-i_{L1}-v_2, b) v_1-i_{L1}-i_{L2}

(a) (b)
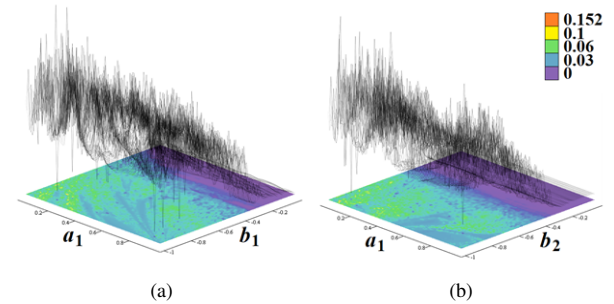
Fig. 2. Rainbow-scaled surface-contour plots of the largest LE as two-dimensional function of coefficients of cubic polynomials: a) $\hat{a}$-$\hat{b}$, b) $\hat{a}$-$\tilde{b}$

(a) (b)
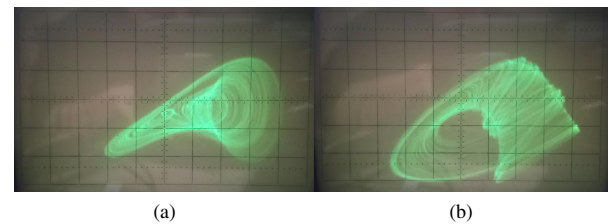
Fig. 3. Plane projection from experimental measurement with oscilloscope:
a) v_a-v_b, b) v_a-v_c

Embedded Systems

Adaptive Resonance Control
Based on the ANC-VSS-LMS Algorithm
for Microphonics Compensation

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Abstract—**This paper proposes an optimal variable step-size least mean square active noise controller to compensate for microphonics effects in the cavities. Microphonics is a prominent vibration source in the resonant frequency when operating cavities operate in continuous wave mode. The microphonics increases the required RF power-reserve and the amplitude, and phase-jitter of the accelerated electron beam. Therefore highly useful to control and identify microphonics. Convergence rate, tacking ability, and low computational complexity are important parameters for the performance of adaptive algorithms. The proposed method presents a high convergence rate and low computational complexity in the shortest amount of time. The proposed method is implemented on the SIS8300-KU board. The top module occupies the FPGA resources of 4.69% LUT, 3.46% FF, and 2.29% DSP.**

Keywords—**ANC-VSS-LMS; Microphonics; CW Mode.**

I. COMPENSATION METHOD OF THE MICROPHONICS DETUNING

The Active Noise Controller with VSS-LMS algorithm is implemented on Vivado software, to compensate and identify the cavity resonance frequency changes induced by the microphonics. The new VSS module comprises three components, namely: 1. Adaptive filter component, 2. Weight-computation component, and 3. Step-size update component. Each component includes some FPGA modules, the first module is the FIFO module to save the microphonics samples. In the next module, the output of the decimator is transferred to the hamming window that suppresses spurious frequencies due to discontinuity in the data of the FIFO module. The hamming window is implemented for suppressing spurious frequencies due to discontinuity on the samples and operates such as a low pass filter. The FFT module detects the frequency of the signal and the Max_Finder module is designed to determine the maximum amplitude of the microphonics signals. The sin_gen_dds modules generate the sine and cosine signals with the same frequency as the microphonics signal and transfer them to each LMS block to identify and estimate the coefficients based on the microphonics changes and generate the controller output.

II. HARDWARE IMPLEMENTATION

The implementation purposes are 1. Based on the maximum amplitudes, the FFT block estimates the specified frequency with high accuracy. 2. To improve the tracking ability of the microphonics effects in the cavity with less computational complexity. 3. To adapt the weights and step size algorithm based on the microphonics changes and compensate for the microphonics in the cavity. In Fig.1, the recognized frequencies of the microphonics are 4, 35, and 66 Hz signals. The error signal, that is difference between measured microphonics and the sum of the LMS outputs, convergences to the minimum value. Therefore the proposed algorithm can track the microphonics changes with a high convergence rate and tracking ability. The proposed algorithm is implemented on the SIS8300-KU board. The FPGA-based hardware resource utilization is listed in Table I. The proposed method presents a high convergence rate and low computational complexity in the shortest amount of time. The proposed method is implemented on the SIS8300-KU board.
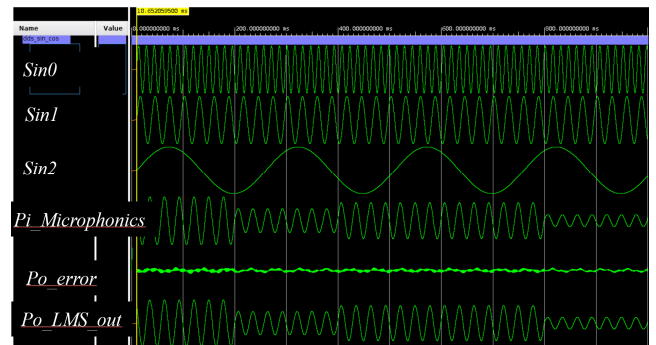

Fig.1 The output signals of ANC Module

TABLE I.
FPGA RESOURCES

Module	LUT	FF	DSP
Top module	11365(4.69%)	16773(3.46%)	44(2.29%)
ANC	676(0.27%)	1168(0.24%)	6(0.31%)

Analysis of Photovoltaics Performance Under Variable Conditions

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EXTENDED ABSTRACT

The basic foundation for obtaining maximum power is reaching the maximum operating point (Maximum Power Point), which makes it the highest possible power produced by the panel in the given irradiance and temperature conditions. Achieving this power requires adjusting the voltage in the work cycle, which unfortunately requires a kind of "search" by "sampling" the value of the instantaneous power at a given voltage. However, it takes a certain time to reach the maximum power, which implies power losses. Another aspect to consider here is the power loss associated with rising temperature (Maximum Power Point shifts towards lower values). Therefore, these two aspects constitute the theme of this work.

The basic foundation for obtaining maximum power is reaching the maximum operating point (Maximum Power Point), which makes it the highest possible power produced by the panel in the given solar and temperature conditions. Achieving this power requires adjusting the voltage in the work cycle, which unfortunately requires a kind of "search" by "sampling" the value of the instantaneous power at a given voltage. However, it takes a certain time to reach the maximum power, which implies power losses. Another aspect to consider here is the power loss associated with rising temperature (Max

Power Point shifts towards lower values). Therefore, these two aspects constitute the theme of this work (in fig. 1. temperature dependency I-V plots are presented). The aim and scope of the work includes the analysis of the optimal solution of the photovoltaic system with the use of available market solutions. The solution analysis was performed on the basis of simulations carried out using the Matlab / SIMULINK software package and the created model of a photovoltaic installation. On the basis of the available databases, the analysis of the existing photovoltaic module (monocrystalline, polycrystalline, with particular emphasis on the bifacial type) was also performed in terms of the Temperature Power Factor, which determines the amount of power losses with a unit temperature increase. Here, 335W Panel was analyzed.

It is quite clearly visible that the current flowing from the PV to the receivers (loads) is strongly conditioned by the temperature of the p-n junction (T_j), appearing mainly in the exponential component of the above dependence. It can be seen, therefore, that this is quite an important aspect that should be taken into account not only at the stage of production of panels, but also at the stage of their operation.

Fig. 2 shows the simulation results of the 335W panel as a function of irradiance and temperature using the constant step in the MPPT algorithm (here P&O has been applied). Each graph represents a simulation for a different temperature (blue graph for 25°C, red for 50°C and green for 75°C).
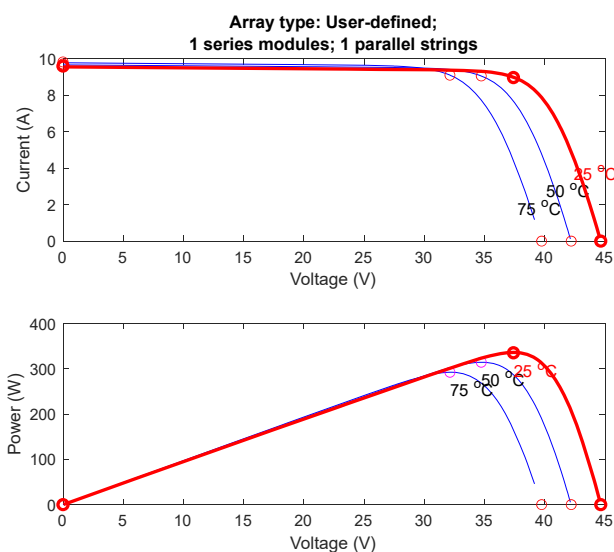

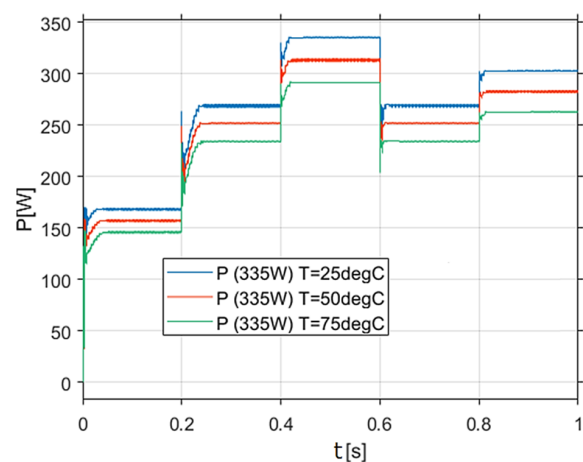Fig. 1. I-V, P-V characteristics for RSM 335W module for different temperature.

Fig. 2. Results of simulations RSM 335W module.

Evaluation of Embedded Devices for Real-Time Video Lane Detection

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EXTENDED ABSTRACT

This paper presents a comparison of the performance of embedded systems processing video sequences in real time. As part of the work, practical programs for detecting lanes located on airport areas, which allow autonomous service vehicles to move around the airport, were tested. The following modules were used during the tests: Raspberry Pi 4B, NVIDIA Jetson Nano, NVIDIA Jetson Xavier AGX. For modules from the NVIDIA Jetson family, the maximum performance of video stream processing (FPS) depending on the resolution and the selected power mode has been checked. The results of the experiment show that NVIDIA Jetson modules have sufficient computing resources to effectively track lines based on the camera image, even in low power modes.

The input training video sequences to the system were obtained from the GoPro Hero+ camera at Poznań - Ławica Airport. The data collected in this way were processed by an embedded system in order to receive optimal track by line detection and road markings located on airport runway and taxiways.

The aim of the experiment was to segment the lines along the airport runway to determine the correct path. Used video sequences show the airport areas with horizontal markings. Our dataset consists of video recordings of 3 hours 33 min. prepared in H264 encoding, resolution 1920×1080 and 60 FPS. Tests were made on 10-second fragments, selected randomly from among 1,278 parts into which the entire recording recorded at the airport was divided.

Two types of algorithms for line detection were investigated. The assumption of the Algorithm 1 was to extract a range of shades of line colors from the image, which in the case of airport markings are white or yellow. The isolation of yellow and white areas from the image was preceded by changing the resolution and color space from RGB to HSV and appropriate saturation thresholds and the component being the power of white light were also set. This results in a mask where the detected colors are pixels with a value of 255, i.e. they are white, and the rest of the frame has a value of 0, i.e. black. Such a data array is used as an input to the Canny algorithm for edge detection. In the final step Hough algorithm finds lines in the image.

The Algorithm 2 is similar to Algorithm 1 and use Canny and Hough transforms, but has no implemented color space change and filtering due to the color of the objects. However, it is additionally equipped with the filtering of the detected edges in terms of their orientation using a Scharr mask for an angle of 0 degrees. This program demonstrates similar effectiveness but exhibits greater computational complexity.

The Algorithm 1, due to its lower computational complexity, is characterized by shorter processing times than the Algorithm 2. The duration processing time of program increases with the higher input resolution. Raspberry Pi 4B microcomputer allowed to achieve almost identical results as in the case of the NVIDIA Jetson Nano module in the limited 5W power mode. When using the MAXN mode for NVIDIA Jetson Xavier AGX, a value of about 64 FPS was obtained. In this case, each NVIDIA Jetson Xavier AGX operating mode will also allow real mode operation, even for 10W mode.

The computational complexity of the Algorithm 2 demonstrates the increase in input processing time in embedded systems. The obtained FPS number depends on the resolution and the selected power mode. are corresponding to the observations from the analysis of Algorithm 1. The efficiency of Algorithm 2, due to the greater computational complexity, causes that the maximum performance of the tested embedded devices, including the GoPro Hero + camera, is worse than in the case of Algorithm 1 and will not be equally usable in real-time work. It can be also observed that processing speed is lower in comparison to Algorithm 1, but this decreasing is not always proportional in corresponding power modes.

An advantage of NVIDIA Jetson Xavier solutions is the ability to select various operating modes. This allows to optimize energy consumption, and at the same time obtain the required computing performance, which was confirmed by tests for practical solutions used in the measurement platform. The experiments carried out clearly show that the operations performed by NVIDIA Jetson Nano and NVIDIA Jetson Xavier AGX are faster not only in terms of neural networks, but also in the area of classical image processing.

It is worth noting that the use of the full potential of NVIDIA Jetson Nano and NVIDIA Jetson Xavier AGX is possible for tasks carried out with the use of machine learning, which requires the use of specific libraries supporting CUDA and adapted code that supports multithreaded work.

Experimental Verification of the Required Power for Electrically Heated Clothing

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Abstract—**Experimental verification of the power required for thermal comfort in electrically heated clothing is presented. The clothing consists of a jumpsuit with embedded woven heating insets, controlled by a dedicated microprocessor system. The user is able to set heating power using a smartphone app. The experiments, conducted in a mobile freezing chamber, aimed at verification of the theoretical power (according to ISO 11079) required to maintain thermal comfort in ambient temperatures below 0 °C. The results are important as they impact the construction of heating insets, power electronics driving the heating insets, and the power rating of the battery.**

Keywords—**actively heated clothing; thermal comfort; automatic control**

I. INTRODUCTION

When designing electrically heated clothing it is crucial to match the heating power with the passive insulation value of clothing and the desired range of external temperatures. ISO 11079 presents one of the possible approaches towards this goal. However, experimental verification in controlled environment is important. This paper reports results of such verification.

II. MATERIALS AND METHODS

A. ISO 11079 standard

This standard is applicable for cold environments. It enables calculation of the clothing insulation required for thermal balance and thermal comfort, based on: Air temperature, Mean radiant temperature, Wind speed, Metabolic rate and Thermal insulation of clothing.

B. Electrically Heated Clothing

The ultimate objective of the research is to develop a set of professional-use clothing, consisting of a windproof Gore-Tex jacket, windproof trousers and an inner jumpsuit with integrated electrical heating elements. The total power of the insets available in the tested version of the clothing prototype was 100 W. The control over the heating insets is possible thanks to a solution consisting of a dedicated embedded system and an application, running on a smartphone.

C. Experiment

In the experiment participants entered the freezing chamber and were asked to adjust heating levels of the insets so that thermal comfort was achieved (or report that it was not possible to achieve such) via smartphone application. The participants remained stationary at all times. The experiment allowed to compare the electrical power required for comfort with the power computed from the standard.

III. RESULTS

Outline of the results is presented in Table 1.

TABLE I.
ISO 11079 VS. EXPERIMENTAL RESULTS.

Parameter	Participant		
	A	*B*	*C*
Theoretical power	**128.66 W**	**81.22 W**	**104.81 W**
Experimental power	**59.99 W**	**48.55 W**	**42.85 W**

There is a big discrepancy between the required power computed using the ISO 11079 standard and the values obtained experimentally. Consequently, caution should be taken when designing heated garments, as relying solely on standards may lead to oversizing of the heating system, while subjective responses of thermal comfort may be falsified by several factors, in turn resulting in undersized system.

Firmware Update for Improved Reliability Embedded Systems

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Abstract—**Embedded systems become more and more complex, and this is also a case for their software. For this reason, there is an increased demand for software updates and data compression to decrease the application download time.**

The purpose of this paper is to compare the compression algorithms in terms of their use for firmware updates in the Micro Telecommunications Computing Architecture (MicroTCA) system for the Advanced Mezzanine Card (AMC) board. To reduce the firmware upload time for Module Management Controller (MMC) a literature review was conducted. Selected lossless data compression algorithms were tested. The implemented solution is compatible with Hardware Platform Management version 1 (HPM.1) standard. Initial results of firmware upgrade performance and challenges faced during the design are presented in this paper.

Keywords—**Data Compression; Firmware Update; Firmware Upload; Intelligent Platform Management Interface, MicroTCA; Advanced Mezzanine Card; Module Management Controller**

EXTENDED ABSTRACT

Modern control systems used in large-scale projects like International Thermonuclear Experimental Reactor (ITER) are designed with use the of programmable devices such as Microcontrollers (MCUs) or Field Programmable Gate Arrays (FPGAs). The firmware is usually held in non-volatile Read-Only Memory (ROM), Electrically Erasable Programmable Read-Only Memory (EEPROM) or flash memory. Changing the firmware of a device manually may rarely or never be done during its lifetime. Common reasons for updating firmware include fixing bugs or adding additional features to the device. Tools for the firmware replacement are provided by the manufacturer. Those tools allow to download the firmware to a non-volatile memory and provide debugging functionality. The debuggers can be connected using a standard Serial Wire Debug (SWD), Joint Test Action Group (JTAG) or proprietary debug connectors. In the case of the Micro Telecommunications Computing Architecture (MicroTCA) which is a modular open standard for high performance switched, fabric computer systems in a small form factor [1], many Advanced Mezzanine Cards (AMCs) can be connected directly to a backplane. At the same time, they require several different tools to program and debug. During development, when the MicroTCA crate is in laboratory, each device is programmed and debugged via the dedicated programmer. Programming and debugging become more difficult when MicroTCA is a part of a more complex and remote system where physical access is hindered. Firmware update with use of a dedicated programmer is no longer possible. The need for a remote and automated firmware update and verification is required for the continued development and software maintenance.

The proposed method of firmware update is based on the Intelligent Platform Management Interface (IPMI) standard and Hardware Platform Management (HPM) firmware upgrade specification which describes the firmware upgrade procedure. It is worth noting that there are newer versions of HPM that allow the use of the faster data transmission protocol - IPMI over Local Area Network (LAN) [2]. MicroTCA imposes an Inter-Integrated Circuit (I^2C) interface for management purposes, so the HPM.1 standard must be applied. The size of flash memory that contains code and/or data in MCUs increases. In the beginning, the size used by MMC (Module Management Controller) was between 32 and 64 kB in case of ATxmega microcontroller [3]. Currently it is 512 kB and is still rising. Due to that, the time required for firmware upgrade also increases. The long-time of the firmware upload (ca. 15 minutes) implies usage of lossless compression algorithms. According to HPM.1 specification, the structure of the system requires designing a software that makes updating a product's firmware in the field possible (bootloader) with two applications that serve as a revision of the loaded software.

The paper will compare and debate various lossless data compression methods suitable for Programmable System-on-Chip version 6 microcontroller in terms of low hardware resources such as processor computing power, program, size of volatile and non-volatile memory. The design and practical implementation of bootloader, including uploading firmware, implementation of an error-detecting function Cyclic Redundancy Check (CRC) and the full set of HPM.1 commands including rollback support for MicroTCA.4 applications will be discussed. The implemented solution is compatible with Hardware Platform Management version 1 (HPM.1) standard. Initial results of firmware upgrade performance, challenges and problems faced during the design and updating firmware are presented in this paper.

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Memory Protection with Dynamic Authentication Trees

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EXTENDED ABSTRACT

Embedded devices that process sensitive data and provide essential services have become increasingly common as modern digital infrastructures have grown at a rapid pace. This raises security concerns as there are more reasons than ever for a malicious party to try to exploit these systems. In an attempt to provide security, encryption methods are oftentimes applied to any sensitive data to provide confidentiality. However, data confidentiality itself is not enough to fully protect a system from an attacker. For example, erroneous data may be injected into the system in an attempt to disrupt the normal functionality of the device. In order to protect against such attacks, it is necessary to verify that any data the device processes is provided by the expected source. In addition, there needs to be a method of ensuring that the data has not been tampered with. Methods of authentication are then used to confirm the integrity of data processed in the system. Existing authentication methods, such as hashes and message authentication codes (MACs), are able to provide the intended protection; however, some of these methods are costly in terms of the device resources and performance overhead required to implement them. In this paper we present a new method of dynamic authentication trees, which update a tree structure based on a processor's memory access patterns. The key features of the approach are as follows:

- *Authentication:* Modified block-level added redundancy explicit authentication (block-level AREA) scheme is employed in our ordered Dynamic Authentication Tree (DAT) method. Utilizing this approach has the benefit of providing encryption inherently with the authentication operations.
- *Tree Structure:* The structure of the tree depends on the weighted frequency of accesses to each data node.
- *Tree Nodes:* The leaf nodes of the authentication tree structure contain the data blocks that are directly protected by the tree. These nodes are referred to as data nodes, and are separated into two parts: the data that is being protected and the nonce. The nonce contains the tree metadata required for tree traversal and a count of the number of times the node has been accessed.
- *FPGA Design:* An AXI-4 based framework is developed as a transparent and highly customizable memory controller. This design is then synthesized onto an FPGA and verified.
- While this design is motivated by vulnerabilities in embedded systems, the method presented is scalable and may be applied to any computing system. Different configuration options are provided allowing for the design to be used in applications with different restraints and requirements.
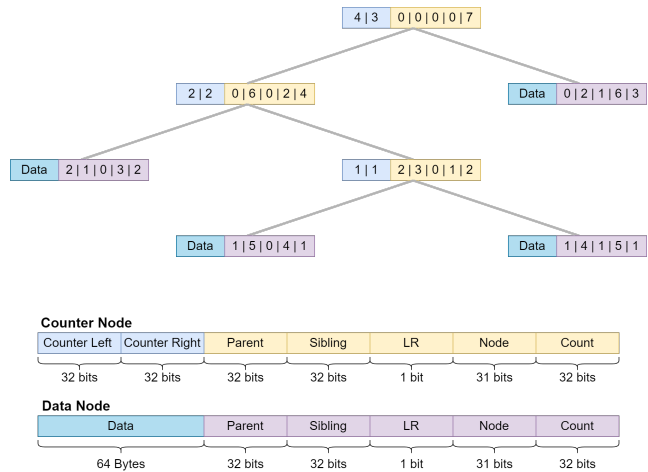

Fig. 1. Ordered Dynamic Authentication Tree

Parameter Efficiency Testing
for an Intrusion Detection System Inspired
by the Human Immune System

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I. Introduction

In a series of papers, we proposed an intrusion detection system (IDS) based on the negative selection algorithm. The IDS proposed by us monitors a specified folder in the operating system. Initially, a set of receptors is generated for each of the files in the folder. Receptors are binary strings that are used to detect e.g. malware patterns injected into the programs. The monitoring process involves the scanning all of the files in the folder periodically in search for anomalies. The scanning process relies on the receptor set that was generated initially after running the solution. In a previous paper, we raised a question of future research of testing various receptor sizes in the IDS. In this paper, which is meant to be a follow-up to that question, we explore various combinations of receptor size and other related parameters.

II. The Proposed IDS

The IDS is a set of algorithms bound by a control unit that allows to monitor a specific location in an environment (e.g. operating system) for anomalies (modifications of software or firmware, or infections). A general diagram of the IDS is shown in Fig. 1. The system utilizes a control block to control the receptor generation block and the anomaly detection block. Once generated, the receptors have the ability to detect infections in computer program files if they are used within specific formulae.

III. Testing Methodology And Results

The IDS was implemented in the C++ programming language and tested in a Microsoft Windows environment. The IDS was set up to monitor the directory C:\ids. Inside the directory, a file called *test.exe* was placed. The method selected for deployment within the IDS was the template method utilizing one set of receptors. The testing was done for the anomaly size of 4 B. The main input parameters for the testing were l, the length of the receptor in bits, and m, the activation threshold of the receptors. The tested ranges for the parameters were $l = \{16, 17, ..., 32\}$ and $m = \{8, 9, ..., 12\}$. A single test of $l = 24, m = 13$ was also conducted.

IV. Test Analysis

Out of the 86 tested combinations of l and m, 26 of them (30%) reached a detection rate of at least 95%. 8 of the results reached a perfect 100% detection rate. To pick the best combination out of the results with $\geq 95\%$ detection accuracy, we calculate their efficiency factors and select the combination that yields the highest. For this study, the best combination to use in this environment turned out to be $l = 22, m = 11$.

V. Concluding Remarks

In this paper, previous research was supplemented with a new study of the IDS parameters and their effect on the memory footprint, detection rates and efficiency of the system. For a given detection rate threshold, an efficiency rate can be calculated and, on its basis, an efficient combination of IDS input parameters can be obtained for the environment. Further research can be carried out to investigate the effect of an additional receptor set on the efficiency of the IDS.
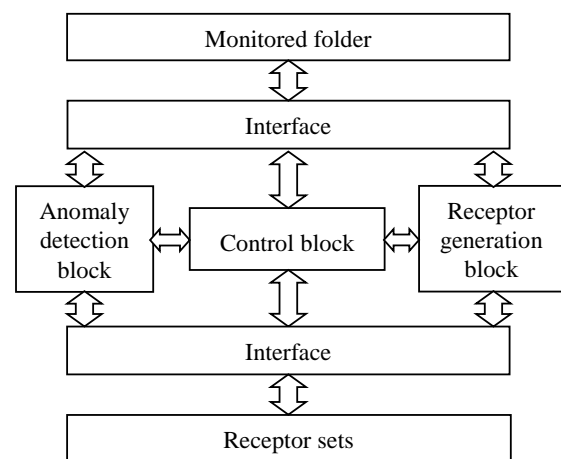

Fig. 1. A diagram of the proposed IDS.

Road Line Detection by Reflected Heat

Assistant system for car navigation

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Abstract—**This article presents a new method of navigating cars using a thermographic camera. The article describes the method of detecting road lines and road edges with the help of heat generated by a car engine and reflected from the road surface. This method may aid current ADAS systems used in car navigation.**

Keywords—**ADAS, line detection, car navigation, infrared detection**

EXTENDED ABSTRACT

Research, testing, and implementation of new driver assistance systems are currently underway. These systems support driving and are designed to ensure safer driving. The collection of safety and driver assistance systems is known collectively as ADAS - Advanced Driver Assistance System. One of its key functions is the ability to detect a road lane or the edge of the road and correct the movement of the vehicle in the event of an unintentional departure from the correct lane.

The article presents the IRHLD ("Infrared Heat Line Detection") method that enables the detection of the road shoulder and horizontal road lines separating traffic lanes for cars. The proposed method uses a thermographic camera (Fig. 1) mounted in the front of the car (IR sensor I) and under the car (IR sensor II).

Fig. 1. Arrangement of thermal sensors (IR I and IR II) in the car

The thermographic camera mounted in the front bumper (method I) uses the temperature difference measured by the sensor, resulting from the existence of temperature differences or different emissivity of the materials of which the road or shoulder surface is made Fig. 2.

The second camera (method II), mounted on the car's chassis, uses the heat generated by the car's engine, which is then reflected off the road surface Fig.3. The amount of heat that is reflected from the road surface depends on the heat reflection coefficient, which is different for different colors and materials.
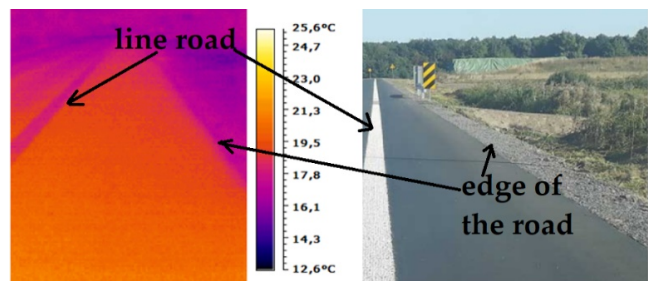

Fig. 2. Photo of road lines and roadsides during the passage of a car, taken with a thermographic camera (left) and a video camera (right)
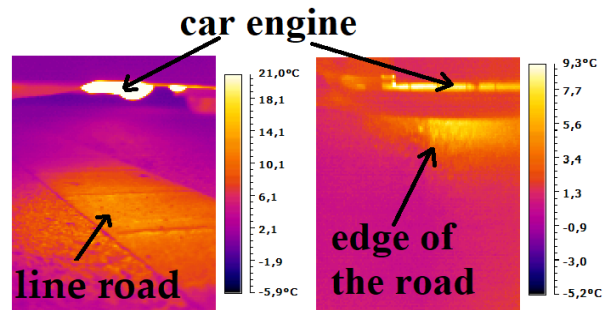

Fig. 3. A photo of the road lane (left) and edge of the road (right) during the passage of a car made with a thermographic camera.

Thanks to the detection of road lanes and roadsides, it is possible to keep the car in the correct lane and inform the driver in the event of an attempted unplanned lane change or an unplanned attempt to drive the car from the edge of the road to the shoulder. The main task of the presented method is to support the already operating line and roadside detection systems as an additional data source, as well as to use the presented method in situations where the current systems do not work properly, such as e.g. heavy rain or fog.

ACKNOWLEDGMENT

Software Solutions for Dynamic Configuration and Deployment of EPICS application for MTCA.4 Chassis Management

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EXTENDED ABSTRACT

The European Spallation Source (ESS) accelerator is a linear accelerator, based on the spallation phenomenon. It generates neutrons by hitting accelerated protons with a rotating, tungsten target. In the operational state, the accelerator will deliver long pulses lasting 2.86 ms with a repetition rate of 14 Hz. The superconducting part of the facility is composed of elliptical cavities fed with an electric field from powerful amplifiers - klystrons. For accurate accelerator functioning, it is essential to fix the amplitude and phase of this field at a given set-point.

A significant number of components of the ESS accelerator control system are designed in Micro Telecommunications Computing Architecture. (MTCA.4) standard. Most of the devices for fast data acquisition follow it. The main advantage of this architecture is its high reliability and its efficiency. It is widely used in large experiments like accelerators. For instance, the Low-Level Radio Frequency (LLRF) control system, which is responsible for monitoring and control electric field's parameters, is composed of components like Local Oscillator, Piezo Driver modules that have the form of MTCA.4 modules - Advanced Mezzanine Carriers (AMCs) and Rear Transition Modules (RTMs).

The management layer in the MTCA standard is based on IPMI. It is an intelligent protocol for managing and monitoring computer and telecommunications systems. The common control standard allows for creating tools that will facilitate the process of management. In the ESS, the control system is based on the Experimental Physics and Industrial Control System (EPICS). It is a framework destined for building distributed control systems. It uses a client/publisher mechanism to share data over its network named Channel Access (CA). As mentioned before, since many of the ESS accelerator devices (for instance LLRF components) are based on MTCA.4 standard, it is important to integrate IPMI protocol with EPICS. This will facilitate the devices' monitoring and will allow for keeping the coherence in terms of software tools.

The paper describes the software that implements the IPMI management layer with EPICS framework and encapsulates it to ESS EPICS Environment (E3) modules. The main feature of the created solution is its scalability. It means that the software can be used with any MTCA.4 crate configurations without excessive, prior modifications. It is presented how we developed the tool, what its architecture is, and how it evolved because of new requirements. We precisely show the solution based on the Input/Output Controller (IOC) that automatically detects the MTCA.4 chassis setup and configures IOC to be able to control it. It is also presented how the graphical user interface is adjusted to the MTCA.4 setup dynamically. Then, we explain why the functionalities of the created software have been moved into separate, stand-alone tools that cooperate with the IOC. In order to verify the proper functioning of the software, we have performed the tests comparing MTCA.4 status read via telnet through NAT interface with data available on the IOC level for various chassis setups. It was confirmed that the proposed tools can detect crate configuration and distribute all necessary information needed to launch an IOC and to generate engineering operator panels. In the end, we discuss current issues and future improvements.

ACKNOWLEDGMENT

Study About Navigation Systems for Autonomous Robots

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EXTENDED ABSTRACT

Technology is evolving rapidly, each year the automobile industry develops and integrates new devices into vehicles, in order to make them increasingly intelligent and capable of offering comfort, convenience and safety to their users.

The purpose of this study is to develop a low-cost mobile vehicle, using technologies such as Raspberry Pi, Arduino, inertial sensors and GPS, which is capable of autonomously performing actions such as steering and speed control.

The navigation system is based on the use of a GPS module, connected to an HKPilot32 controller board, responsible for providing data on the robot's current position, and on the MPU6050 module connected to an Arduino UNO board, which through its accelerometer and gyroscope sensors , gives the vehicle's turning angle. The information from the sensors is sent to a single-board computer, Raspberry PI 3, where the system is programmed in Python language.

The sending of some commands for system initialization or information analysis is carried out through a Control Center, which communicates with the vehicle through an Ad Roc network.

For autonomous vehicles to navigate safely, it is necessary to increase the reliability of measurements and the quality of the data provided by the sensors. Digital filters are then used, which allow performing the data fusion technique to combine information from different devices such as GPS, accelerometers, gyroscopes and magnetometers, and thus obtain more accurate and less noisy measurements.

In this work, the navigation system used in the vehicle in question, as well as all the parts that compose it, are presented in detail. The practical part of the study is addressed, detailing how everything was interconnected, objectives achieved, data obtained and final considerations.

The diagram with the connections of the elements present in the developed navigation system can be seen in Figure 1, and the vehicle assembly with all the components connected can be seen in Figure 2
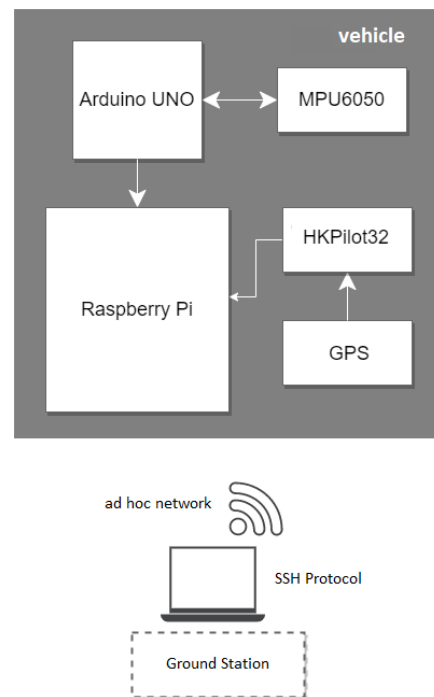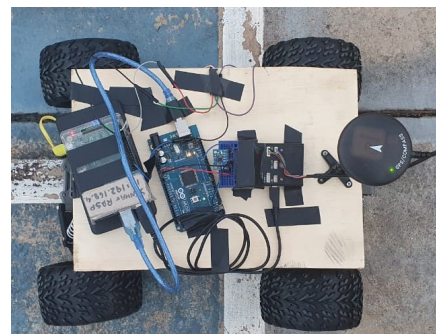
Fig. 1. Component wiring diagram.

Fig. 2. Vehicle with components connected.

Medical Applications

An Application of Dual-Q Tunable Q-factor Wavelet Transform for QRS Detection in ECG Signal

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Abstract—**Accurate localization of QRS complexes in the electrocardiographic signal is essential in clinical practice for prevention of heart disease. In this paper, we propose a new method for QRS complex detection based on the decomposition of electrocardiographic signal with dual-Q tunable Q-factor wavelet transform (Dual-Q TQWT). The proposed method starts with a preprocessing stage which consists of baseline wandering removing, and then the obtained signal is decomposed into low and high resonance components with Dual-Q TQWT. In the next stage the decomposed signal is created from the selected low resonance components. On this basis, after the non-linear mapping, the detection function waveform is derived. Applying the three-stages amplitude threshold method allows us peaks localization. These peaks correspond to locations of QRS complexes. Our approach has been evaluated over publicly available ECG signal databases.**

Extended Abstract

Cardiovascular diseases (CVDs) are the number one cause of death globally. Because of this, scientists are still working on the development and improvement of electrocardiographic signal processing methods. Any changes in the electrocardiographic (ECG) signal may be an indication of a cardiac disorder, such as the presence of a cardiac arrhythmia [1]. Therefore, it is crucial to accurately and correctly detect the location of the QRS complex. The major complication in accurate detection of the QRS complexes is the presence of noise in the ECG signal which is corrupted with different kinds of artifacts. To ensure accurate detection of QRS complexes, ECG de-noising remains one of the important problems for researchers.

In this work, the improved QRS detection method is proposed. In the first step the wandering baseline effect is removed. Then, we apply the dual-Q tunable Q-factor wavelet transform (TQWT) as the method for ECG signal denoising and decomposition. The Dual-Q TQWT was introduced in [2]. In the next step, the selected low resonance components from signal decomposition are used to compose the so-called detection function which peaks are detected with the three stage amplitude threshold based method with additional peaks slope evaluation. The main amplitude threshold is set as 20% of the estimated varying RMS of the so-called detection function.

The detection efficacy is evaluated on the basis of the following performance measures: sensitivity SEN = TP/(TP+FN)·100%, positive predictivity (precision) P^+ = TP/(TP+FP)·100% and F-measure F = (2 ·SEN·P^+)/(SEN+ P^+), where TP is the number of correctly detected QRS complexes, FN is the number of QRS complexes, which the proposed method fails to identify, and FP is the amount of detection, which are not the real QRS complexes, regardless the proposed method detects those as real QRS complexes.

The requirement of QRS complex accurate detection is one of the most important in ECG signal processing. Two wellknown annotated ECG databases are used in this study: MITBIH Arrhythmia Database (ARRDB) [3] and MIT-BIH Noise Stress Test Database (NSTDB) [3]. The obtained results are presented in Table I.

The main innovations in the proposed technique are: the application of the dual-Q TQWT for denoising and decomposition of ECG signal as well as using the RMS over the detection function for amplitude threshold estimation. Backtracking with two different values of amplitude threshold allows to increase the accuracy of detection due to possibility of detection of undetected QRS complexes in first step and eliminate those which originate from noise. The obtained results are promising, and the performance indicators are higher, or comparable, to similar studies in the scientific literature.

TABLE I
RESULTS OBTAINED FOR TWO ECG STANDARD DATABASES

ECG database	total beats	SEN(%)	P^+(%)	F(%)
ARRDB	109494	99.88	99.86	99.87
NSTDB	25590	97.87	92.79	95.26

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Enviropulmoguard ICT System for Interactive Health Monitoring – Preliminary Study

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EXTENDED ABSTRACT

Among respiratory diseases ones with obstructive spirometry pattern can be distinguished (e.g., bronchial asthma, bronchitis, cystic fibrosis). Main groups of diseases exacerbated by air pollution are cardiovascular and respiratory conditions. The air pollution is not only responsible for clinically significant worsening of symptoms in patients with already diagnosed diseases, but can also affect basic physiological parameters.

Air pollution is defined as all substances present in the air that poses a threat to health, independently of the physical or chemical structure. Air pollutants can be divided into two main groups: gaseous air pollutants and particulate matter. The gases include: O_3 (tropospheric ozone) – emitted by energy sector, transport, mining industry, NO_2 (nitrogen dioxide) - road transport, heating systems, CO (carbon monoxide) - transport, coal combustion, SO_2 (sulfur dioxide) - side effect of fossil fuel combustion.

Team of scientists working at the Institute of Medical Technology and Equipment in Zabrze have designed four sensors (piezoelectric, resistive, inductive, rheographic), special sensors band and application for mobile phone. The project is implemented under the grant POIR.04.01.04-00-0060/19. We will present preliminary results to obtained for the device, environmental sensor and portable device with a battery for measuring environmental parameters in the direct surroundings of the patient (EMP). It can be worn over the arm thanks to the built-in elastic headband or it can be placed on the desk. Measurable parameters such as: PM2.5, Temperature, Humidity, Pressure, NO_2, SO_2, Insolation and their range. In addition, sensors of environmental parameters allow you to monitor air quality, which is extremely important among patients with respiratory diseases. The mobile application was designed, was created in Xamarin, version 4.12.3.83, which is used for showing the environment and respiratory parameters to the patient. We focused on solutions that were already available by proposing a new, more innovative solution, which the transmission of signals to a smartphone application and monitoring center. The application, together with the monitoring center, enables continuous monitoring of patients' health and consultation with a doctor at any time.

The physician, through continuous monitoring, is able to verify e.g. cough attacks or other complaints on the basis of the presented records. A telephone consultation or an appointment may be necessary. In addition to these situations, a worsening of the condition can be adjusted with an appropriate dose of medication (increase of dose, change of medication or change of current medication). The physician throughout the patient's collaboration, can monitor, consult and stay in touch. As you can see, this developed system gives a lot of possibilities. It allows you to reduce the queues to specialists, - one of the main problems of the health service.

The aim of this paper is to present the preliminary data on the relationship between environmental parameters and respiratory waveform and to propose a new teleinformatic health monitoring system for people with respiratory diseases.
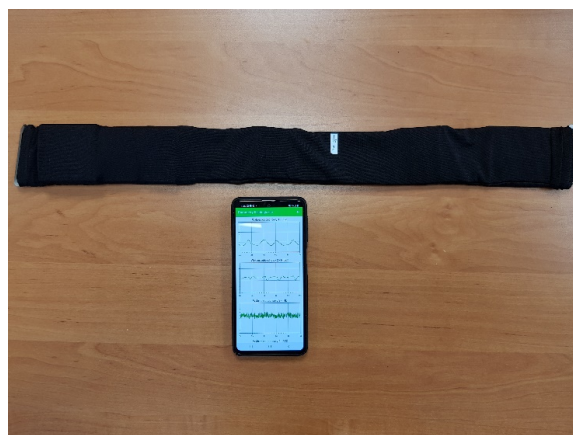

Fig. 1. Sensors band and application.

Fluid Therapy Completion Time Assessment

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I. INTRODUCTION

The course of fluid therapy is essential to patient health and safety. Too fast application of medications can lead to complications and deterioration of the patient's condition. On the other hand, too slow application of drugs unnecessarily burdens the patient. Therefore, during starting a fluid therapy, information of its expected duration plays a crucial role. Existing solutions for fluid therapy monitoring are based on optical methods, i.e. the available devices count the number of drops of applied fluid. Our motivation was to provide information about the completion time of the fluid therapy as soon as possible. Early information about the time of therapy termination seems to be crucial especially for infectious wards, where the number of contacts between medical personnel and patients should be limited. In this paper we propose a different approach to the fluid therapy monitoring problem. The proposed solution uses direct measurements of the therapeutic fluid tank.

II. COMPLETION TIME PREDICTION

Figure 1 shows an example of weight loss during fluid therapy (solid line). The gray circle marks the moment when the weight of the fluid bag reaches the desired weight, in this case 100g. The final weight is reached after a time $t_0 = 1155$s. In order to predict the time at which the fluid tank weight reaches the target value, a linear model was use. The relationship between a dependent variable (the weight) and the explanatory variable (the time) takes the following form
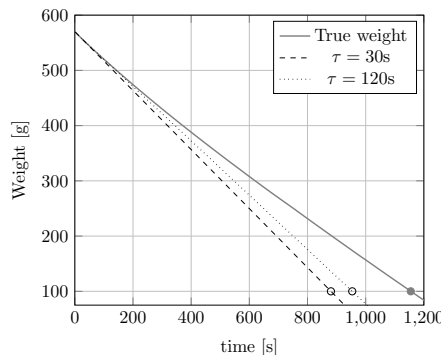

Fig. 1. Plots of container weight loss. The solid line corresponds to the true weight loss, the dashed line illustrates the regression line for $\tau = 30$s period, and the dotted line shows the regression line obtained for $\tau = 120$s period.

$$\tilde{y}_k = \beta_0 + \beta_1 t_k, \tag{1}$$

where $\tilde{y}_k$ is the predicted weight of the fluid tank after time t_k. β_0 and β_1 are the regression parameters.

Table I presents the predicted time of drip completion determined for different amount of data and for both sampling frequencies. The first column includes information about experiment number and the real completion time. The upper row shows the estimated completion time for the original signal, while the lower row contains the completion time predicted for the decimated signal.

TABLE I
ESTIMATED COMPLETION TIME IN MINUTES OF DRIP FOR DIFFERENT ESTIMATION PERIOD. TWO ROWS CORRESPOND TO A SINGLE DRIP. THE UPPER ROW INCLUDES DETERMINED TIME t_0 FOR SIGNAL SAMPLED OF 5 HZ, WHILE THE LOWER ROWS SHOWS THE PREDICTED TIME OBTAINED FROM THE DECIMATED SIGNAL.

No	$\tau = 30$ s	$\tau = 45$ s	$\tau = 60$ s	$\tau = 90$ s	$\tau = 120$ s
1	13.53	14.31	15.00	15.43	15.71
19.25	14.25	14.67	15.19	15.54	15.80
2	15.45	15.93	16.30	16.38	16.46
18.32	16.28	16.41	16.50	16.53	16.58
3	54.20	43.28	38.84	37.74	37.14
40.02	58.69	44.43	39.31	38.00	37.34
4	65.48	45.83	40.34	38.99	38.44
44.42	68.10	46.83	40.72	39.25	38.63

From the Table I, one can state that both predicted times are under estimated. This fact is caused by the model selection. During the fluid therapy, the slope of the weight curve takes the highest value at the beginning. During the infusion, for the model parameter, the initial data is still utilized. So, the model curve slope is higher than the real one resulting in underestimation of the completion time. It also can seen that the completion time estimated from the decimated signal is more accurate than the completion time estimated from the original signal. This fact is caused by the decimation process and especially by the low-pass filtering. The required bandwidth limitation of the decimated signal reduces the influence of high-frequency components on the estimation process.

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