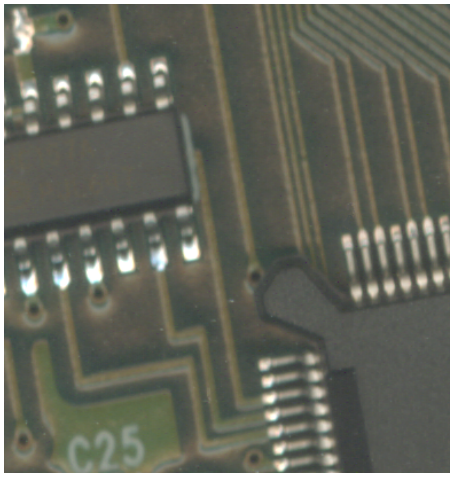
Book of Abstracts of 32nd International Conference

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

MIXDES 2025



Szczecin, Poland
June 26 – 27, 2025

Organised by:

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

in co-operation with:

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and Section of Signals, Electronic Circuits & Systems
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee
of International Union of Radio Science – URSI

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Preface

For 30 years the MIXDES Conference has been a forum devoted to recent advances in micro- and nanoelectronics design methods, modelling, simulation, testing and manufacturing technology in diverse areas including embedded systems, MEMS, sensors, actuators, power devices and biomedical applications. This year we meet together for the 32nd time in Szczecin. As this is the first conference after passing away of Prof. Andrzej Napieralski, its founder, we will be commemorating His life and achievements during a presentation given on the first day.

The program of the conference consists of two days of sessions starting each day with invited talks. The following keynote talks will be presented:

- *AI for Processors, Processors for AI: Going New Ways for Processor Architectures*
  M. Hübner (Brandenburg Univ. of Techn. Cottbus - Senftenberg, Germany)
- *Electronic Control Systems for Ion Trap Quantum Computers*
  G. Kasprowicz (Warsaw Univ. of Techn., Poland)
- *Mixed Mode: More than Analog and Digital*
  R.S. Murphy - EDS Distinguished Lecturer, R. Torres (INAOE, Mexico)
- *Modern Challenges in Hardware Design*
  M. Zmuda (Intel Technology, Poland)
- *Video-assisted Dentistry with Deep Neural Networks*
  D. Węsierski (Gdansk Univ. of Techn., Poland)

The program of MIXDES 2025 also includes two special sessions:

- *Advancing FOSS Compact Modelling: From OTF Transistors to Mott Memristors*
  organized by A. Kloes, M. Schwarz (Technische Hochschule Mittelhessen, Germany),
  W. Grabiński (GMC, Switzerland) and D. Tomaszewski (Lukasiewicz - IMiF, Warsaw, Poland)
- *Artificial Intelligence in Electronic Systems*
  organized by T. Stefański (Gdańsk Univ. of Techn., Poland) and R. Długosz (Bydgoszcz Univ. of Science and Techn., Poland)

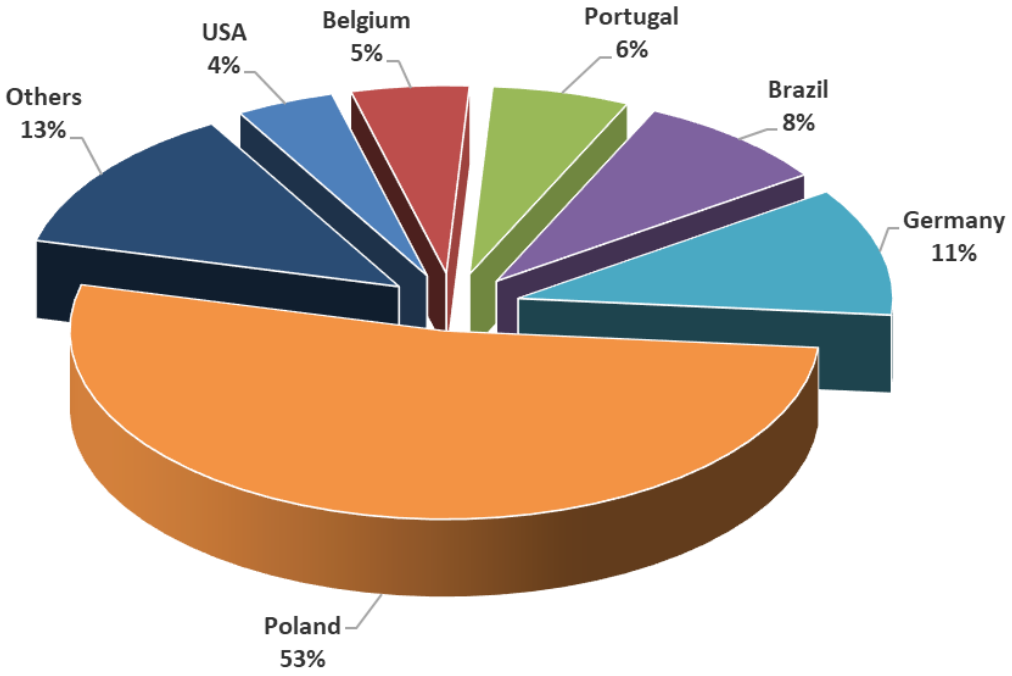
Latest editions of MIXDES Conference showed increasing interest in Artificial Intelligence topics, so starting from next year the AI topic will be included as a regular session.

All regular papers were reviewed and selected from submissions from 12 countries. The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing contributed papers.

Number of accepted papers and authors by country

Country	Number of		Country	Number of		Country	Number of	
	papers	co-authors		papers	co-authors		papers	co-authors
Belgium	2	6	Italy	1	1	Spain	1	4
Brazil	2	10	Mexico	1	2	UK	2	4
Germany	3	13	Poland	21	62	Ukraine	2	3
Iran	1	1	Portugal	2	7	USA	1	5
						Total	**41**	**118**

Number of authors by country



We hope that we will meet together next year in Poznań, June 25 – 27, 2026, one of the oldest and largest cities in western Poland.

Łódź, June 2025

Wojciech TYLMAN
Department of Microelectronics and Computer Science
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General Invited Papers

AI for Processors, Processors for AI: Going New Ways for Processor Architectures

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SUMMARY

The rapid evolution of artificial intelligence (AI) is driving a paradigm shift in processor architecture design. Traditional processors in the embedded computing domain, originally optimized for special-purpose computing but traditionally broad in their application domain, are increasingly sub-optimal in meeting the performance, energy efficiency, and scalability demands for applications with restricted resources. At the same time, AI techniques themselves are being used to enhance and even automate processor design, creating a reciprocal innovation cycle between AI and hardware. Additionally, AI technology can become implemented deeply into the processor hardware architecture in order to enable a adaptation of the architecture supported by inference results of the AI.

This presentation shows selected opportunities for developing architectures of embedded processors using new features of AI. First, it examines how AI accelerates innovation in processor architecture. Furthermore, first results will become presented what benefits the deployment of AI technology in processors have.

A particularly promising direction lies in run-time adaptive hardware architectures. New approaches, such as the FPGA based GPU or the high flexible iCore, illustrate how inference results from AI models can directly guide the adaptive reconfiguration of processor hardware during operation. These architectures are not static; instead, they monitor workload characteristics and dynamically tune their configuration—such as parallelism, precision, memory hierarchy, and execution units—to operate at the most beneficial point of the power-performance curve at any given time (see figure 1).

This run-time adaptability, informed by AI-driven inference and control, enables systems to achieve higher performance while simultaneously reducing power and energy consumption. It represents a shift from the traditional worst-case provisioning approach to an intelligent, context-aware optimization that evolves with the workload in real time.

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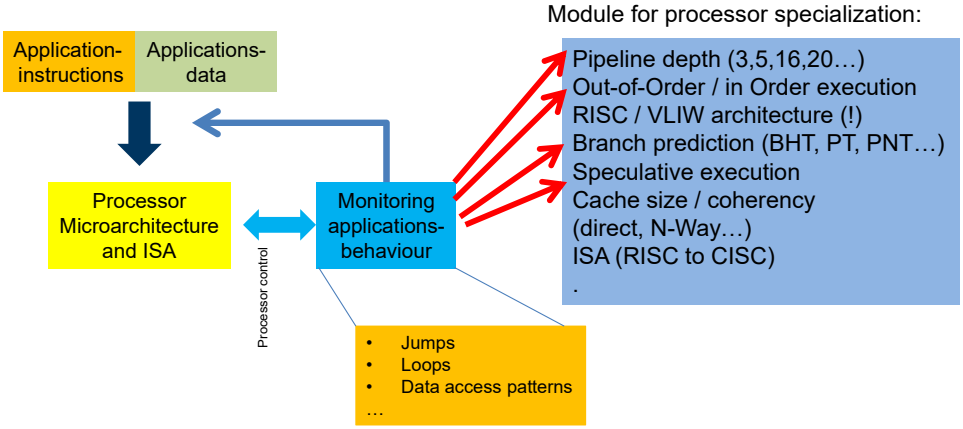

Figure 1. Monitoring and selection of processor mode

Electronic Control Systems for Ion Trap Quantum Computers

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***Abstract*—Ion trap quantum computers are complex optoelectronic systems that require several electronic subsystems orchestrated to sub-1ns precision, both low-noise and high speed. WUT developed a modular control system in EEM/DIOT form factor called SINARA [1].**

(Standardised Instrumentation Architecture for Research Applications). SINARA became the de facto standard in atomic and Molecular laboratories worldwide; a few leading quantum computer manufacturers also use it. Its success, which can be attributed to the open-source, open-hardware licensing model, has significantly advanced the field of quantum computing by providing a reliable and adaptable control system. SINARA was primarily developed for lab applications but recently has been transformed into an industrial form factor (DIOT[5]) because many lab projects have turned into spin-offs and startups.

The scaling of quantum computers creates several technological issues. Most topologies are enclosed in a vacuum and use cryogenic temperatures. Future quantum computer architectures need to implement electronic control systems capable of steering hundreds of thousands of electrodes with high precision and relatively high voltage of a few dozen V. Within the framework of the Quantera SIQCI [3] project, a collaborative effort aimed at advancing the field of quantum computing, we are building a demonstrator of such a scalable control system. An essential step of the design process is characterising a standard 180nm high voltage process at temperatures below 10 K. The next step is updating the process PDK and designing the test structures using updated models. This paper presents the requirements for such a control system, the first results of the measurements and the design methodology.

Furthermore, this talk will unveil the first coherent operations results performed on ions trapped in the WUT labs using the SINARA system, marking a significant milestone in our system's practical applications.

***Keywords*—FPGA, ASIC, Cryogenics, AMO, Trapped Ions, ARTIQ**

I. Introduction

Scalable, fault-tolerant quantum computers (QCs) will solve certain classes of problems significantly faster than their best classical counterparts. While the ultimate realisation of a fault-tolerant device is considered a long-term goal, noisy intermediate-scale quantum (NISQ) devices are already available today and are expected to be used, for example, in optimisation tasks, novel material design, or critical processes in logistics, healthcare, and finance. However, current quantum devices cannot be scaled to 1000 qubits or efficiently programmed due to the lack of suitable control systems and software. As a result, the roadmap for building large-scale, universal computing devices faces a key technological "bottleneck**." The WUT team develops dedicated control systems for ion trap quantum computers. Since 2022, our quantum computer infrastructure has been built based on developed technology[5].** Several key technologies are necessary to create a multi-thousand-qubit ion trap quantum computer:

Advanced cryogenic ion trap with integrated optics (photonic integrated circuit), ion transport electrodes (QCCD) and readout sensors, capable of trapping and manipulating of hundreds of thousands of ions

Scalable, low-noise electronic circuits tailored for ion transport operations such as moving, splitting, and merging sub-registers within segmented traps at room temperature and under cryogenic conditions;

Efficient compilation of quantum algorithms based on low-level instruction sets for segmented QPU units, optimizing algorithms with more than 100 qubits.

II. SINARA Control Sysem

A. Introduction

SINARA is a modular, open-source measurement and control hardware ecosystem designed for quantum information processing applications that require deterministic, high-precision timing. It is based on industrial standards and consists of over 50 digital and analogue input and output modules. The hardware is controlled and managed by ARTIQ [2], an open-source software system for experimental control that provides nanosecond timing resolution and sub-microsecond latency via a high-level programming language. The measurement and control systems used in quantum physics experiments suffer several problems. In general, an improvised solution is built in-house without enough consideration for good design,

Several grants and contracts funded this research: NESTER (MAZOWSZE/0153/1900), DOB-SZAFIR/01/A/023/01/2020, IDUB-POB-FWEiTE, QUANTERAII/1/80/SIQCI/2022, POIR.01.01.01000553/20

reproducibility, testing, and documentation. It makes those systems unreliable, fragile, difficult to use, maintain, and reproduce in other labs, and hard to repair. It also duplicates work in different laboratories. Also, the performance and features of the existing systems (e.g., regarding pulse shaping and synchronisation abilities) are becoming insufficient for some experiments.

Sinara and ARTIQ projects address the above issues by providing a collaborative hardware and software environment that is both open-source and commercially available from multiple vendors. The community involved in the Sinara project has successfully developed over 100 boards and modules over the last eight years. Some are already commercially available, with most of the rest to follow. Nearly all modules were developed at the WUT, most of which were designed by the Author. The design of SINARA is indebted to much prior work on control hardware and software by the ion-trapping community. Currently, SINARA is the leading control system in the AOM community, and several quantum computing vendors use it as a foundation for their systems.

B. SINARA ecosystem

The Sinara ecosystem offers a nearly complete set of modules performing the following functions:

- System controllers
- Analogue to digital and time to digital converters
- Digital to analogue converters
- Servos and regulators
- Fast digital Inputs and Outputs
- Camera and optical sensor interfaces
- Arbitrary Waveform Generators (AWG)
- Radio Frequency and DDS synthesisers
- RF, low frequency, and HV amplifiers
- Low-voltage and high-voltage power supplies
- Various adapters and converters

III. ION TRAP QUANTUM COMPUTER SCALING

Practical, real-life problem-solving algorithms require hundreds of thousands of qubits. While the standard, modular SINARA system addresses most quantum computer needs, it fails to deliver signals for future ion trap processing units. Existing and near-term quantum computers up to 1000 qubits are built on the existing SINARA ecosystem, including 32-channel DAC cards, but such a solution is not scalable due to several reasons:

- Difficulty in delivering millions of signals to cryogenic QPU
- Physical space and power needed for hundreds of electronic racks
- Noise limitation of room-temperature electronics, essential for high-fidelity qubits

Due to those constraints, WUT develops dedicated ASICs within the Quantera SIQCI project.

Those ASICs need to address the following issues:

- Operation at 4K in ultra-high vacuum
- Offer scalability to millions of DAC channels
- Provide high voltage operation of at least +/-20V
- Consume very low power, the entire cooling budget at 4K is a few Watts
- Provide ultra-low noise, at least 16-bit precision and very low drift
- Integrate with the SINARA/ARTIQ ecosystem

The WUT team developed and succeeded in tape-out and cryogenic measurements of the first test ASIC, which includes DAC and test structures. The second, multi-channel DAC is being finalised and will be sent for tape-out in June.

ACKNOWLEDGMENT

I want to thank the entire Sinara and the ARTIQ community, without whom this project wouldn't exist. Special appreciation to: David Allcock, Chris Ballance, Tim Ballance, Sebastien Bourdeauducq, Joe Britton, Ken Brown, Stanisław Hanasz, Tom Harty, Robert Jordens, Anna Kaminska, Marcin Kiepiela, Paweł Kozakiewicz, Paweł Kulik, Jakub Matyas, Jonathan Mixrahi, David Nadlinger, Christian Ospelkaus, Krzysztof Pozniak, Maciej Przybysz, Drew Risinger, Daniel Slichter, Ana Sotirova, Mikołaj Sowinski, Filip Switakowski, Zbigniew Wawrzyniak, Weida Zhang, Konrad Norowski, Krzysztof Siwiec, Dominik Kasprowicz, Tomasz przywózki, Adam Borkowski, and others involved.

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Mixed Mode: More than Analog and Digital

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SUMMARY

In its origin, the term "Mixed Mode" referred to integrated circuits (ICs) made from digital and analog components. Mixing these types of circuits opened the field of IC design to include a vast scope of functionalities, paving the way for versatile circuits including system on chip (SoC), and lab on chip (LoC), amongst many more.

Nowadays, due to the evolution of technologies, manufacturing processes including transistors than reach cut-off frequencies in the hundreds of GHz range are readily available, providing sophisticated bases for the design and development of a slew of wireless circuits impacting telecommunications, the Internet of Things (IoT), industrial and medical applications, and many more.

All these wireless circuits require, besides transistors, resistors and capacitors, inductors, transmission lines on chip, through silicon vias (TSVs) for 3D integration, and antennas to transmit and receive all sorts of data. Hence, mixed mode circuitry includes many passive devices working together with active ones to be able to meet the stringent requirements imposed on these types of circuits.

Inductors, for instance, are mandatory in RF circuits as impedance matchers, filters of all kinds, resonant circuits, and transformers. And even though inductors have a resonant frequency, they are present in the chip, representing parasitic components at different frequency ranges. An example of an integrated inductor is shown in Fig 1, showing two different shielding platforms.

Transmission lines and coplanar waveguides are other fundamental elements of RF circuits. Stages in the same chip have to be connected to others, and eventually to the chip package. The impedance between stages has to be matched, and therefore, these structures have to be fully characterized and modeled in order to design interconnects adequately.

Three D integration has become common in recent years, since it is a convenient and direct form to create complex systems on-chip while reducing losses and interconnect delays. This requires conducting lines from the active part of the chip to the bas of the wafer, Through Silicon Vias (TSVs), which have to be manufactured with reliability and efficiency in mind. Hence, accurate models for TSVs are also needed to design ICs for 3D integration.

As technology evolves, the cut-off frequency that active devices can attain is ever increasing, reaching now values of the order of several hundreds of GHz. This has made the inclusion of antennas in the same IC possible, notwithstanding all the limitations that are encountered in the process. Nevertheless, research on integrated antennas has been a very active field in recent times, and it will surely continue to be so.

To characterize and model devices for RF ICs, the measurement set-up has to be calibrated and the data must be subsequently de-embedded. As the frequency of operation increases, this is not straightforward, and some additional procedures must be carried out to model the actual behavior of the device. For instance, when measuring an integrated transmission line, the model shown in Fig. 2 has to be taken into account.

This talk will present the efforts that the High-Frequency Group at the *Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE: National Institute for Research on Astrophysics, Optics and Electronics)* has undertaken in the last 35 years, covering different aspects of active device modeling, inductors, transmission lines, coplanar waveguides, TSVs and antennas. Some aspects regarding measurements, calibration and de-embedding will be also highlighted, as they are ever present in the characterization of devices in the high-frequency regime.

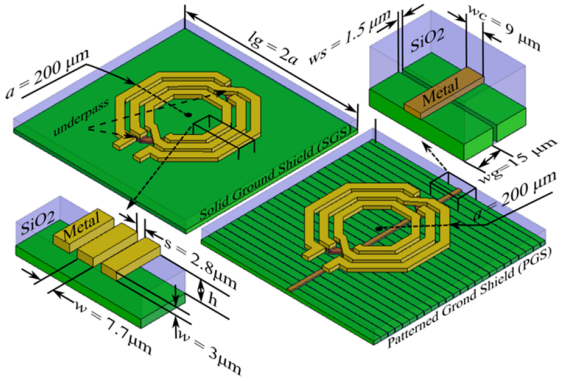

Fig. 1. Integrated inductors with a solid ground shield and a patterned ground shield.

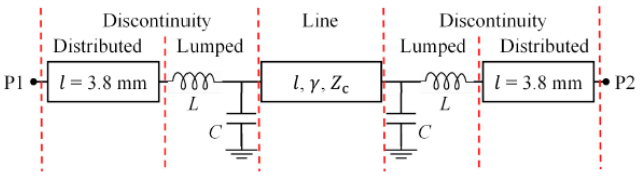

Fig. 2. Model for an IC transmission line.

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Modern Challenges in Hardware Design

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***Abstract*—Over the years, the technology of designing and manufacturing electronic devices has evolved dynamically, introducing new possibilities in the production of integrated circuits, devices, and systems. Despite advancements, significant challenges remain. The presented problems will be supported by examples from real-world projects, including Open Hardware, Chiplets, and security issues such as supply chain attacks, side-channel vulnerabilities, and quantum computing threats. This presentation aims to highlight interesting research directions related to hardware design that are crucial from an industrial perspective.**

***Keywords*—hardware design, design challenges, cybersecurity, supply chain security.**

I. Introduction

Each year, we observe increasingly rapid advancements in technologies related to the design and manufacturing of electronic circuits. These new possibilities often bring new challenges that are entirely different from those we have faced in the past. This presentation highlights attractive research directions related to hardware design that are crucial for industry. By examining recent trends and real-world examples from last years, the challenges related to Open Hardware, Chiplet technology, and critical security issues will be explored. The discussion will provide insights into how these problems impact design and production processes to finally consider strategies to address them.

II. Supply Chain Security Challenges

In today's world, electronic devices have become increasingly complex, with components sourced from numerous manufacturers. Modern integrated circuits often incorporate intellectual property (IP) from multiple suppliers, creating an interconnected system [1]. The design and manufacturing processes involve many subcontractors, each playing a critical role.

The presentation will showcase real-world cases where attacks on advanced supply chains had significant consequences, illustrating system vulnerabilities and the impact of security breaches. It will also discuss current countermeasures to prevent such situations. By examining these cases, we aim to highlight the importance of robust security practices and ongoing efforts to safeguard the integrity of electronic devices.

III. Internet of Things (IoT)

The market for IoT devices is experiencing rapid growth. Despite this swift development, there are no established industry standards for IoT that enable efficient and secure design and deployment of IoT-class devices [2]. This presentation will showcase solutions that offer hope for changing this situation, providing a pathway towards standardized practices that ensure both effectiveness and security in IoT device development.

IV. Side-channel Attacks

In recent years, we have observed a significant increase in both the cost and scope of side-channel attacks [3]. This trend is driven by the substantially decreasing cost of tools required to execute such attacks. The presentation will showcase representative examples of successfully conducted side-channel attacks on real-world devices available in the market. These examples will highlight the vulnerabilities exploited and the impact of these attacks, emphasizing the need for enhanced security measures in hardware design.

V. Quantum Computing

The capabilities of quantum computers are increasing significantly. Currently, widely known implementations of quantum computers do not allow for effective attacks on classical cryptographic algorithms. However, it is anticipated that with the advancement of quantum technology, this will change in the future [4]. The presentation will discuss current strategies to address this increasingly real threat, providing insights into the measures being developed to safeguard against potential quantum computing attacks.

VI. Conclusion

The dynamic evolution of electronic device design and manufacturing presents both opportunities and challenges. By focusing on innovative research directions and addressing critical issues such as supply chain security, IoT standards, side-channel attacks, and quantum computing threats, we can drive the advancement of the electronics industry.

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Advancing FOSS Compact Modelling: From OTF Transistors to Mott Memristors

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A Generic Approach for Compact Modeling of Variability and Low-Frequency Noise in Organic Thin-Film Transistors

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SUMMARY

In organic thin-film transistors (OTFT), low-frequency noise (LFN) is dominated mainly by grain-boundary traps and mobility fluctuation [1]. Furthermore, OTFTs are sensitive to process variability. Charges being trapped in the channel region cause a local variation of the accumulated charge density, having impact on the threshold voltage of the device [2], [3] and reducing the effective carrier mobility in the channel by Coulomb scattering. Based on the results published in [3], [4], we present a generic physics-based modeling approach for drain-current fluctuations by carrier-number and correlated mobility fluctuations, which leads to similar expressions for drain-current variability and ΔN noise in OTFTs.

Measurements performed on fabricated OTFTs show drain-current variability ([5]). In [3] it has been shown that the drain-current variability in the subthreshold regime is dominated by carrier-number fluctuations, whereas for above threshold operation the mobility-fluctuation effect by correlated Coulomb scattering comes to the fore (Fig. 1).

In case of LFN, measurements on staggered DNTT OTFTs have shown that ΔN noise alone is not sufficient to describe the noise spectra in the deep subthreshold regime of operation (refer to Fig. 2) [4]. Here, LFN due to mobility fluctuation ($\Delta\mu$ noise) must be included.

In conclusion, following a generic modeling approach, the combined equations for carrier-number and correlated mobility fluctuations allow consideration drain-current variability and LFN noise in a charge-based compact model of OTFTs following similar expressions for all regions of operation. The results have been shown to be good agreement with measurements. However, for percolative mobility fluctuation dominant in operation below threshold additional expressions have to be considered for modeling LFN noise.

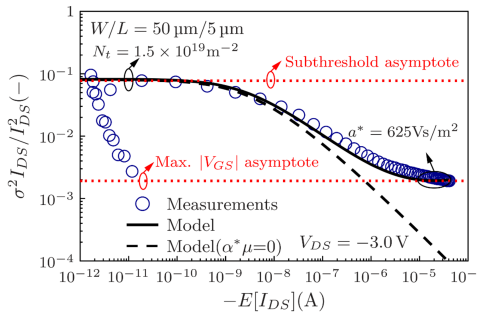

Fig. 1. Normalized drain-current variance $\sigma^2 I_D/I_D^2$ versus mean-value drain current $E[I_{DS}]$ for OTFTs with L = 5 μm, measured at V_{DS} = -3.0 V [3]. The experimental mean values were calculated over a population of 16 nominally identical transistors. Full line: model including, dashed line: without Coulomb scattering [3].

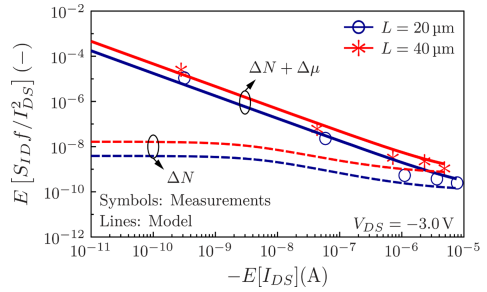

Fig. 2. Mean-value power spectral densities $E[S_{ID}/I_D^2]$ @ 1 Hz vs. drain current, measured at V_{DS} = -3.0 V [4]. Full line: model including, dashed line: without $\Delta\mu$ noise. The experimental mean values were calculated over a population of 15 nominally identical transistors [4].

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Extraction of Open-Access-PDK Active Inductance Parameters with FOSS Tools

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Extended Abstract

A recent trend in support of integrated circuit (IC) design and manufacture has been the release of open-access production development kits (PDKs) [1] [2], encouraging the use of FOSS ECAD tools at every stage in the semiconductor manufacturing cycle [3]. This in turn under-pins a growing "Open-Hardware" movement [4] [5] particularly, through the merger of FOSS circuit simulators with freely available open-access PDK kits. Prior to the release of open-access PDKs, Verilog-A compact device modelling acted as a bridge between sub-micron semiconductor models and circuit simulation. This is still true, but the addition of PDK semiconductor processing data to the open-access IC design tool chain now allows the application of FOSS tools to be extended to the characterization of manufacturable IC circuit blocks. The main elements in the PDK/FOSS merger are model libraries, characterized by Verilog-A parameters extracted from measured device data. In parallel there has also been a steady improvement in FOSS circuit simulator modelling capabilities that link extended analysis and simulation features with post simulation graphical visualisation. These allow, at an early stage in the IC design/manufacture sequence, extraction of analogue block parameters from simulation output data. This paper introduces a number of extended Qucs-S/Ngspice circuit simulation capabilities and demonstrates their application in the analysis and design of a single ended CMOS active inductor cell designed with the IHP-SG13G2 BiCMOS technology node. Particular attention is given to the modelling and simulation of the fundamental two transistor CMOS active inductance based on a admittance approach that allows simple extraction of the inductor parameters from real and imaginary admittance properties and their differentiation in the frequency domain. Figure 1 shows a Qucs-S/Ngspice test bench for simulating the admittance of a CMOS active inductance over a GHz frequency band. Fig. 2 illustrates a set of typical Zin and Yin simulation data plots.

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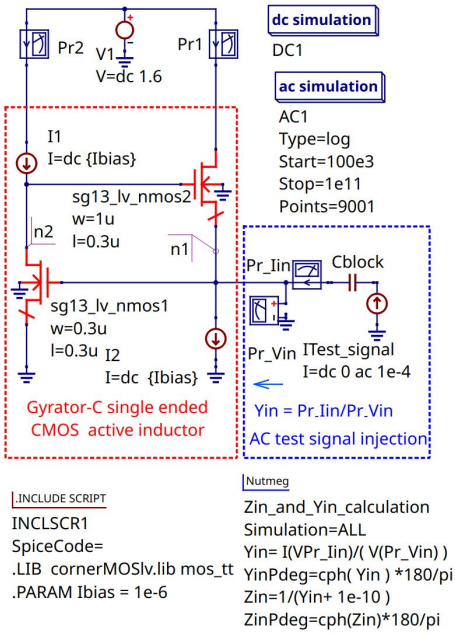

Fig. 1. A Qucs-S/Ngspice test bench for evaluating the a.c. performance of an IHP-Sg13g2 technology CMOS active inductance.

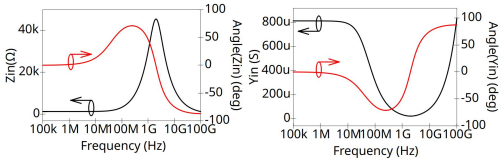

Fig. 2. Example IHP-Sg13g2 thin oxide technology CMOS active inductor Zin and Yin characteristics for $Ibias = 1\mu A$

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Spiking Neurons Demystified by a Dynamical Model of Mott Memristors

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I. Introduction

Bio-inspired sensory neurons implemented with phase-change materials [1] like Vanadium dioxide (VO_2) [4] are able to encode the perceived information into spikes in the time domain. Since they fully operate in the analog world and do not require digital conversions and memories, exceptional energy efficiency is promised for these systems compared to ultra-low-voltage CMOS architectures [1].

At UCLouvain, VO_2 *memristors* exhibiting reversible Metal-Insulator Transitions (MIT) have been micro-fabricated [4]. The experimental static characteristics of one typical device are shown in Figure 1(a) in two different configurations: voltage- or current-controlled, respectively. A circuit made of a VO2 memristor (Figure 1(b)) driven by an appropriate current source (e.g. a MOS transistor,) can leverage the MIT to produce continuous voltage spikes on the output capacitor shaped by a charge/discharge process (Figure 1(c)). Such experimentally evidenced spiking or oscillating behaviour still awaits insightful mathematical model and quantitative predictions from the theory of nonlinear dynamical systems.

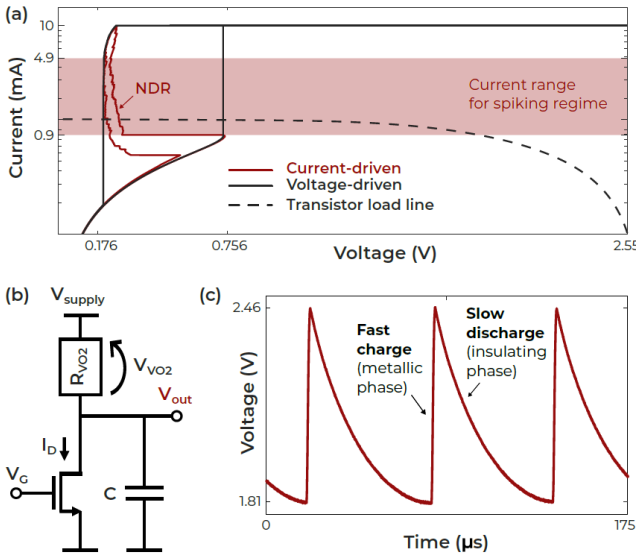

Figure 1. (a) Static characteristics of a micro-fabricated VO_2 memristor in both voltage- and current-controlled mode. (b) Schematic of the spiking sensory neuron. (c) Experimentally measured spikes when the neuron operates as a relaxation oscillator, suggesting that the studied system has a closed orbit that is a limit cycle. Reproduced from [4].

II. Nonlinear Dynamical Model of Mott Memristors

A insightful toy model of Mott memristors capable of reproducing the experimental static characteristics such as those reported in Figure 1(a) has been proposed in the pioneer modelling work of [2], more deeply exploited by [3]. The memristor is regarded as a nonlinear dynamical system with internal state u, describing the metallic phase fraction, and input v or i, respectively in voltage- and current-controlled mode. Consistently with Chua's formulation, the dynamics of the memristor is then shown to be governed by two coupled nonlinear equations (we here limit to the current-controlled mode):

$$v = f(u, i) = R(u)i \tag{1}$$

$$\frac{\mathrm{d}u}{\mathrm{d}t} = g(u, i) \tag{2}$$

where $g(u, i)$ is a strongly nonlinear function absorbing all the electrothermal phenomena inherent to the device.

As we will present, the state model (1) and (2) can be harnessed to discuss the stability of the steady states of the memristor system. In particular, we will mathematically show that, in current-controlled mode, such device exhibits the so-called *negative differential resistance* behaviour (Figure 1(a)), all the steady states being stable, while this region is unstable and hence cannot be observed in voltage-controlled mode. We will then provide an oscillation criterion for the neuron of Figure 1(b), thought as a Van Der Pol relaxation oscillator. Future work also includes fine investigation and analysis of the *stochastic bursting* regime, offering more sparsity and promising lower energy consumption.

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Artificial Intelligence in Electronic Systems

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Video-assisted Dentistry with Deep Neural Networks

(Invited paper)

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***Abstract*—This study aims to develop a novel video-based technology to support the next generation of digital dentistry. By enabling enhanced and continuous intraoral visualization, the system has the potential to improve educational environments, clinical training, and real-time operational workflows in conservative dental procedures. The proposed approach is grounded in multi-task learning, where a unified neural network is trained to simultaneously perform multiple vision based tasks for enhanced human-system interaction. To facilitate this development, the study leverages existing and newly curated dental video datasets, including annotated sequences for training and evaluation.**

***Keywords*—dentistry, multi-task learning, video**

I. Introduction

This study aims to develop a novel video-based technology for next-generation digital dentistry. A miniature camera integrated into a dental handpiece could enable dentists to continuously monitor the treatment area during conservative dental procedures (Fig. 1). Such integration promises to enhance clinical outcomes, improve ergonomic efficiency for dental professionals, and elevate the quality of dental education and training. However, image acquisition in intraoral environments presents significant challenges. Miniaturized sensors and optics introduce visual distortions, while handpiece movements cause eye strain. Additionally, complex intraoral conditions—such as noise, blur, illumination changes, shadows, and dynamic fluids—degrade visual clarity, complicating continuous macro-visualization of the treatment field.

II. Method

To address the intraoral imaging challenges [5], we propose a vision-based system capable of jointly solving multiple interrelated video processing tasks. The proposed decoder-centric multi-task network [3], [2] enhances video quality under challenging conditions such as low light, noise, and camera shake. It integrates auxiliary tasks—teeth segmentation and teeth-based motion estimation—to support temporal alignment of encoder features, enabling more stable and accurate restoration. Perform robust long-range motion compensation [4] allows stabilizing the tooth's visual representation in the video, reducing eye fatigue even under fluid motion and fluctuating lighting.

III. Conclusions and Future Work

Integrating video super-resolution techniques will further enhance image quality, offering visual feedback comparable to that provided by dental microscopes [1]. Real-time intraoral video enhancement could enable 3D reconstruction for augmented reality and immersive dental education, analogous to recent advances in minimally invasive surgery. Additionally, semantic segmentation of clinically relevant structures—such as caries, dentin, and pulp—can support young practitioners in performing more precise and less risky procedures, while enabling expert-guided assessment of their clinical performance. Through this comprehensive approach, we seek to lay the technological foundation for intelligent, vision-assisted dental procedures in modern digital dentistry.

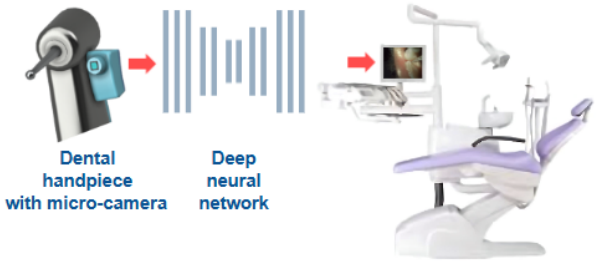

Fig. 1. Camera-assisted dental procedures offer significant potential to enhance training, education, and documentation, streamline clinical workflow and ergonomics, and ultimately improve patient care. However, the complexity of intraoral imaging—characterized by noise, motion blur, and varying lighting conditions—makes continuous macro-level visualization on custom displays particularly challenging. Effective video enhancement techniques are therefore essential to provide a clearer and more stable view of intraoral scenes throughout the entire course of tooth's treatment.

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Anomaly Detection on the Edge: Comparison of Reconstruction and Classification Based Approaches

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***Abstract*—In this work we discuss and evaluate different approaches to solving anomaly detection task when the target platform is a tiny microcontroller. We investigate modeling techniques and propose a comprehensive set of measurements to analyze performance, compute and memory requirements, and power efficiency. We run experiments to collect these measurements on platforms used in TinyML systems including Cortex-M7, Cortex-M55 and Ethos-U55 running TensorFlow Lite for Microcontrollers. The measurements are collected for an autoencoder in reconstruction-based anomaly detection and a MobileNetV2-like model trained for classification. We show which approach is more suitable depending on the system requirements and constraints. This work underscores the need for a holistic approach in selecting modeling and deployment strategies, providing empirical evidence to guide the development of efficient on-device anomaly detection systems.**

***Keywords*—Edge computing, embedded software, tiny machine learning, anomaly detection, sound recognition.**

I. Introduction

Tiny Machine Learning (TinyML) enables machine learning models to be executed on resource-constrained microcontrollers and other low-power edge devices, for instance, for anomaly detection to enable on-device monitoring of heavy equipment, in automotive or industrial settings. This paper addresses the deployment of anomaly detection systems on the representative TinyML hardware. We compare distinct modeling strategies and system configurations. Through precise measurements and analysis of key metrics, this work aims to provide an insight into the current capabilities of TinyML for anomaly detection.

II. Experiments

We train the models for anomaly detection using the reconstruction error and the classification approaches. In the former, an autoencoder is trained on normal samples to reconstruct the input. The reconstruction error is the anomaly score. For classification, a multi-class dataset of normal samples is used to train a model, which during evaluation is used with a known class. The model negative confidence in this class is the anomaly score. We use modified baseline models, an autoencoder and a MobileNetV2-like [1], from the DCASE task 2 challenge [2]. We use MIMII [3] and ToyADMOS [4] datasets of acoustic sounds generated by industrial machines.

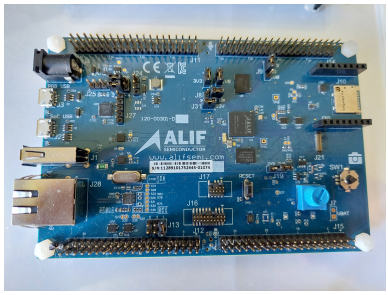

Fig. 1. DUT2 - Alif Ensemble DevKit Gen, equipped with ARM Ethos U55 Neural Processing Unit.

We evaluate the models deployed on representative devices used in TinyML systems. We use ARM Cortex-M CPUs, also test acceleration with neural processing unit, ARM Ethos-U55 (Fig. 1). We collect a comprehensive number of measurements, including inference latency and energy consumption, peak memory usage, storage for code, model parameters and MACs across different configurations.

III. Conclusions

We conclude that to select the appropriate model and platform, a holistic approach is necessary. The decision on the model used impacts the latency, memory footprint and energy consumption, and must be made by considering technical and business requirements. In the future work, we will focus on employing neural architecture search techniques which use the proposed measurements to find optimal models or a model family for given design requirements.

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Application of Dual-Q TQWT for Atrial Fibrillation Detection with Three-Layered Neural Network

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EXTENDED ABSTRACT

Atrial fibrillation belongs to the class of arrhythmia diseases and automatic detection algorithms are the desired early stage of diagnosis of this type of arrhythmia. Various methods are employed to analyse the characteristics of atrial activity in the electrocardiography (ECG) signal.

This work proposes and evaluates an improved algorithm for automatically detecting atrial fibrillation (AF). The algorithm analyzes the ECG signal by dividing it into segments. The first step of the proposed method involves preprocessing, which includes signal filtering and the extraction of feature vectors based on two composed signals on the base of high Q-factor and low Q-factor resonance components obtained after Dual-Q Tunable Q-factor Wavelet Transform (Dual-Q TQWT) and finally, the classification stage, which contains training (for creating a classification model) and testing.

The Dual-Q TQWT application comprises the simultaneous use of the two Q-factors of the wavelet transform [1]. This transformation allows of decomposition the signal $\mathbf{x}$ into two components $\mathbf{x}_1$ and $\mathbf{x}_2$, where $\mathbf{x}_1$ consists mostly of sustained oscillations and $\mathbf{x}_2$ consists mostly of non-oscillatory transients such that $\mathbf{x} = \text{TQWT}_1^{-1}(\mathbf{w}_1) + \text{TQWT}_2^{-1}(\mathbf{w}_2)$, where $\mathbf{w}_{i,j}$ denotes wavelet coefficients of TQWT_i for $i = 1, 2$ and TQWT^{-1} is the inverse transform [2]. The energy from each sub-bands are determined on the base of $\mathbf{w}_1$ and $\mathbf{w}_2$. The implemented feature estimation methods are all inherently finite or possess stopping criteria to avoid latency or run-time errors. With a data window width of 20 beats, the window is marked with a pre-trained classifier.

A three-layered neural network classifier is applied in this work. This architecture enables to capture and model of the nonlinear and intricate relationships in subbands of energy distribution. The structure of the neural network applied in this work is presented in Table I.

TABLE I
THE DETAILED PARAMETERS OF THE NEURAL NETWORK STRUCTURE

#	Network layer type & activation function
1	Input Layer for 58 features with 'zscore' normalization
2	Fully Connected Layer with 500 neurons and ReLU
3	Fully Connected Layer with 300 neurons and ReLU
4	Fully Connected Layer with 50 neurons and ReLU
5	Output Layer with 2 neurons and SoftMax

The performance of the AF classification is evaluated by the following quality factors: accuracy (Acc), sensitivity (Sen), specificity (Spec), positive predictivity (PPV), and F1 score. Factors are calculated on the unseen (testing) data set using a confusion matrix. The proposed method is evaluated using the publicly available MIT-BIH Atrial Fibrillation Database of ECGs. The cross-validation (CV) statistical method is used in this work to estimate the skill of the used classifier for AF detection method assessment. The performance of the proposed algorithm was compared against several methods on the same, obtained in this approach feature vectors as well as methods which were also evaluated on the MIT-BIH Atrial Fibrillation Database. The results for comparison are summarised in the Table II.

TABLE II
RESULTS OF AF DETECTION WITH DIFFERENT METHODS ON THE OBTAINED FEATURE DATABASE

Classifiers	Sen %	Spec %	PPV %	Acc %	F1 %
SVM	98.71	97.32	97.82	98.09	98.27
KNN	98.91	98.76	98.98	98.73	98.85
Ensable Subspace KNN	98.91	**98.96**	**99.14**	98.93	99.03
three-layered NN	**99.02**	98.91	99.11	**98.97**	**99.07**
[3] LS-SVM	98.86	98.96	99.04	98.95	98.84
[4] D2AFNet	98.39	98.57	99.19	98.45	98.78

This study presents and evaluates a novel and reliable algorithm for detecting AF episodes in ECG signals. The algorithm utilizes a classifier based on a three-layer neural network and incorporates a feature vector that includes energy indices from high and low Q-factor subbands derived from the Dual-Q TQWT. The proposed method yields better results than traditional reference methods.

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Application of Modified Particle Swarm Optimization Algorithm in FIR Filter Design

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SUMMARY

In this work we present an application of Particle Swarm Optimization (PSO) algorithm as a support in the design of Finite Impulse Response (FIR) filters. The conventional PSO algorithm was not sufficient to obtain desired filter parameters for filters longer than 20 coefficients. For this reason, we used an adaptive PSO algorithm that allows for adjustment of several key parameters during the optimization process of the swarm. In comparison to existing adaptive algorithms, in which for example only the inertia coefficient was subject to change, in our approach the possibility of changing several parameters simultaneously has been introduced. In our approach we additionally modify the social and cognitive coefficients in parallel. As a result, it was possible to obtain satisfactory results for FIR filters of lengths exceeding 50. In this work, we focused in particular on examining the effect of the swarm population size on the algorithm convergence. It turned out that for FIR filters of lengths around 40-50, satisfactory results are obtained with the number of particles in the swarm at the level of 100-150.

Designing FIR filters with the use of the PSO algorithm is an alternative approach to conventional methods known since years. It requires defining an appropriate fitness function, which allows for the evaluation of differences between the theoretical and desired frequency responses. One of the assumptions of this work was to achieve a linear phase response. The design criteria may also include the passband and stopband boundaries, as well as minimizing signal distortion in the passband. The objective function can be defined in such a way as to minimize the sum of absolute errors in the passband and stopband. Optimization of such a fitness (objective) function leads to better attenuation of signals in the stopband, minimal ripples in the passband, and optimal transition width between these bands.

In this work we used the objective function that is a weighted sum of two criteria related to the accurate reconstruction of the passband and stopband of an ideal filter. Both bands are defined using cut-off frequencies. Additionally, a parameter associated with the transition band width is introduced, which masks error accumulation within specific frequency ranges. This is because the dynamics in this band largely depends on the filter size and could mislead the algorithm.

Selected obtained results are shown in Fig. 1. In this case the filter designed using the PSO algorithm performs better in damping oscillations in the passband. However, it is characterized by a wider transition band than the filter designed using the conventional window method. Both filters offer a similar attenuation. In the case of the filter designed with the PSO algorithm a wider transition band has been obtained.

Results presented in our work are a fragment of a broader investigations on this topic. These studies show that the PSO algorithm allows for the design of a filter with a moderate length. In following stages of the project, it is planned to split filters with long impulse responses into shorter sections connected in series, and then optimize them separately. Optimizing each of such shorter sections separately would be easier due to the significantly smaller dimensions of the search space.

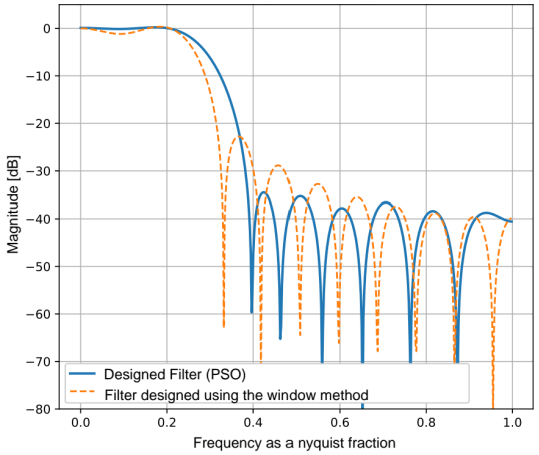

Fig. 1. Magnitude response of the low-pass FIR filter obtained using the PSO algorithm with improved parameters.

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Design Flow for AI-driven Medical Systems Demonstrated through an Example in Dental Imaging Analysis

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I. Introduction

The use of Machine Learning (ML) mechanisms for image analysis in dentistry may potentially bring many benefits. At the same time, potential challenges may include the availability of dental images, the availability of specialist imaging equipment, and the selection of an appropriate ML model. The main goal of this paper is to propose a procedure for designing an ML-based module of a dental system for analyzing dental images, using the example of a tooth detection algorithm within images obtained from popular devices such as a camera or a smartphone. As part of this paper, a review of open access dental image datasets with assumed characteristics was conducted, followed by a review of ML models used for tooth detection. Next, a proposal for the architecture of a tooth detection module was developed along with a prototype implementation version. The works carried out also constituted an extension of the DentIO system, enabling, among other things, the generation of dental diagrams based on voice commands.

In this paper a fragment (presented in Fig.1) of the system that supports dental practice is analyzed using the automatic analysis mechanism of dental images for tooth detection, its efficiency, complexity and potential availability for dentists and patients. In particular, in terms of the availability of the algorithm, one of the assumptions made is to limit the input data only to images from relatively common devices, such as a camera or a smartphone. Such an approach might potentially increase the range of recipients due to the lack of the need to use specialist dental imaging equipment, however, on the other hand, it might leave the question of the potential algorithmic efficiency. An additional challenge associated with this approach might be the availability of public dental image datasets with such characteristics on the basis of which AI models could be trained. In the longer term, beyond the scope of the current article, the suggested algorithm could be one of the elements of the method developed to support the diagnosis of Temporomandibular Joint Disorder (TMD). The suggested tooth detection mechanism might potentially be used in the analysis of jaw movement tracking based on the recorded video image.

The following research questions are addressed in this paper.

RQ1 What publicly available dental image collections containing camera images could be found in the literature?

RQ2 What classes of algorithms have been suggested in the literature for tooth detection from dental images?

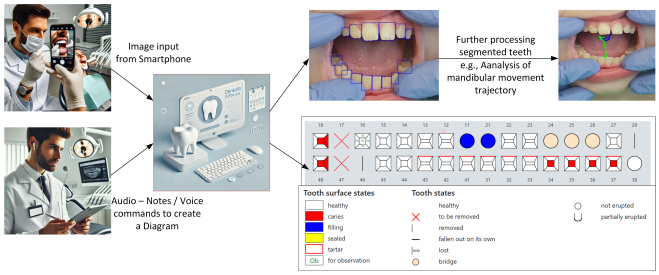

Fig. 1. Example Functionality of the DentIO System

II. Conclusions

As an example of ML models used for image tooth detection, we have discussed an AI tool that would help segment (recognized) teeth from images. The YOLO model was chosen for this application. We have presented the parameters obtained from the trained model. As an example, the practical application of the presented solutions, DentIO, a system that supports dental work, was briefly described. The elaborated module was used successfully for teeth segmentation. This result is an initial point for other algorithms that can be used to improve dental diagnosis, e.g., analysis of mandibular movement trajectory. The elaborated DentIO system is currently under preliminary tests in the dental clinic of the Poznan University of Medical Science.

Acknowledgements

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Edge Computing of Human Poselet

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Extended Abstract

Human Pose Estimation in 2 dimensions (HPE 2D) involves detecting keypoints (e.g., joints) in human images and assembling them into skeleton-like structures called poselets. While 3D pose estimation offers richer representations, it is computationally demanding and requires additional sensing equipment. Three model families were selected based on their relevance to edge deployment and support for the ARM-based Jetson Orin Nano environment: You Only Look Once (YOLO) from Ultralytics, Real-Time Multi-Person Pose Estimation (RTMPose) from the MMPose toolbox) and Tensor RT Pose (TRT_Pose) – as a part of the NVIDIA toolkit.

YOLOv8-Pose and YOLOv11-Pose are anchor-free extensions of the YOLO object detection framework, integrating pose regression into a single forward pass with 17 COCO-format keypoints. These models rely on CSP-based (Cross Stage Partial Network) backbones and PANet (Path Aggregation Network) necks, with lightweight versions (M) and heavier, high-accuracy versions (X). RTMPose, in contrast, separates detection and keypoint estimation into two stages: a generic object detector provides bounding boxes, followed by a CSPNeXt-based keypoint regressor with a coordinate classification strategy. The RTMPose head includes convolutional and fully connected layers, as well as a Gated Attention Unit. Finally, TRT Pose employs PyTorch-trained keypoint regression models converted to TensorRT format, using ResNet-18 and DenseNet-121 backbones. These architectures differ not only in design but also in computational cost, ranging from under 1 GFLOP (RTMPose) to over 260 GFLOPs (YOLOv8 X).

To evaluate these models, we used the COCO val2017 dataset, focusing on a subset of 2,693 images with low to moderate person counts. The metrics recorded included average precision (AP), average recall (AR), inference latency (ms and FPS), CPU and GPU utilization, temperatures, and power consumption. In particular, no fine-tuning, quantization, or pruning was applied.

The results show that RTMPose S achieved the highest accuracy (AP 0.667, AR 0.728), though with limited inference speed (5.49 FPS), making it less suitable for latency-critical applications. The YOLOv8 and YOLOv11 X variants achieved competitive accuracy (AP 0.583) while halving latency compared to RTMPose, reaching around 9.4 FPS. The M variants of YOLOv8 and YOLOv11 offered the best real-time performance (17–18 FPS) with acceptable accuracy (AP 0.537). In contrast, TRT Pose models had much lower AP values (0.117 for ResNet-18, 0.148 for DenseNet-121), but excelled in energy efficiency, achieving up to 34 FPS on ResNet-18 with average power consumption just above 8 Watts—barely more than the idle Jetson Nano. However, this speed comes at a significant cost to accuracy.

Fig. 1. Example of RTMPose on image from COCO dataset.

Power and thermal analysis further revealed that the YOLO X models had the highest GPU usage and power draw (over 18W), while the RTMPose models, despite higher latency, maintained lower and more stable thermal footprints. RTMPose also exhibited larger fluctuations in power consumption, likely due to multistage MMPose implementation. YOLO models demonstrated consistent power usage and efficient GPU exploitation. Despite their higher peak consumption, they offered the most favorable trade-off between speed and accuracy.

In conclusion, we identify YOLOv8-M and YOLOv11-M as the most viable models for real-time edge deployment. These models balance inference speed (more than 17 FPS), moderate power consumption, and reasonable accuracy, making them well-suited for interactive or surveillance applications on embedded platforms. RTMPose, while the most accurate, is hindered by latency, making it less practical for real-time use. TRT Pose remains useful for applications with strict power or thermal limits but lacks the precision required for detailed pose understanding.

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Evaluating Device Variability in RRAM-Based Single- and Multi-Layer Perceptrons

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Summary

This work evaluates the effect of stochastic weight variations in resistive random-access memory (RRAM)-based implementations of artificial neural networks (ANNs). It studies two types of ANNs: the Single-Layer Perceptron (SLP) [1] and the Multi-Layer Perceptron (MLP) [2]. The study focuses on comparing their sensitivity under two types of device-level variability: device-to-device (D2D) and cycle-to-cycle (C2C).

A simulation framework is developed using a Variable Neural Network (VNN) model [3], where Gaussian noise is applied to synaptic weights to emulate the statistical behavior of RRAM devices. The extent of variability is controlled by an Adjustment Rate (AR), which defines the proportion of perturbed weights. Quantization is also introduced, with 9 and 21 discrete levels considered, to examine the effect of resolution on accuracy under variability.

Results using the MNIST dataset show that SLPs are significantly more sensitive to variability, with accuracy dropping rapidly as AR increases. In contrast, MLPs demonstrate greater robustness and more gradual performance degradation. Increasing quantization levels from 9 to 21 consistently improves accuracy stability, especially for MLPs. Stochastic quantization further enhances performance in MLPs but has minimal impact on SLPs.

The impact of AR on accuracy is analyzed for the D2D simulation of the MLP with quantization at two levels. As shown in Fig. 1, increasing quantization from 9 to 21 levels improves median accuracy from 77.87% to 83.66%, with the 21-level setup showing greater stability. Similarly, for the SLP Fig. 2, illustrates a drop in median accuracy from 75.41% (21 levels) to 46.85% (9 levels) as AR increases, again highlighting the higher stability achieved with more quantization levels.

This approach helps identify the impact of synaptic weight variation and optimal quantization levels for hardware by analyzing their effects on ANN's accuracy (η), robustness, and AR. It enables the selection of optimized network architectures and practical quantization strategies that balance performance and resource efficiency. Understanding AR's influence supports hardware design by ensuring performance goals are met with minimal overhead, improving efficiency, robustness, and cost-effectiveness.

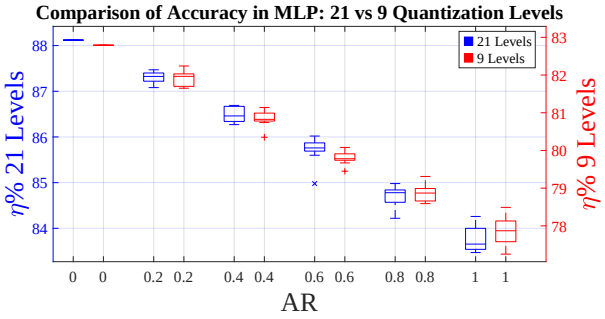

Fig. 1. MLP performance with 21 Quantization levels vs 9 Quantizatio levels

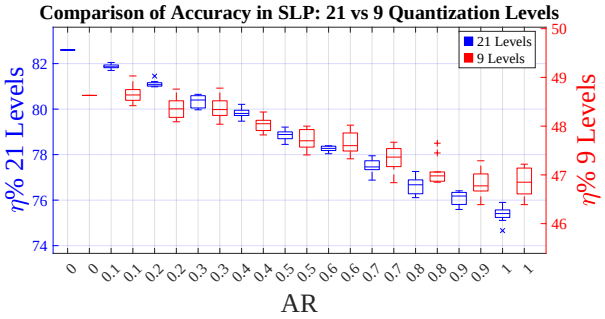

Fig. 2. SLP performance with 21 Quantization levels vs 9 Quantizatio levels

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Design of Integrated Circuits and Microsystems

CMOS OTA for Detector Readout Electronics Integrator in the ALICE FIT Project

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EXTENDED ABSTRACT

The paper discusses the design and optimization of a CMOS OTA (Operational Transconductance Amplifier) circuit for the FIT detector in the ALICE experiment at CERN, aimed at efficiently processing particle collisions in high-noise environments. The OTA scheme is visible in Figure 1.

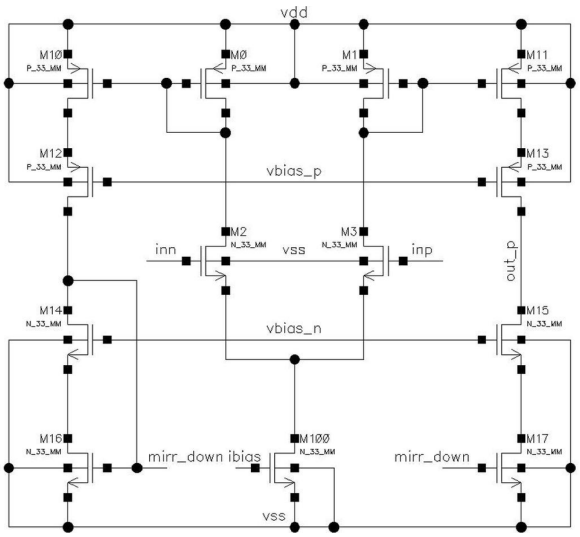

Fig. 1. Scheme of the designed OTA

The OTA is part of an integrated ASIC intended to replace current discrete components, providing a power-efficient, area-efficient solution while handling nanosecond analog pulses. The circuit is implemented using 180-nm CMOS technology within Cadence Virtuoso, and powered by a 3.3 V supply. The paper delves into the specific challenges of maintaining high bandwidth, linearity, and signal stability, alongside reducing power consumption. The chosen OTA architecture, a symmetric CMOS with cascodes, offers a balanced trade-off between these factors, leveraging high currents and careful layout designs to mitigate process-related variations. Simulations reveal that while the OTA performs well under various conditions and corners, calibration systems are necessary to counteract inevitable mismatches.

These features culminate in an OTA that is smaller, uses less power, and maintains functional accuracy relative to its discrete predecessors, despite a reduced input voltage range due to technological constraints (Table I).

TABLE I
SUMMARY OF SIMULATION RESULTS

Parameter [units]	**(a)**	**(b)**	**(c)**
CMOS process [nm]	180	180	XFCB
Supply voltage [V]	±1.65	±1.65	±5
Capacitive load [pF]	50	50	–
DC gain [dB]	53.31	52.91	63
PM [◦]	90.81	90.43	56
GBW [MHz]	7.978	7.908	410
CMRR @DC [dB]	66.5	65.6	90
PSRR+ @DC [dB]	66.1	65.3	74
PSRR- @DC [dB]	46.2	45.1	74
Power [mW]	22.8	22.5	190
Area [mm2]	–	0.044	9
FoM [MHz·pF/mA]	57.7	58	–

(a) Simulation (b) Post-extraction simulation (c) Discrete amplifier

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Design Considerations for Integrated SiGe BiCMOS Phase-Locked Loops in the Millimeter-Wave Band

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Extended Abstract

We present design guidelines for analog phase-locked loops (PLL) at millimeter wave (mmWave) frequencies in SiGe BiCMOS technology. Emphasis is placed on a robust functionality with a relatively constant phase noise performance under ionizing radiation in space. The analog tuning range of the voltage-controlled oscillator (VCO) is split into coarse and fine tuning. Using negative feedback in the fine tuning loop of the PLL, the fine tuning control voltage is kept close to the VCO gain maximum for a constant PLL loop bandwidth. Together with self-triggered sub-band switching, a long lifetime of the PLL is expected, since any VCO degradation will be compensated keeping VCO gain and loop bandwidth fairly constant. An integrated SiGe-HBT based phase detector for mmWave PLLs is proposed, where a fractional-N PLL in the lower GHz range drives several simple mmWave PLLs in a phased-array transceiver.

An integration of the VCO and the loop filter together with the PLL core would give a significant cost advantage. However, the low quality factor of the variable capacitors (varactors) in the VCO results in a relatively high phase noise at mmWave frequencies. In order to meet the stringent phase noise requirements in space applications, a large loop bandwidth is mandatory in order to filter out VCO phase noise as much as possible. Using several phase-aligned mmWave PLLs would reduce the phase noise at the output of the receiver frontend. In order to achieve a programmable output frequency, the mmWave PLL (array) should be driven by a fractional-N PLL at a moderate frequency. The jitter performance of a hybrid OFDM system using such an architecture was analyzed in [1]. It was shown that the phase noise of the common low-frequency PLL can be reduced by one global pilot tracking loop, while the phase noise of the mmWave PLL array is much reduced due to noise averaging in conjunction with a large PLL bandwidth. A high frequency at the phase detector input was found to be essential for a low jitter of the mmWave PLL, since it allows a large loop bandwidth to be used for VCO phase noise reduction.

This paper presents a robust 28.3-33 GHz integer-N PLL design in a 130 nm SiGe-BiCMOS technology. It describes and compares two different phase detector (PD) versions using MOSFETs or SiGe HBTs, respectively. The first PLL uses high-voltage MOSFETs for the PD design which is limited to a few hundred MHz at the PD input. By contrast, a bipolar PD achieves several GHz. Fig. 1 shows a block diagram of the PLL with a bipolar PD using an input frequency around 2 GHz. A bipolar phase-frequency detector (PFD) followed

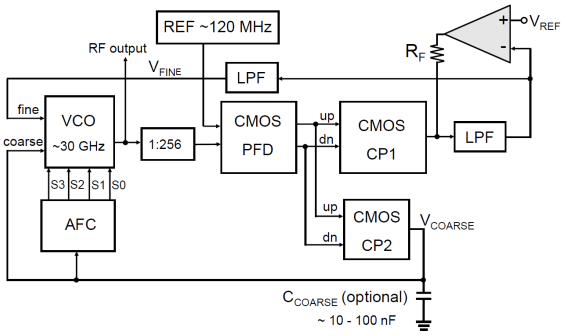

Fig. 1. Block diagram of a dual-loop PLL using a bipolar phase detector.

by an integrated differential bipolar amplifier is employed for a high speed. By using 1:16 frequency dividers, the input frequency to the CMOS PFD is reduced to about 125 MHz, a convenient frequency for the thick-oxide MOSFETs used for CMOS PFD and charge pump.

The coarse tuning voltage is depicted in Fig. 2 together with the fine tuning voltage $V_{\mathrm{FINE}} \approx V_{\mathrm{IN}-}$.

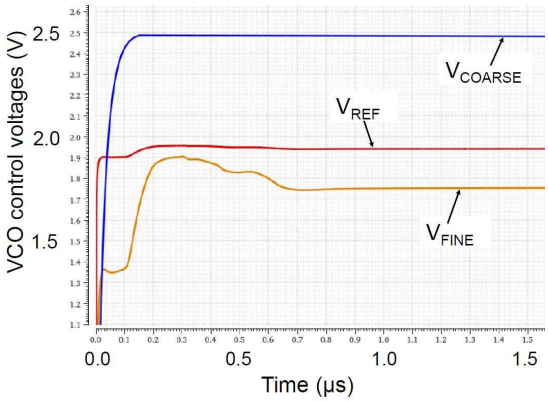

Fig. 2. Transistor-level simulation of VCO tuning voltages during frequency settling.

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Design and Optimization of OTA-C Filters with Shared CMFB and Output Stages: Performance, Power and Area Analysis

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SUMMARY

This paper proposes a novel methodology for optimizing OTA-C filters by incorporating shared common-mode feedback (CMFB) and output stages. The approach aims to minimize power consumption and silicon area without compromising the filter's performance, including frequency response, noise, and distortion. The key innovation lies in decomposing the operational transconductance amplifier (OTA) into modular sub-blocks—specifically input, output, and CMFB stages—that can be reused within a filter structure. This strategy significantly reduces redundancy, enhances integration density, and supports the development of compact analog systems.

Two distinct OTA-C filter architectures were evaluated: a ladder-based filter and a signal-flow-based filter. Each was designed in three configurations: a base model using complete OTA units, a version sharing CMFB circuits among nodes, and a fully optimized variant with shared CMFB and output stages. Through simulations using 45nm CMOS technology, substantial improvements in efficiency were achieved. For the ladder-based design, power consumption was reduced by up to 42.2%, and transistor area by 37.1%. Similar reductions were observed in the signal-flow-based filter, demonstrating the general applicability of the method.

Importantly, these optimizations maintained essential filter characteristics. Despite structural changes, the 3dB cutoff frequency, total harmonic distortion (THD), noise performance, and dynamic range were preserved or improved. To address challenges such as transconductance reduction due to parallel connections in shared output stages, precise tuning of component values, particularly capacitors, was implemented. This compensation ensured stable and accurate filter behavior across varying configurations.

The proposed approach provides a promising direction for analog circuit designers aiming to create energy-efficient, scalable, and high-performance filtering solutions. The modular design strategy is especially beneficial for battery-powered or area-constrained applications, where reducing power draw and chip size are critical. The results validate the effectiveness of using shared sub-blocks in analog filter design and encourage further exploration in similar circuit optimization domains.

TABLE I.
THE DESIGNED VI-TH ORDER FILTERS' SIMULATED PARAMETERS

Measured parameters	Ladder-based OTA-C filter			Signal-flow-based OTA-C filter		
	Full OTA	*Shared CMFB*	*Shared CMFB and output stage*	*Full OTA*	*Shared CMFB*	*Shared CMFB and output stage*
3dB frequency [MHz]	4.504	4.504	4.513	4.512	4.51	4.501
-270° frequency [MHz]	4.489	4.49	4.489	4.492	4.499	4.489
Frequency of 1dB difference from ideal filter [MHz]	142.7	150.6	43.46	295.5	327.5	46.99
Frequency of 1° difference from ideal filter	6.856	6.867	5.139	6.19	10.34	9.654
Input voltage amplitude for 1% THD [mV]	163.28	163.28	179.1	168	168	184
Input referred noise [mV RMS]	5.717	5.717	4.922	5.189	5.131	4.443
Dynamic range [dB]	26.105	26.105	28.209	27.194	27.292	29.333
Power consumption [µW]	1006.74	680.76	582.12	890.5	600.8	513
Transistor area [μm^2]	344.82	279.48	216.84	302.94	244.86	189.18

Design of the Charge-Sampling Multiplying PLL in CMOS 40 nm

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Extended Abstract

One of the very popular PLLs is the subsampling-based architecture that main advantage is creating virtual clock multiplier which allow to avoid amplifying noise originating from charge pump. Also in locked state divider's phase noise is eliminated and power consumptions is lower. Drawback of this solution is necessity of interrupting oscillator output nodes by sampling process. Many approaches have been proposed to minimize such effects, like power gating operations, but still limitations were set by time needed for common mode setting or resonant steady-state time in the case of the LC tank [1, 2].

To overcome the above-mentioned issues, charge integrating phase detector was proposed [3]. Designed as a simple common source stage measures phase error by integrating charge on capacitor during only half time of VCO period. Principles of phase difference detection is presented in Fig. 1, where we can see two scenarios and corresponding detector outputs in locked state and VCO leading case. The negligible detection time (only 0.45% of the total clock reference period) minimize capacitance modulation effect.

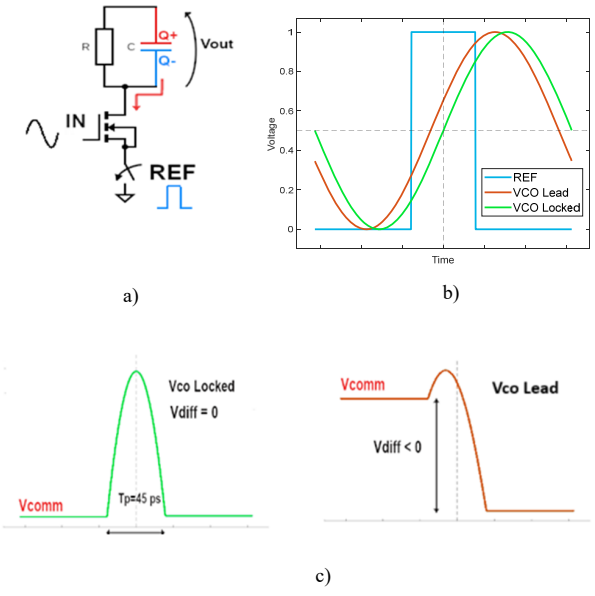

Fig. 1. Phase detection process overview: a) Phase Detector, b) PLL in locked and dislocked state, and c) resulting output voltage.

The charge sampling process is based on integrating current on a capacitance without applying any switches to hold the sampled voltage. The drawback of this solution is the discharging process, with time-constant R_SC_S (impedance of common mode stage), by current flowing in parallel connected resistor (needed to avoid extra origin pole in PLL transfer function). However this disadvantage can be partially alleviated by using high common mode suppressing amplifier, as the ripples appear both on positive and negative PD output. Also choosing differential input VCO additionally suppress this effect. Here folded cascode operational transconductance amplifier (OTA) is used. For further improvement of the common mode gain, the tail current source is cascaded. The OTA is supported with common mode amplifier, as it is illustrated in Fig 2. Native NMOS is pertinent, as just one couple is sufficient in average voltage level block (source follower configuration). With these applications PLL's reference spur power can be lowered below -70 dBc.

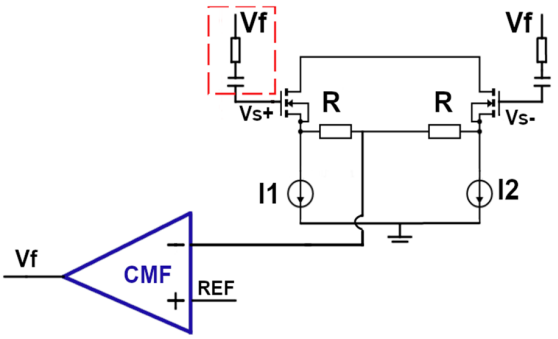

Fig. 2. CMF feedback.

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Enhancing Test-Driven Development for Reconfigurable Hardware through High-Level Synthesis and Early-Stage Validation

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SUMMARY

High-level synthesis tools help engineers deal with the challenges of building complex systems that use reconfigurable technologies. Such serves as a precursor to well-established methods in the software industry, such as Test-Driven Development, in the development process of hardware components of an embedded system. However, the assistance offered by the high-level synthesis validation tools could be strengthened and targeted at the early stages of project development. This paper describes a hardware testing framework as a means to quickly evaluate the capabilities of embedded components using a unit testing paradigm, leading to Test-Driven Development implementation on reconfigurable hardware.

High-Level Synthesis (HLS) has recently gained significant popularity, contributing to the acceleration of FPGA-based development and simplifying the verification process. HLS expands the capabilities of the FPGA market by allowing even users with basic programming knowledge to evaluate available architectural options quickly. FPGA technology is accessible to software engineers and hardware developers. However, HLS does not provide immediate verification of project credibility, which creates particular challenges in the development process.

This paper aims to develop and implement an HLS-based verification framework that leverages the TDD approach to overcome existing challenges in verifying FPGA-based systems. Additionally, this study evaluates the effectiveness of HLS in accelerating FPGA development and improving program verification. The proposed framework is expected to provide
a standardized testing methodology that simplifies FPGA verification while enhancing reliability and reducing time-to-market.

The Test Manager, Device Under Test (DUT), and communication partner are interconnected via AMBA technology, which ensures efficient data transmission. The Test Manager is directly connected to the bus, receiving messages that control the DUT's testing process. It integrates into the development process by delegating data transfer tasks to DDR memory. In this model, test cases provide stimulus data to reserved DDR regions, which the Test Manager reads to configure and trigger the DUT. Subsequently, DUT outputs are written back to DDR, where the Test Manager reads and compares them to predefined reference values.

This paper describes a framework for verifying the Ceedling protocol. This framework aims to develop and implement an HLS-based design verification environment that utilizes a TDD approach to address the current challenges of verifying systems implemented with FPGA technology. Ceedling is a complete package that uses HLS-based hardware component testing to facilitate and improve the design of embedded systems targeting the FPGA platform. The main objectives of this framework include evaluating the effectiveness of HLS in accelerating FPGA-based development, developing a test environment for modeling hardware components, and implementing TDD principles to ensure the correctness of designs. To the best of our knowledge, this is the first study to create an on-board verification environment that can be used throughout the design cycle, regardless of the level of abstraction associated with system specifications. This facilitates the development of the necessary hardware and software components and saves time and effort. In addition, Ceedling allows you to use the TDD method in system design, enabling you to take advantage of the popular software development method. Ceedling supports functional testing and timing testing; this is a new complexity related to the nature of real-time projects and hardware. As a result, the proposed verification framework includes three primary levels of abstraction regarding the specifics of the embedded system (functional, RTL, and implementation/physical). The main contribution of this framework is creating a configurable and standardized test environment for heterogeneous devices, which allows engineers to reduce the amount of testing and accelerate the path to FPGA implementation. After all, automatic generation makes this proposition accessible and straightforward for software and hardware developers, who do not need extra effort to use it quickly.

FSMLock: Sequential Logic Locking Case Study

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SUMMARY

FSMLock is a sequential logic locking technique that has been proposed for protection of intellectual property (IP) of finite state machine (FSM) circuits. FSMLock is applied to a sequential circuit by abstracting a flattened version of its distinct state entry table (SET) into a binary data file, which can then be encrypted and stored in non-volatile memory. The encrypted flattened state entry table (FSET) representation is read in partitions such that, at run-time, only a subset of the sequential logic is in scope. A high level architecture of the FSMLock is illustrated in Figure 1. While this technique provides security advantages over other sequential logic locking techniques, one major drawback it brings is the large amount of memory required for storing data of all states, transitions, and outputs. Finite state machines with input multiplexing (FSMIM) is an optimization methodology and tool set that was proposed for efficient mapping of FSMs into memory. This is primarily achieved by reducing the number of effective inputs to the FSM, and converting it from Moore's to Mealy's machine for minimizing the number of states. This paper discusses our work on integrating these two techniques in a practical case study of converting an existing state machine into an implementation using FSMLock with input multiplexing.

The state machine used in this case study has 55 states, 71 transitions, 45 inputs and 63 outputs, and its behavior was originally modeled in Verilog HDL. We analyzed configurations with one partition, where the entire state machine would fit into Scoped FSET memory, with two partitions, and with four partitions. The memory based architecture together with the original model were simulated in a VHDL test bench in order to ensure that functionality of the original FSM was preserved. The hardware tests were conducted on a Digilent Nexys4 development board with an Artix 7 100T FPGA

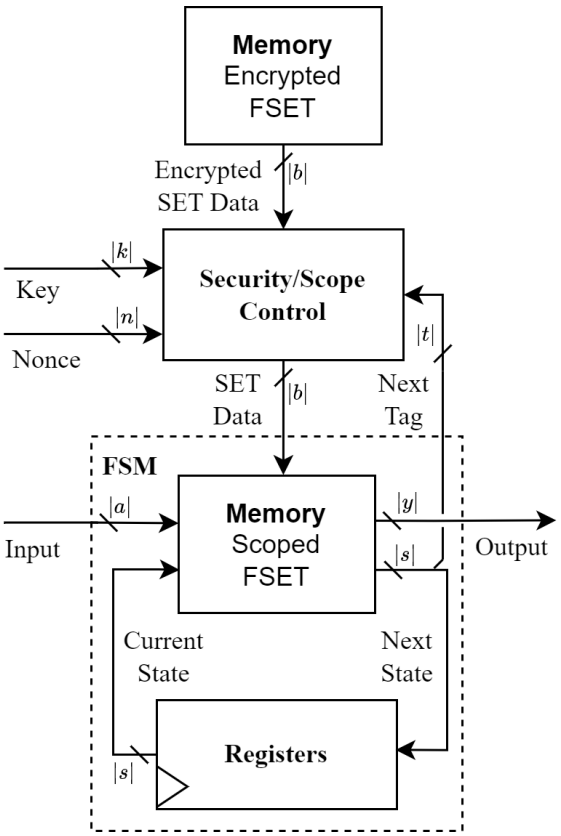

Fig. 1. The FSMLock primitive.

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Implementation of a PLL Loop Circuit for Frequency Synthesis in 65 nm CMOS Technology

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***Abstract*—This paper presents the design and implementation of a phase-locked loop (PLL) circuit in 65 nm CMOS technology, dedicated to frequency synthesis and multiplication in radio frequency (RF) applications. The circuit processes an input signal of 13.56 MHz and generates a multiplied output signal of 867.84 MHz in the ultra high frequency (UHF) band, making it suitable for short-range communication systems such as radio-frequency identification (RFID) and near-field communication (NFC). The circuit was designed to ensure low phase noise, frequency stability, and fast locking time. The results demonstrate the feasibility of the proposed PLL architecture for modern wireless communication systems, highlighting its potential for integration into advanced RF applications.**

***Keywords*—VLSI, IC, PLL, phase-locked loop, CMOS, NFC, RFID, RF, HF, UHF, phase noise, stability.**

SUMMARY

The paper presents a complete design flow and performance analysis of a Phase-Locked Loop (PLL) system implemented in 65 nm CMOS technology, intended for use in short-range RF communication applications such as radio-frequency identification (RFID) and near-field communication (NFC).

Section I introduces the motivation and use cases for PLLs in modern RF systems, discussing their essential role in precise frequency synthesis for reliable data transmission. Section II provides a theoretical foundation by presenting a linearized model in the Laplace domain, defining key parameters like loop gain, and stability considerations. The use of Integer-N architecture is analysed and justified based on its influence on the transfer function.

Section III details the design process of individual PLL blocks. The PFD and charge pump are implemented in a configuration that ensures accurate phase and frequency error detection. A wide-swing cascode current mirror is used to achieve wide output voltage range and maintain current matching across PVT variations. The VCO is implemented as a current-starved ring oscillator with seven stages, incorporating Schmitt triggers for enhanced noise immunity and output stability. The third-order passive loop filter stabilizes the loop response, balancing responsiveness and stability. The frequency divider, implemented using six D flip-flops, provides the necessary frequency division factor of 64 and ensures synchronization between the PLL input (13.56 MHz) and the divider's output. Additionally, a 27.12 MHz clock signal, twice the reference frequency, can be potentially extracted from the second-to-last divider stage for potential NFC digital circuit applications.

Section IV discusses the verification and simulation results, including phase noise analysis, system stability evaluation, settling time measurements and current consumption under various process corners. The worst-case settling time is approximately 30 µs, and phase noise performance remains under -100 dBc/Hz at 10 MHz offset. Simulation results confirm that the PLL achieves fast synchronization within 50 µs, ensuring compliance with the ISO/IEC 14443 standard. The design demonstrates stable operation across various PVT conditions.

Section V concludes with a summary of the results and highlights directions for future research to further enhance the PLL's efficiency and performance. These include potential gain stabilization techniques for the VCO - improvements such as dynamic charge pump current scaling and digitally controlled filter trimming to enhance loop adaptability and robustness in changing environmental conditions.

Beyond the technical aspects, this study underscores the relevance of PLL-based frequency synthesis in modern communication technologies, where signal accuracy and stability are crucial. The proposed architecture balances performance, efficiency, and integration feasibility, making it a compelling candidate for next-generation wireless applications. Further research will explore circuit optimizations to enhance power efficiency and improve performance under extreme operating conditions.

These results highlight the feasibility of the proposed PLL for integration into modern wireless communication systems, offering a compact and efficient solution for high-frequency signal generation. The findings presented in this work contribute to ongoing advancements in RF circuit design, paving the way for more efficient and reliable frequency synthesis techniques.

Optimum Design of a Mostly-Digital Fleischer-Laker Switched-Capacitor Bilinear Bandpass Filter in Standard CMOS Technology

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Extended Abstract

This paper presents a Fleischer-Laker switched-capacitor (SC) bilinear bandpass filter implemented using an inverter-based amplifier. Due to the generalized scaling used in advanced deep-submicron CMOS technology over the past decades, it is becoming increasingly more difficult to design high-gain high-bandwidth opamps, due to the reduction of the supply voltage and of the intrinsic gain of the transistors. Since the amplifier used is implemented using inverters, it can take advantage of the improved transistor performance in smaller nodes, which is mainly exploited by digital circuits.

A. Bilinear Bandpass Fleischer-Laker SC filter

The bilinear bandpass SC filter circuit, shown in Fig. 1, is based on the Fleischer–Laker architecture [1].

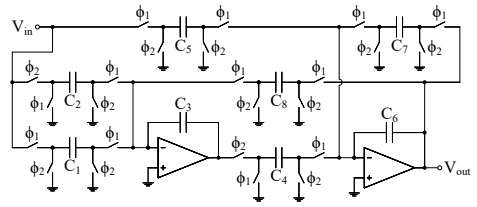


Fig. 1. Bilinear bandpass Fleischer-Laker SC filter.

Considering that the output signal is sampled at the end of clock phase ϕ_2, that the input signal only changes value once per clock period ($1/F_s$) and if $C_1 = C_2 = C_5$ and $C_3 = C_4 = C_6$, the Fleischer-Laker SC filter's transfer function is given by (1) and have a bilinear type response.

$$H_{bp}^{\phi_2}(z) = \frac{C_1(z+1)(z-1)}{C_3(z-1)^2 + (C_7(z-1) + C_8)z} \qquad (1)$$

B. Inverter-based Amplifier

The amplifiers used in the Fleischer-Laker SC filter have been implemented using a three-stage inverter-based architecture [2], [3], which is shown in Fig. 2.

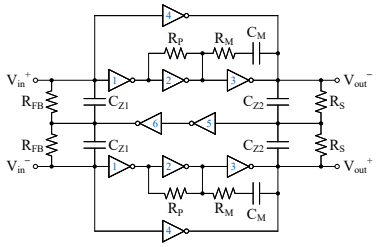
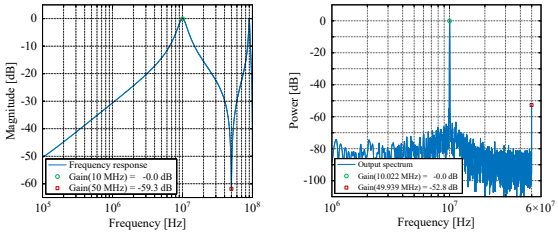


Fig. 2. Three-stage pseudo-differential inverter-based amplifier [2], [3].

C. Simulation Results

The filter circuit was designed in a 28-nm bulk-CMOS technology, using a supply voltage of 0.9 V and a clock frequency of 100 MHz. Simulation results show that the filter's central frequency is approximately 10 MHz, with a gain of 0 dB, and a quality factor of 10/3. The amplifiers have a typical gain of 42.5 dB, the SC filter has a SNR of 54.4 dB, an IM3 of -63.6 dB, and the circuit's total power dissipation is 2.5 mW.

The resulting frequency response and output spectrum of the bilinear bandpass SC filter are shown in Fig. 3. Results from the filter's impulse response show a notch depth at $F_s/2$ of -59.3 dB, while the transient simulation using an input signal with two 100 mV tones has a depth of -52.8 dB.



(a) Frequency response (b) Normalized output spectrum

Fig. 3. Bilinear bandpass Fleischer-Laker SC filter: (a) Frequency response, (b) Normalized output spectrum for an input with two 100 mV tones.

The bilinear bandpass SC filter was also tested under 12 different process, voltage, and temperature (PVT) corners (TT/FF/SS, $V_{DD}\pm5\,\%\,V_{DD}$, 0°/85°) and under 100 Monte Carlo (MC) cases of mismatch variations, the performance obtained from these two tests is summarized in Table I.

TABLE I
PERFORMANCE UNDER PVT CORNERS AND MISMATCH VARIATIONS.

		Impulse response performance				Transient performance			
		f_c [MHz]	$G_{f_{sl}}$ [dB]	G_{f_c} [dB]	$G_{f_{sh}}$ [dB]	SNR [dB]	THD [dB]	IM3 [dB]	$G_{f_{sh}}$ [dB]
Nom.		10.00	-50.89	0.03	-59.16	54.38	-80.56	-63.58	-52.75
MC	μ	9.97	-49.70	0.01	-60.81	53.74	-77.14	-63.53	-52.81
MC	σ	0.03	1.42	0.04	1.38	0.08	3.21	2.49	0.13
PVT	μ	9.94	-50.27	-0.02	-60.02	53.91	-72.71	-57.46	-52.41
PVT	σ	0.16	0.65	0.59	4.28	0.97	11.35	12.78	4.64

f_{sl} – lower stopband frequency (0.1 MHz), f_{sh} – higher stopband frequency (49.939 MHz)

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Practical Implementation of Voltage-to-Current and Current-to-Voltage Converter in High Voltage SOI Technology

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EXTENDED ABSTRACT

This paper presents an introduction to the analysis of a circuit that can serve as both a voltage-to-current and current to voltage converter. This circuit enables transitions between low-voltage and high voltage ranges of analog signal processing and can produce two counterphase waveforms. The analysis includes the schematic of the circuit, the schematic equipped with overvoltage protection device set and the full layout of the latter schematic version. The consecutive design steps show a degradation in the quality of circuit operation. These changes are presented in relation to the change of selected operation parameters.

Basic circuits that share the same mode of operation (Fig. 1) were first introduced as designed in SmartIs 0.8 µm SOI (Silicon on Insulator) process by Atmel [1] (later developed into TeleSmart 0.8 µm by Telefunken). Another implementation was attempted with the H35B4 0.35 µm process by AMS and finally the most complete one with XDM 1.0 µm SOI by XFAB. This design has reached the furthest stage of advancement with a full layout with post-layout extraction.

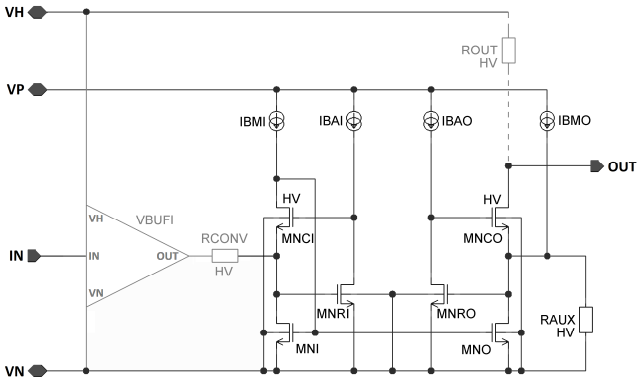

Fig. 1. Operation mode of the circuit discussed.

The presented results for the final version of the converter design show that the influence of the SOA related devices is very limited in comparison to the operation deterioration caused by the laying out the protected schematic (Fig. 2). Parameters such as THD or oscillations of the summed output signals are comparable or better in case of the final layout only outside its bandwidth.

Very similar operation quality for both versions of the schematic (original and protected) opposed by significantly deteriorated operation of the final layout is consistent with results obtained for the already published analysis results for the HV unity-gain buffer and trapezoidal waveform generator [2], both designed as components of a wider set of HV current-mode-based function blocks.

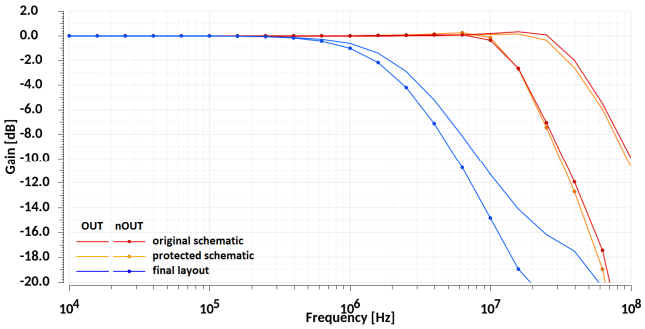

Fig. 2. Small signal AC simulations of gain vs. frequency for all three stages of the converter design.

The presented analysis can be considered as an introductory part to the wider study of application possibilities of the discussed function blocks, including a comparative analysis with implementations in different HV technology processes.

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Recording Channel Parameters Influence Analysis on Time-Related X-ray Based Measurements in CMOS 40 nm

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***Abstract*—This paper describes the influence analysis of typical detector readout electronics front-end parameters on time-related X-ray based measurements. Here two types of recordings are considered, i.e. the Time over Threshold (ToT) and Time of Arrival (ToA) used for energy and arrival time measurements of incoming particles, respectively. The electronics considered is composed of the core amplifier based on a folded cascode amplifier and the feedback circuit based on the constant current architecture. The recorded channel presented is designed in the CMOS 40nm process. This work provides information on how the precision of time-related measurement depends on the front-end electronics.**

***Keywords*—X-ray detectors, readout electronics, time measurements, ToT, ToA, CSA, folded cascode, constant current feedback**

I. Introduction

X-ray-based imaging cameras are a crucial part of medicine, physics, and industry that allow inspection of the interior of visualised objects without mechanical damage [1, 2]. Contemporary, these are often hybrid pixel detectors (HPDs) that are composed of two pixel-shaped bump-bonded structures, i.e. the detector and the electronic chip. Typically, the purpose of the HPD recording channel is to convert a current pulse, which is a result of charge generated by the impinging into the detector volume photon, into a voltage pulse. The voltage pulse may then be used to extract information regarding the photon energy, its arrival time, or hitting region. The main block of a processing chain is a Charge Sensitive Amplifier (CSA) whose function is to generate an output signal proportional to the input charge collected from the detector; this can be interpreted as current signal integration. Taking into account that the detector signal is a current pulse of amplitude proportional to the energy carried by the photon and is further processed by the transimpedance amplifier, it could be assumed that the CSA output voltage signal is also proportional to the energy of that photon.

Classically, the recording chain is composed of a shaper circuit (preceded by the CSA) to improve the signal-to-noise ratio of the recorded data and analogue-to-digital converter (ADC) for converting analogue signal into digital signal. However, mainly due to the pixel size and its power consumption limits, it is very difficult to use the shaper and ADC in a single pixel. A very attractive alternative is a time-based measurement that provides many advantages, especially when considering modern processes. The time-based method allows one to evaluate the energy carried by the photon hitting detector by measuring the time that the voltage pulse (related to the energy of the particle) exceeds over the set threshold (Time-over-Threshold, ToT). Also, this approach enables the possibility of measuring the time of hitting the detector by the particle (Time-of-Arrival, ToA) especially important when the particle track needs to be found. A conceptual description of this approach is presented in Fig. 1.

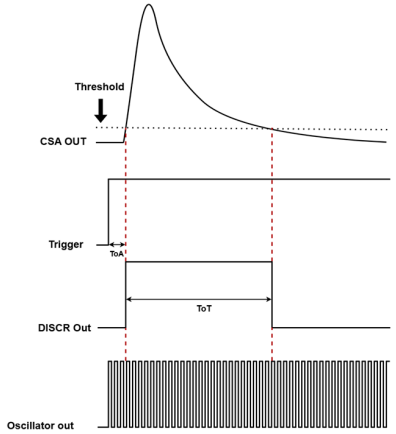

Fig. 1. The conceptual idea of ToT and ToA measurements.

A typical circuit used to measure ToT and ToA, similarly to the classical approach with an ADC, contains a CSA circuit and a discriminator (see Fig. 2). The role of the discriminator is to notify whether the output CSA signal exceeded a preset threshold (this also allows to differentiate among pulses of different energies and to separate them from noise). Whenever the discriminator registers the pulse crossing its threshold, the following actions take place: in the case of ToA the counter is stopped preserving the value proportional to the chip reference clock period, while in the case of ToT the counter is started until the signal amplitude falls below the set threshold.

In this paper, the particular blocks of the recording channel (see Fig. 2) are analysed in terms of their influence on the ToT and ToA measurement.

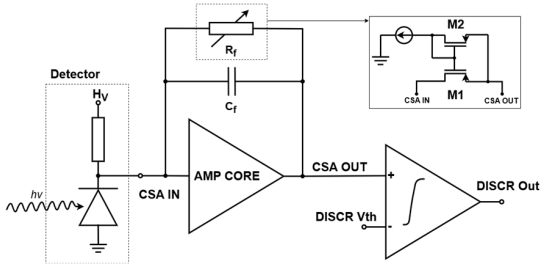

Fig. 2. Schematic diagram of a typical ToT/ToA measurement circuit.

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SHA-256 Hash Generator in Verilog HDL

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***Abstract*—An implementation of SHA-256 hash generator is presented. A block has been described in Verilog HDL. A generator code is written with basic logical and arithmetic operations to create a easily-synthesizable block. A design process a 512-bit block in 67 cycles. The generator is tested in simulations with the test vectors and reference digests published by NIST. The simulation testbench has been designed in SystemVerilog. The design passed all test cases used.**

***Keywords*—hash function, SHA-256, HDL, Verilog.**

Extended Abstract

A SHA-256 is one of the SHA-2 hash function family participant published by U.S. National Institute of Standards and Technology (NIST). Thanks to the hardware implementation of this cryptographic function, the compatibility of uploading software, transactions, etc. can be checked.The SHA-256 generator block is designed in Verilog HDL using the SHA-256 hash function. Generator after serving on the data input to be hashed and the length of the message binary record returns to output *hash* with a length of 32 bytes (256 bits).

The generator is created with 21 interconnected submodules that execute appropriate logical and arithmetic operations (like XOR, OR, AND, bit-shift, +, etc.) that control and operate the course of subsequent rounds across the algorithm. The built-in controller controls the block submodules in compliance with the *FIPS 180-4* standard. The entire block is resetable by asynchoronous *RESET* input.

The generator starts processing at the rising edge of *CLK* when the *FLAG_IN* flag is raised. It confirms that 512-bit (one chunk) of input data *MESSAGE* and 64-bit input data length were sent. Immediately, the number of 512-bit data blocks is computed by division of *MESSAGE_LENGTH* by $2^9 = 512$ (realized by the 9-bit shift). This *OUT_CHUNK* output value is needed by the controller to control how many of the chunks the generator needs to compute.

Preprocessing step is split into two steps, Parsing and Padding. We decided to implement the parsing step in software, but the padding inside hardware implementation. The preparation of data and padding is done within three clock cycles, but the padding itself is done in one clock cycle. However, these steps are rather complex since these require e.g. bit rotation by variable bit number.

Our preliminary synthesis and static timing analysis (STA) tests with several CMOS standard libraries shown that the critical path is mostly hidden in padding operation. This issue needs further investigations, but we see two potential approaches to deal with it:

- pipelining the operation in preprocessing;
- move the preprocessing operations to the software domain.

Main SHA256 loop block strictly follows the *FIPS 180-4* standard. Since the SHA-256 algorithm is designed with simple arithmetic and logical operations (AND, OR, ROTR, etc.), the implementation in any HDL is rather straightforward.

After the preprocessing, the following operations are performed

- $H_{0:7}^{(0)}$ values initialization;
- $W_t^{(i)}$ message schedule preparation;
- main compression loop;
- intermediate hash $H_{0:7}^{(i)}$ update;

After processing a 512-bit block, the intermediate hash values are used in the next round (with latter 512-bit data block). When the entire message is processed, the final 8 32-bit hash values are concatenated to the final 256-bit output hash value. Simultaneously, the output flag *FLAG_OUT* is raised, indicating the end of the calculations. Now the outer system can collect the output hash. The generator computes one 512-bit chunk of data in 67 clock cycles.

The generator tests start with reading all test vectors from the text files provided by *NIST*.

Then, these vectors are transmitted to the *MESSAGE* input, and the length of their binary notation to the *MESSAGE_-LENGTH* input. After the calculations, the testbench save the generator's output hash value. After that, the calculated hash is compared to the reference hash *MD (Message Digest)*. If the hashes are the same, the *SUCCESS* message is written in the log file. Otherwise, the *ERROR* message is written in the log file. The project can be extended by adding the standard interface (such as Wishbone or AXI4-Lite) to improve the adaptability to microprocessor architecture and verify a design on an FPGA platform to perform experimental tests.

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SYNAPSE - A New Approach to Semi-automated Design of Ultra-low-power Application-specific Embedded Processors

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EXTENDED ABSTRACT

Application-Specific Embedded Processors (ASEPs) provide critical cybersecurity resilience and power efficiency for embedded systems. However, they use customised instruction sets which lack standardised toolchain support, necessitating manual design by specialised engineers. The growing demand for ASEPs in medical, industrial, and smart grid applications, driven by their advantages over general-purpose processors, underscores the urgency for automation. This paper proposes SYNAPSE, a semi-automated framework that combines architectural libraries with optimization methods to synthesise hardware-software co-designed ASEPs. This addresses scalability barriers while maintaining domain-specific performance benefits.

SYNAPSE generates multiple processor designs optimized for either power or performance, depending on the configuration data provided, as illustrated in Figure 1. The core process automates the generation and verification of both the hardware and software components of ASEPs, diverging from classical High-Level Synthesis (HLS), which focuses on dedicated hardware controllers. The tool constructs datapaths using combinatorial variations from its architectural library to produce both picoRISC-based ASEPs and No Instruction Set Computers (NISCs) for comparative analysis. While NISCs replace instruction memory with direct control word storage, ASEPs retain instruction decoders, which theoretically favors memory efficiency for larger programs. In our case study, ASEP designs showed marginally smaller memory footprints, though program sizes were insufficient to demonstrate this advantage fully.

The case study demonstrates the automated ASEPs synthesis for image affine transformation processing 8-bit pixel streams. Experimental comparisons show that SYNAPSE-generated ASEPs, such as picoRISC '1011', achieve size reduction of over an order of magnitude compared to RISC-V and NIOS-based processors. This is enabled by the customisation of the architecture and instruction set for a specific application. Although general-purpose processors use accessible compiler toolchains, our automation approach significantly reduces the need for manual design expertise. These results validate the feasibility of task-tailored automation for the development of scalable embedded systems.

The proposed semi-automated approach combines preconfigured architectural libraries with parallelizable optimization methods to synthesise ASEPs, replacing manual hardware-software co-design with automated generation and verification. Future work will expand the proposed method to generate more design variants and adapt them to more specific applications, thereby improving the versatility of the proposed approach. This methodology shows potential for integration with AI/ML techniques in the future to further leverage expert knowledge in design automation.

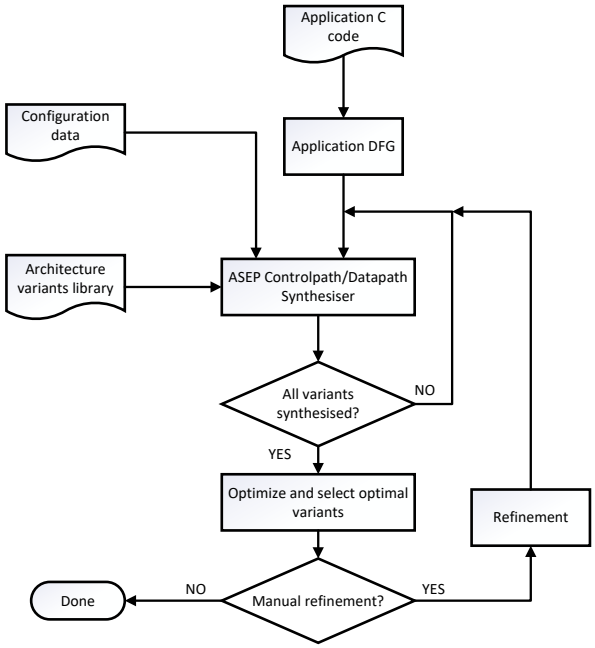

Fig. 1. SYNAPSE ASEP generation flow

Analysis and Modelling of ICs and Microsystems

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Fractional Spurious Tones Analysis of the Space-Time Averaging PLL

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***Abstract*—This paper presents a step-by-step process for modeling and analyzing the Space-Time Averaging Phase-Locked Loop architecture, which significantly reduces the quantization error caused by fractional division. The analysis focuses primarily on the reduction of spurious fractional tones.**

***Keywords*—fractional spurious tones, fractional phase-locked loop, space-time averaging, quantization error.**

I. Introduction

Phase-locked loops (PLLs) play a critical role in modern systems, satisfying various requirements depending on the application. Conventional Time-Averaging PLLs (TA PLLs) use a Delta-Sigma Modulator (DSM) to alternate between integer division ratios, enabling fractional frequency synthesis through time averaging. However, this method introduces quantization noise that manifests as undesirable spectral components. The Space-Time Averaging PLL (STA PLL) mitigates these issues by introducing spatial averaging.

II. STA PLL Architecture

The STA PLL uses an array of frequency dividers (N-DIVs), phase-frequency detectors (PFDs), and charge pumps (CPs) operating in parallel (Fig. 1) to achieve instantaneous fractional division ratios. For instance, to obtain a 3.25 division ratio, three dividers divide by 3 and one by 4, resulting in the desired output frequency. The STA PLL also supports arbitrary fractional division ratios by combining spatial and time averaging, enabling precise fractional frequency synthesis with significantly reduced quantization noise.

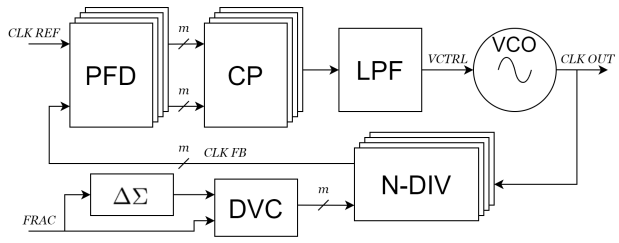

Fig. 1. STA PLL architecture.

III. Design Methodology

Before starting the design, the simulation strategy must be carefully planned. Simulating PLL is a time-consuming process, so only the phase-frequency detector, charge pump, and low-pass filter are modeled at the circuit level using TSMC 40nm CMOS technology to preserve loop dynamics. The other components are implemented in Verilog-A to speed up the simulation. The main focus is on designing transistor-level models and the divider vector controller (DVC) algorithm that is responsible for adjusting the divider values.

IV. Simulation Results

Due to the nature of fractional PLLs loop dynamics, PSS analysis is unsuitable [2], so transient simulation combined with Discrete Fourier Transform (DFT) is used to analyze the output frequency spectrum. The DFT output (Fig. 2) shows that the STA PLL achieves significantly lower spur levels and reduced frequency fluctuation compared to that of the TA PLL.

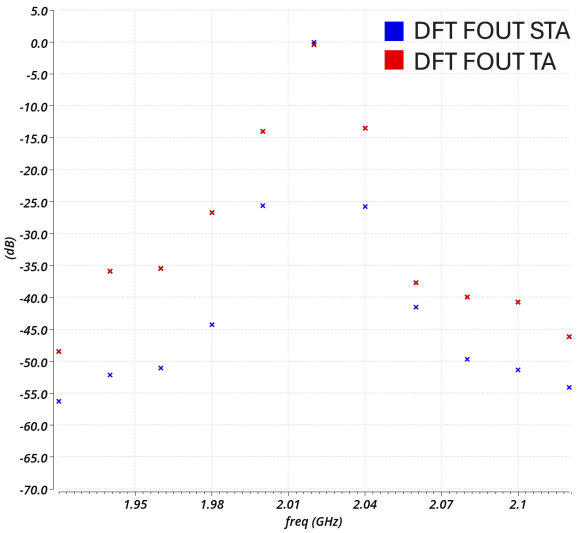

Fig. 2. DFT of STA and TA PLL output signal for 20.2 division ratio.

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High-Level Modeling of RF Power Amplifiers and Antenna Arrays for Efficient Over-the-Air Power Combination in RF Transceivers

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SUMMARY

Efficient RF amplification and power combination are key challenges in 5G/6G transceivers. In particular, Power Amplifier (PA) designs have to balance linearity and efficiency requirements to accommodate high Peak-to-Average Power Ratio (PAPR) waveforms, and power combining networks such as Wilkinson combiners introduce insertion losses, limiting the achievable energy efficiency of the RF Front-End (RFFE). This work explores Power Combination Over-the-Air (PCOA), where four sinusoidal components are individually amplified by an RF PA operating at near saturation, driving a 4×4 patch antenna array. Though beamforming, the components are spatially power combined, in the far-field. PCOA allows more efficient PAs to be used, reduces interference to other systems, and avoids circuit-based power combiner disadvantages. A high-level system model, Fig. 1, is developed to analyse the influence of per-component power control, PA sizing, and antenna array configuration on PCOA efficiency and directivity. Nonidealities such as noise, PA distortion, impedance mismatches, path loss, and mutual coupling are considered, providing insights into optimal PA output power levels, beamforming strategies, and array design trade-offs. Simulation results show that PCOA is well adapted to beamforming, Fig. 2, decreasing RFFE losses, making it a promising technique for next-generation transceivers.

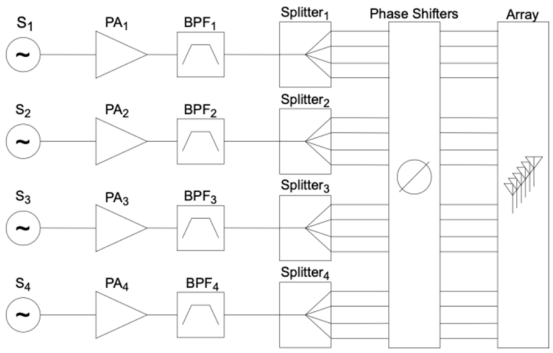
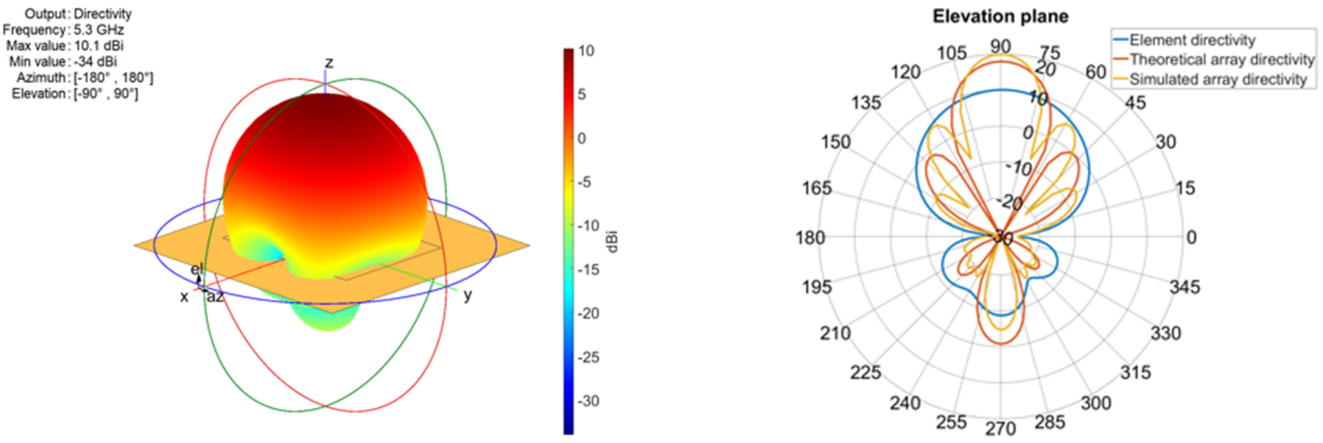


Fig. 1. Simplified transmitter block diagram.



a) b)

Fig. 2. a) Isolated Element directivity and b) array directivity-

Reliability Analyses of Ultra-Low Voltage Analog Spiking Neurons

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Extended Abstract

In recent years, a lot of developments have been made in the field of neuromorphic engineering towards time-based architectures such as Spiking Neural Networks (SNN) to overcome the limitations reached by Moore's law [1]. The neurons, fundamentals elements constituting these SNNs, must be optimized with regards to area, speed and most importantly energy consumption to accommodate for their large-scale integration or specific low-power applications. CMOS-based analog neurons approximating the Morris-Lecar (ML) mathematical model (Fig. 1.a) offer an interesting trade-off between energy efficiency and biophysical plausibility [2].

In this work, SPICE simulations of the compact circuit proposed in [3] are carried out to analyse its behaviour under ultra-low voltage. We observe a severe degradation of the typical spike characteristics (Fig. 1.b) that we try to quantify with the use of several metrics such as the peak-to-peak amplitude of the membrane voltage (V_m), its period and the spike rising/falling times.

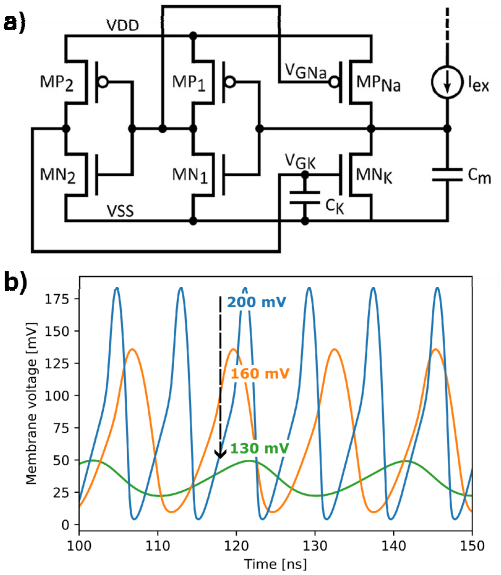

Fig. 1. a) Compact analog neuron design based on the Morris-Lecar model, from [3]. b) Membrane voltage of a simplified ML analog neuron under different ultra-low supply voltages.

These figures of merit allow us to determine, for different excitation currents, a minimum supply voltage ($V_{DD,min}$) below which the amplitude of V_m becomes lower than the neuron inverter switching voltages (V_{switch}), making the circuit unable to properly drive other devices. A severe degradation of the biophysically-plausible spike shape is also observed with the help of the two time-based metrics, negating one of the main advantages of ML-based neurons.

To estimate the functionality of a prospective SNN under ultra-low voltage, we perform variability analyses on the neuron circuit with Monte Carlo simulations. We present the simulated distribution of the normalized spike amplitude and observe significant shifts from the nominal values at lower supply voltages, demonstrating the high variability and instability of the analog neuron operating in deep subthreshold regime.

Using the previously defined minimum voltage limit $V_{DD,min}$, a neuronal failure probability is presented for supply voltage values between 100 and 200 mV and it shows the rapid decrease in functioning neurons under voltages lower than 200 mV, which can prove to be a problem with regards to SNN classifying accuracy [4]. These findings highlight the importance of carrying out thorough stability and robustness analyses for analog neurons operating in subthreshold regimes.

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Power Electronics

Book of Abstracts of the 32nd International Conference *"Mixed Design of Integrated Circuits and Systems"*
June 26-27, 2025, Szczecin, Poland

A Thermal Behavior of Lateral (VESTIC) BJTs on SOI Substrate

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***Abstract*—This paper analyzes the thermal behavior of lateral (Vertical Slit Transistor Integrated Circuits, VESTIC) and vertical BJTs on SOI substrates, focusing on self-heating effects, heat dissipation mechanisms, and thermal stability. The buried oxide (BOX) layer in SOI significantly impacts heat flow, leading to localized hot spots in vertical BJTs and more distributed heating in lateral BJTs. Using numerical simulations and experimental data, we evaluate thermal management strategies and their implications for complementary bipolar logic (CBip). The findings highlight the need for optimized device layouts and biasing techniques to mitigate self-heating, ensuring stable and efficient operation of SOI-based bipolar circuits.**

***Keywords*—lateral BJT; VESTIC; SOI; self-heating; thermal management**

SUMMARY

This paper investigates the thermal behavior of lateral bipolar junction transistors (BJTs), specifically those fabricated using VESTIC (Vertical Slit Transistor Integrated Circuit) technology, on silicon-on-insulator (SOI) substrates. The study contrasts lateral BJTs with traditional vertical BJTs, emphasizing self-heating effects, heat dissipation mechanisms, and implications for logic circuit stability and performance.

The unique geometry of lateral BJTs—where current flows parallel to the wafer surface—results in a more distributed heat generation profile compared to the localized hot spots observed in vertical BJTs. On SOI substrates, the buried oxide (BOX) layer inhibits vertical heat conduction, making lateral heat spreading a critical pathway. This limitation accentuates the importance of thermal-aware design techniques such as layout optimization, the use of pillar metal contacts (acting as thermal vias), and careful biasing strategies to mitigate thermal runaway.

The analysis draws on experimental data, electrothermal simulations, and literature comparisons, indicating that lateral BJTs, particularly the VES-BJT design, offer superior thermal behavior for certain applications due to their planar heat dissipation characteristics. Furthermore, the work explores thermally stabilized complementary bipolar logic (CBip), which employs matched NPN and PNP lateral BJTs on SOI for CMOS-like operation. Proper thermal management, including resistive biasing and circuit-level stabilization, allows these logic gates to function reliably and adapt their performance based on operating conditions.

Ultimately, the paper positions VESTIC-based lateral BJTs as a compelling technology for energy-efficient, high-speed bipolar logic, with thermal behavior as both a challenge and a design lever. The findings open opportunities for hybrid logic architectures combining bipolar speed with CMOS-like control.

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Considerations on the Importance of Proper Modeling of Heat Transfer Coefficient Values

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SUMMARY

Thermal analysis of electronic circuits is an essential part of the design process because thermal issues are the major cause of malfunctions and failures. The temperature field is modeled by the Fourier heat equation. Most engineers consider thermal model parameters, such as thermal conductivity or heat transfer coefficient, independent from temperature, but in reality these quantities depend on temperature.

This problem is described in this paper based on the results of temperature simulations carried out for a test structure using the analytical Green's function thermal solver. This structure resembles a real electronic power circuit manufactured in a thin substrate of high thermal conductivity. It has the dimensions of 10 cm x 10 cm x 1.5 mm and it contains a 1 cm x 1 cm square heat source, whose location is varied during simulations along the circuit diagonal, as indicated in Fig. 1.

The structure is cooled by natural convection and generated heat is exchanged with ambient at its surfaces, what is modeled by the heat exchange coefficient reflecting two mechanisms: radiation and convection. The radiation occurs always when surface temperature is higher than the absolute zero, whereas the convection appears only when there exists a temperature difference between a surface and surrounding ambient. Since the cooling mechanisms mostly occur at the same time, they are represented in thermal models by a single value of the total heat transfer coefficient h_t, which is the sum of the radiation coefficient h_r and the convection one h_c.

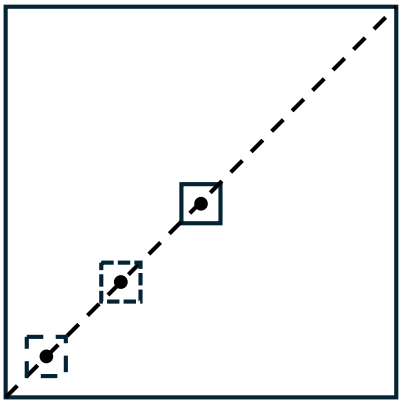

Fig. 1. Test structure layout indicating the locations of heat source and the temperature profile line along the diagonal.

The first component, as visible in (1), depends on surface absolute temperature T and ambient absolute temperature T_a. On the other hand, the latter component is proportional to the surface temperature rise over the ambient ΔT, as shown in (2). According to these equations, for ambient temperature of 20 °C the value of the total heat transfer coefficient increases rapidly, mainly due to the variation of the convective component, from just 5.7 W/(m^2 K) at the ambient temperature to 22.2 W/(m^2 K) when the surface temperature rise equals 100 K.

$$h_r = \sigma * (T + T_a) * (T^2 + T_a{}^2) \tag{1}$$

$$h_c = a * \Delta T^{0.25} \tag{2}$$

The simulation results in Fig. 2 represent the temperature profiles along the test structure diagonal computed for 20 W of power dissipated in the source placed in different locations, the center, the corner and the intermediated middle one, either with the constant heat transfer coefficient value of 10 W/(m^2 K) (lighter lines) or the variable one (black lines). As can be seen, the heat source temperature rise values predicted by the thermal model with the variable coefficient are significantly lower than in the case when the heat transfer coefficient value is constant. Moreover, the temperature differences are visibly reduced then. Furthermore, the source temperature increases when the source is placed closer to structure edges.

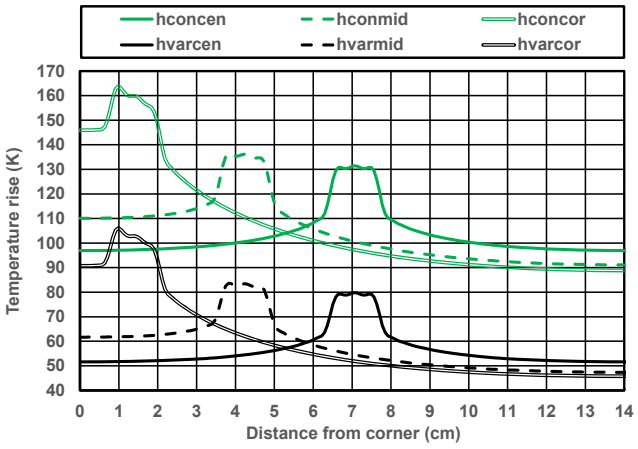

Fig. 2. Simulated temperature rise profiles with constant and variable heat transfer coefficient values for heat source in different locations.

Influence of the Cooling System on Characteristics of Power LEDs in COB Packages

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EXTENDED ABSTRACT

Power LEDs are a basic component of modern lighting systems. They usually contain many diode chips mounted on a common substrate and emitting a desired luminous flux value. COB (Chip on Board) devices contain many diode chips placed on a common ceramic substrate, connected in series-parallel and covered with a common phosphor layer.

Despite the big number of papers on the study of power LEDs in COB packages, there is still a lack of information in the literature on the study of non-isothermal characteristics of these devices obtained at different cooling conditions.

The aim of this paper is to present the results of experimental studies illustrating the effect of self-heating on the electrical characteristics and optical and radiometric parameters of power LEDs in COB packages. Two components with different sizes and different permissible values of forward current were selected for the studies. Devices operating under different cooling conditions were considered.

Two power LEDs in COB packages manufactured by Cree were selected for the tests: CXB2540-0000-000N0ZU4L5A (hereinafter referred to as CXB2540) and CXB1507-0000-000F0ZG2L5A (hereinafter referred to as CXB1507). Both devices under consideration are characterized by the same value of correlated colour temperature CCT = 4000 K and colour rendering index CRI = 95. The CXB2540 diode allows to obtain more than 5 times higher luminous flux, 3 times higher forward current and 2 times higher forward voltage.

The tested diodes differ in the size of the substrate. They are 16x16 mm for the CXB1507F diode and 24x24 mm for the CXB2540 diode. Diode chips are mounted in a circle with a diameter of 9 and 19 mm, respectively. The CXB1507F diode contains 24 semiconductor chips connected in 4 parallel chains of 6 chips each. In turn, the CXB2540 diode contains 120 semiconductor chips connected in 10 parallel chains of 12 chips each. The ceramic substrate of each of the tested diodes is 1 mm thick.

The measurements were performed for three variants of the cooling system of the tested diodes. In the first one, the tested diodes operated without any additional cooling system. In the second variant, the diodes were attached to an aluminum heat-sink with dimensions of 175 x 118 x 10 mm. In the third variant, the diodes were placed on a coldplate with dimensions of 150 x 70 x 10 mm connected to the forced cooling system.

As an example, Fig. 1 shows the dependence of the luminous flux Φ_V produced by each of the tested diodes as a function of their forward current. In this figure, the solid lines refer to the CXB1507 diode, while the dashed lines refer to the CXB2540 diode.

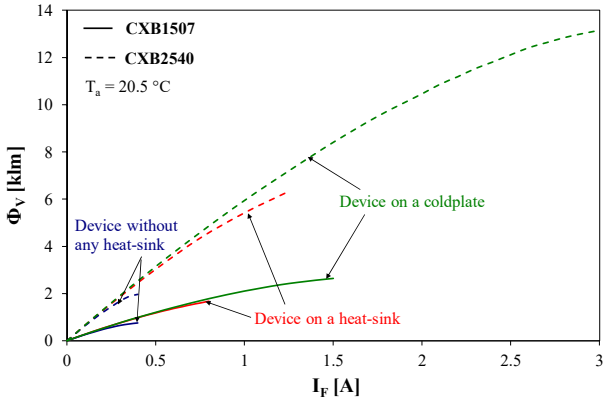

Fig. 1. Dependences of the produced luminous flux on the forward current

It is clearly visible that the maximum value of the luminous flux obtained for the CXB2540 diode is even 6 times higher than for the CXB1507 diode. This discrepancy results, among others, from the difference in the active surface of the devices under consideration and the maximum permissible value of the forward current. At the current value of I_F = 1.5 A, the Φ_V values for both diodes differ four times. The deterioration of the cooling conditions of the diodes under consideration causes a limitation of the maximum permissible value of the I_F current, and consequently – a limitation of the maximum value of Φ_V. Additionally, due to self-heating, the value of the luminous flux corresponding to the set value of the I_F current decreases. This decrease reaches as much as 20%.

The presented measurement results indicate that the design of LEDs in COB packages and the selection of their cooling system significantly affect the electrical and optical parameters of the considered class of semiconductor devices. In further studies, the authors will attempt to prepare a mathematical description of the observed relationships.

The presented research results may be useful for designers of lighting systems. They may also be useful in teaching to illustrate to students the influence of selected factors on the parameters of power LEDs in COB packages.

Signal Processing

Azure Kubernetes Service Design Principles in Machine Learning Systems

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EXTENDED ABSTRACT

The deployment of machine learning (ML) systems at scale requires infrastructure that is robust, adaptable, and intelligently orchestrated. Azure Kubernetes Service (AKS) has emerged as a pivotal platform for managing such systems, offering automation, scalability, and deep integration with Microsoft's cloud-native AI services. This article explores foundational design principles for architecting ML systems on AKS, placing emphasis on scalability, operational reliability, security, observability, and cost optimization. These principles are examined through the lens of architectural decisions, including cluster management, model training and deployment pipelines, and governance strategies. The discussion is enriched with insights from real-world implementations across diverse industries and concludes with an analysis of future trends that shape the evolution of Kubernetes-based ML infrastructures.

Machine learning continues to be a catalyst for digital transformation, driving innovation across sectors such as healthcare, finance, manufacturing, and retail. With applications ranging from predictive analytics and computer vision to natural language processing and autonomous decision-making, ML is enabling organizations to redefine operational models and unlock new business opportunities. However, the complexity and resource intensity of modern ML workloads present significant infrastructure challenges. These workloads demand high computational throughput, elastic resource provisioning, and support for real-time processing, all of which must be managed efficiently to ensure performance and cost control.

Kubernetes has become the foundation for orchestrating ML pipelines due to its support for containerization, declarative configuration, and dynamic scheduling. Its ability to automate scaling, isolate workloads, and maintain high availability makes it ideally suited for operationalizing ML models in production environments. Furthermore, Kubernetes provides a modular framework that accommodates rapid experimentation, continuous integration, and flexible deployment strategies. This extensibility allows teams to integrate components such as experiment tracking tools, feature stores, and GPU-accelerated compute, creating end-to-end MLOps workflows that align with modern engineering practices.

Its integration with Azure Machine Learning enables seamless orchestration of training and inference workloads, while support for GPU-enabled nodes allows high-performance model development and serving. Additionally, AKS is designed to operate in hybrid and multi-cloud environments, empowering organizations to unify on-premises, cloud, and edge deployments under a common governance framework. This flexibility is particularly valuable for enterprises operating under strict data sovereignty or latency-sensitive conditions.

Nevertheless, architecting ML systems on AKS introduces several technical and strategic challenges that must be addressed holistically. Resource allocation is a critical concern, as the efficiency of ML workloads depends on fine-grained control over CPU, memory, and GPU usage. Inadequate provisioning can lead to performance degradation, while over-provisioning inflates operational costs. Security is equally vital, particularly when ML models are trained on sensitive or proprietary data. Ensuring compliance with privacy regulations requires rigorous enforcement of encryption, identity access control, and network segmentation policies. Observability also plays a crucial role in maintaining system health and ensuring model reliability. Without proper monitoring, it becomes difficult to detect issues such as model drift, latency spikes, or pipeline failures. In addition, as ML workloads grow, so does the importance of sustainable cost management, which demands proactive tracking, resource right-sizing, and budget-aware workload planning.

To address these challenges, organizations must adopt a system-wide approach that integrates resource orchestration, security governance, observability tooling, and financial accountability into the ML platform design. AKS supports these goals through its native services and integrations with Azure's broader ecosystem. The ability to configure intelligent autoscaling policies, enforce compliance with infrastructure-as-code, and embed telemetry at every stage of the ML lifecycle positions AKS as a comprehensive solution for enterprise-grade AI systems. Moreover, its extensibility allows teams to leverage third-party tools and open-source frameworks alongside Azure-native components, enabling the creation of highly customized, cloud-agnostic ML environments.

Successful implementations of ML systems on AKS demonstrate the value of this design philosophy. Enterprises are leveraging AKS to shorten development cycles, reduce operational burden, and increase the reliability of model deployments. These case studies reveal patterns such as the use of dedicated node pools for GPU tasks, integration of Azure Monitor and Prometheus for fine-grained telemetry, and deployment strategies that balance performance with cost by dynamically adjusting compute allocations based on workload characteristics.

In closing, the use of AKS in machine learning system design marks a significant shift in how organizations build and scale AI capabilities. As ML platforms continue to evolve, the principles of modularity, observability, security, and adaptive resource management will become increasingly central. The future of Kubernetes-based ML infrastructure lies in greater automation, tighter integration between MLOps components, and enhanced support for decentralized and edge workloads. With its comprehensive features and seamless alignment with cloud-native AI services, AKS stands as a key enabler of this transformation, offering a strategic foundation for scalable and intelligent ML system design in the cloud.

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High-Accuracy ECG Signal Acquisition Using a Power-Efficient 6-bit Level-Crossing ADC

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Summary

This paper presents a novel approach using level-crossing ADCs (LC-ADCs), which provide a more power-efficient solution by sampling only when the input signal exceeds predefined amplitude thresholds. A 6-bit LC-ADC architecture that eliminates the need for an n-bit DAC and uses a single comparator, incorporating integrated sample-and-hold and logic functions, is proposed. This design drastically reduces power consumption while maintaining accuracy, making it particularly suitable for low-power biomedical applications. Simulation results in 180 nm CMOS technology with 1.8-V power supply demonstrate the system's high performance, including a Figure-of-Merit (FoM) that outperforms traditional designs. The proposed LC-ADC architecture is shown to be highly efficient, with significant reductions in power usage and FoM to 90 nW and 0.115 fJ/step, offering an ideal solution for long-term, energy-constrained biomedical signal monitoring.

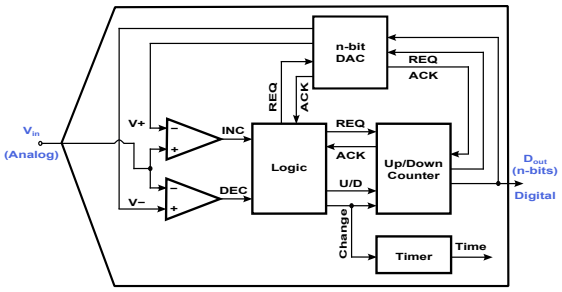

Fig. 1. Block diagram of the conventional LC-ADC using two comparators, an n-bit DAC, a logic block, a timer, and an up/down counter

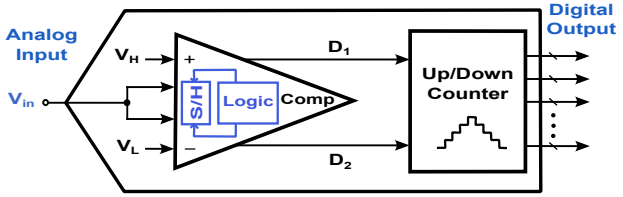

Fig. 2. Block diagram of the proposed LC-ADC, consisting of a comparator with integrated S/H and logic blocks, along with an up/down counter

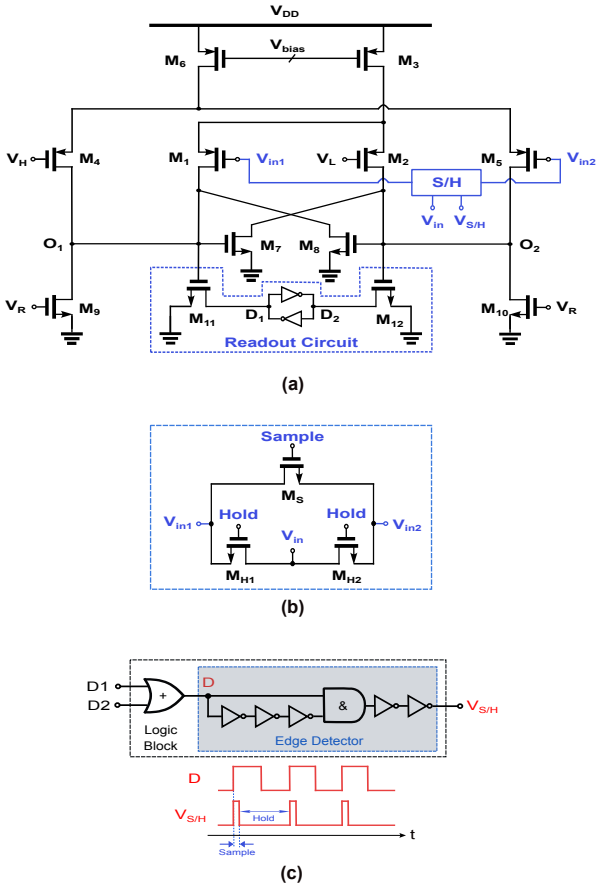

Fig. 3. Transistor level structure of the comparator block including: (a) core current comparator and readout circuit, (b) sample and hold (S/H) circuit, and (c) embedded logic block with edge detector and its input and output pulses

TABLE I
Performance Comparison with Other LC-ADCs

Reference	16	17	22	23	This Work
Process (nm)	180	180	180	180	180
Supply (V)	0.55-1	0.5	1	1.8	1.8
Power (nW)	186	60-220	18	220	90
BW (kHz)	1	1	2.5	10	15
ENOB (bit)	6.2-7.9	5.6	6.2-7.7	6.8	5.7
FoM (fJ/conv.)	165	124	98	198	115
Sim./Meas.	Meas.	Meas.	Sim.	Sim.	Sim.

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Low Voltage, High Power Electronic Load Design for FPGA Current Draw Reproducing

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SUMMARY

FPGA devices can draw exceptionally high currents from low-voltage rails, imposing stringent constraints on the associated power-supply architecture. The present paper introduces an electronic load that faithfully reproduces such current profiles, thereby streamlining the development of low-voltage, high-power supplies and facilitating rigorous validation of the target rails (Figure 1). The conception of an electronic load is intrinsically demanding: the schematic must be meticulously devised, the PCB layout must respect an aggressive resistance budget, and the attendant thermal issues require explicit mitigation. The study demonstrates that loads analogous to those drawn by FPGAs can be generated using more economical solutions than commercial offerings. Accordingly, the prototype operates across 0.8–2.5 V rails and sinks up to 100 A with sub-microsecond edges whilst maintaining an aggregate path resistance below 8 mΩ. A bipartite topology comprising a low-loss MOSFET power stage and a microcontroller-supervised analogue feedback loop—provides constant-current operation with over-voltage, over-current and thermal protection. Bench-top characterisation confirmed rise times of approximately 1 µs and precise replication of the dynamic waveform captured with a Rogowski coil at DesignCon 2020, substantiating the load's suitability for exercising contemporary FPGA regulators. Although a residual temperature-dependent phase lag persists, the data indicate that an appropriately sized heat sink and judicious capacitor selection would yield a compact, robust solution at a fraction of the cost of commercial dynamic loads.

ACKNOWLEDGMENT

The authors would like to express their special thanks to FastLogic Sp.z o.o. and dr Kamil Grabowski for proposing this research topic, financing its implementation, and collaborating during the execution of this project.

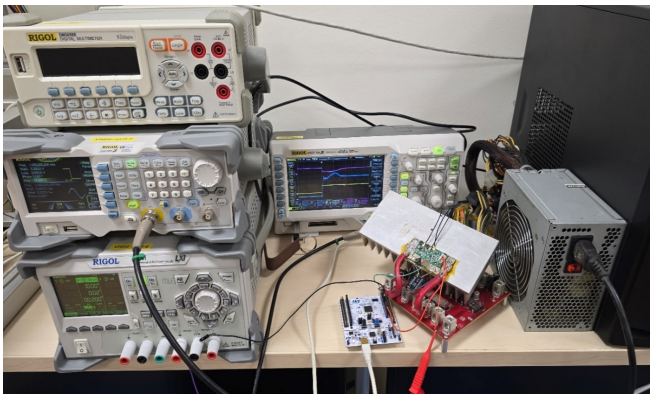

Figure 1. Test setup

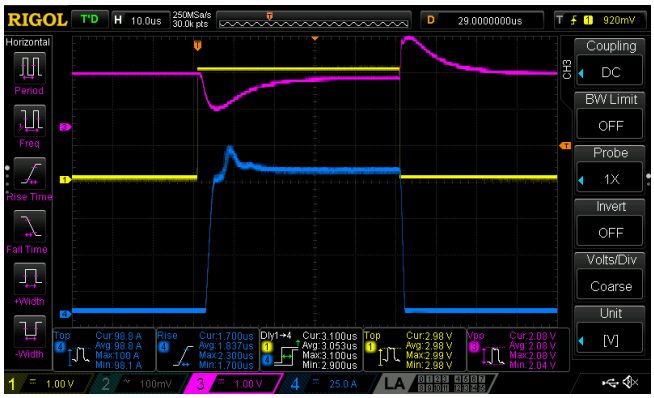

Figure 2. Transient response of the electronic load

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Recurrent LSTM Neural Networks for Language Modelling and Speech Recognition

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***Abstract*—This paper examines interesting natural language modelling tasks, such as word-based and subword-based language modelling, where deep learning methods are making some progress. Language modelling helps to predict the sequence of recognised words or subwords and thus can be used to improve the speech recognition process. However, the field of language modelling is currently witnessing a shift from statistical methods to recurrent neural networks and deep learning techniques. This article focusses on an example of using recurrent LSTM neural networks for language modelling and speech recognition. The new research results presented in this paper, following on from previous papers, focus on how to develop word-based and subword-based LSTM language models and how to use them together. The simultaneous use of both LSTM language modelling methods allows for the development of hybrid language models that have even better properties and can further improve the speech recognition process. The results presented in this paper apply to Polish language modelling, but the results obtained and the conclusions formulated on their basis can also be applied to language modelling applications for other languages.**

***Keywords*—artificial intelligence, neural networks, language modelling, speech recognition.**

Statistical language modelling enables the development of probabilistic models that can predict the next word in a sequence given the words that precede it. Language modelling is the task of assigning a probability to sentences in a language. In addition to assigning a probability to each sequence of words, language models also assign a probability for the likelihood that a given word (or a sequence of words) will follow a sequence of words.

A language model learns the probability of word occurrence based on examples of text. Simpler models may look at the context of a short sequence of words, whereas larger models may work at the level of sentences or paragraphs. Most commonly, language models operate at the level of words. The notion of a language model is inherently probabilistic. A language model is a function that puts a probability measure on strings drawn from some vocabulary. A language model can be developed and used stand-alone, such as to generate new sequences of text that appear to have come from the corpus. Language modelling is a root problem for a wide range of natural language processing tasks. More practically, language models are used on the front- or back-end of a more sophisticated model for a task that requires language understanding. Language modelling is a crucial component in real-world applications such as machine translation and automatic speech recognition. For these reasons, language modelling plays a central role in natural language processing, AI, machine learning and speech recognition research.

A good example is speech recognition, where audio data are used as input to the model and the output requires a language model that interprets the input signal and recognises each new word within the context of the words already recognised. Speech recognition is principally concerned with the problem of transcribing the speech signal as a sequence of words. From this point of view, speech is very often represented by a language model that provides estimates of $P(W)$ for all word strings W independently of the observed signal. The main goal of speech recognition is to find the most likely word sequence given the observed acoustic signal.

Developing better language models often results better on natural language processing and speech recognition task. It is therefore a motivation to develop ever better and more accurate language models. The main objective of the research presented in this paper is to develop language models using recurrent neural networks with a special focus on Long-Short-Term Memory (LSTM) networks. The results presented in this article relate to the development of an LSTM language model using word-based and subword-based methods. In addition, it was proposed to use both LSTM language modelling methods simultaneously to develop a hybrid language model, which has even better properties and can significantly improve speech recognition. The accuracy, loss, and perplexity parameters were used as a measure of language model performance. The hybrid model performs quite well in comparison to other models developed. The performance of the hybrid model is clearly better than the word-based or subword-based language model used alone. The calculated parameters were only used to compare the developed language models. The language models were trained on a limited size test corpus to reduce the training time. Computing the real parameters of the language models would require a long learning process using corpora of very large size and sufficient quality to reflect the specifics of the language. The use of relevant language corpora as training data for developed language models provides the opportunity to simultaneously use word-based and subword-based types of models, as a hybrid language model, to predict word more effectively in the speech recognition process.

Embedded Systems

A Survey and Practical Application of Ethernet-APL, PROFINET Network and HMI

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EXTENDED ABSTRACT

Development of industrial communication protocols has accelerated over the years, leading to increasingly diverse applications. Traditional fieldbus systems are gradually being replaced by protocols based on the Ethernet standard, due to their ability to integrate Information Technology – IT and Automation Technology – AT devices, which are increasingly present in automation environments.

In this context, the Ethernet-APL physical medium emerged. Ethernet-APL (Advanced Physical Layer) is a physical medium that allows the use of protocols based on the Ethernet standard (such as PROFINET, Ethernet/IP and Ethernet Powerlink). It allows electrical connection for severe conditions; two-wire cabling, power and data transmission through the same pair of cables and the possibility of being used in intrinsically safe hazardous areas. Its speed and bandwidth are compatible with the Ethernet standard and the cable can have up to 1,000 meters long.

Objective of this paper is to carry out a practical study, by demonstrating an application that integrates the PROFINET network with a visualization and monitoring system using an Ethernet-APL physical layer. Utilizing PROFINET network devices, the study aims to establish the connection and monitoring of a temperature sensor. In order to achieve this, an Ethernet-APL-based medium will be used to configure a PROFINET network, program the PLC (Programmable Logic Controller) and its peripherals, and set up and program an HMI (Human-Machine Interface) to assemble the final practical application. Study will also assess the interoperability of the equipment.

The goal was to create a practical industrial automation application using the Ethernet-APL physical medium, integrated with the PROFINET protocol and monitored by an HMI, thus demonstrating the interoperability between the different communication protocols and equipments. The system must read the temperature from a PT-100 sensor, activate a set of light signals and pneumatic actuators, and present the information on the HMI. First figure shows the system components (KTP400; XF204 and ET200 SP) and their respective digital input/output cards. Second figure also illustrates the system components (PT-100; TMT86 and A111) and the APL cabling.

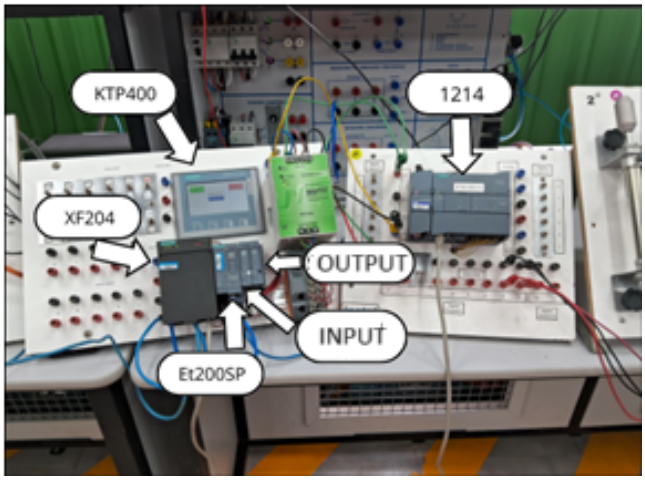

Fig. 1. Fine connections.

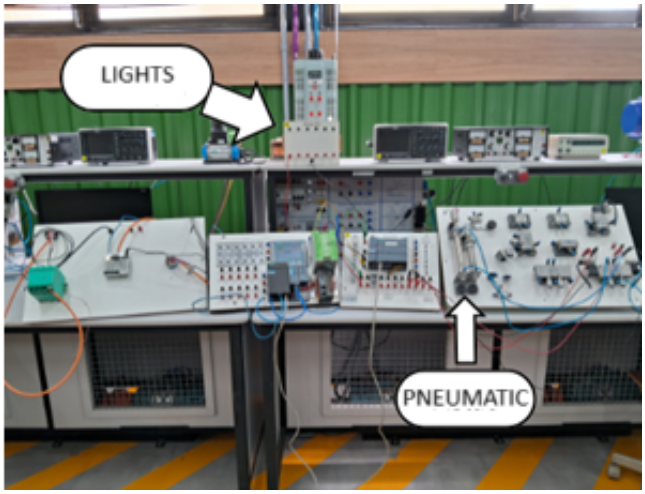

Fig. 2. Image of the entire system structure.

This paper addressed the importance and applicability of the PROFINET network, by using the Ethernet-APL physical layer in the industrial environment. The implementation of this network allows the integration and monitoring for hazardous applications.

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Analysis of Selected Cryptographic Algorithms for Data Transmission in Airborne Networks

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I. Introduction

This paper presents an analysis of a selected set of lightweight cryptographic algorithms in terms of their applications in data transmission in airborne networks. We analyze different types of microcontrollers as possible hardware platforms to apply the chosen algorithms. The ESP32 microcontroller is used for hardware testing. A selected set of lightweight cryptography algorithms is implemented in the microcontroller to test their computational efficiency. The tests for AEAD algorithms include: ChaChaPoly, ASCON-128, TinyJAMBU, ISAP, and PHOTON-Beetle, and for Hashing algorithms: BLAKE2s, ASCON-HASH, and PHOTON-Beetle-HASH.

II. Performance Analysis of Cryptographic Algorithms on ESP32

A. Lightweight cryptography applications

A lightweight cryptography refers to a cryptosystem with low computational cost and suitable for devices with limited resources. The concept was initiated by the National Institute of Standards and Technology (NIST) to develop a cryptographic algorithm that can work with small electronic devices in the IoT environment.

B. Methodology

As a result of our experiments, we wanted to compare different cryptography algorithms which would be suitable to implement on a UAV platform. The study includes a range of cryptographic algorithms, divided into two categories:

- AEAD algorithms: These algorithms provide confidentiality and authenticity in encryption. The tested AEAD algorithms include ChaChaPoly, ASCON-128, TinyJAMBU, ISAP, and PHOTON-Beetle.
- Hashing algorithms: These ensure data integrity and are widely used in digital signatures and authentication mechanisms. The tested hashing algorithms include BLAKE2s, ASCON-HASH, and PHOTON-Beetle-HASH.

The evaluation metrics used to measure their performance are the encryption, decryption, and hashing times in microseconds per byte. Each algorithm is tested for two data sizes: 128 bytes (larger packets) and 16 bytes (smaller packets) to assess performance variations with different input lengths. The execution time is converted into throughput (bytes per second) to facilitate direct comparison.

C. Testing environment

The tests were carried out on the ESP32 microcontroller, a widely used low-power system-on-chip (SoC) designed for embedded and IoT applications. The ESP32 was chosen because of its balance between performance and energy efficiency, which makes it a suitable platform for cryptographic operations in constrained environments.

III. Conclusion

The comparative analysis highlights ChaChaPoly and BLAKE2s as the most performant algorithms in encryption and hashing, respectively. Their high throughput and low per-byte latency make them excellent choices for applications requiring both speed and reliability. ASCON-128 and TinyJAMBU-128, while not as fast, demonstrate sufficient efficiency and are better suited for systems with severe resource constraints. In contrast, the PHOTON-Beetle family, though optimized for lightweight implementation, offers limited performance and may only be appropriate in scenarios where minimal code size or energy consumption is more critical than speed. These findings underscore the importance of context-specific algorithm selection. While high-performance primitives like ChaChaPoly and BLAKE2s offer impressive speed, lightweight alternatives like ASCON and TinyJAMBU remain essential for ultraconstrained platforms. Future research will explore optimizations to balance security and efficiency, ensuring that cryptographic solutions meet the needs of diverse applications.

Acknowledgements

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Comparative Survey Between Industrial Communication Protocols Applied in Hazardous Areas

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EXTENDED ABSTRACT

With the advancement of technology and the integration of industrial systems, communication between devices has been playing an increasingly fundamental role in the efficiency, monitoring and control of processes in manufacturing environments. Consequently, choosing a network protocol is a crucial decision since it requires a careful analysis of each one. The analysis must take into account the nature and features of the industry, the number and type of equipment, the distance between them and the type of industrial environment.

However, there are significant challenges in these applications, such as the presence of explosive atmospheres and flammable materials. These areas, known as Hazardous Areas, are categorized based on the duration that flammable substances, vapors, gases, or dust are present, as well as the potential for these substances to escape or leak, which raises concerns about the safety and operation of these environments.

In order to mitigate these risks, industrial plants must be managed to minimize the likelihood of accidents. In this context, understanding the relationship between network protocols and the safety requirements of hazardous areas is crucial for ensuring the safe operation of industrial systems.

For improved integration between devices and to meet the safety measures required in Hazardous Areas, several industrial network protocols can be employed. In this paper, three protocols will be highlighted: PROFIBUS PA, Fieldbus Foundation, and Ethernet-APL.

This paper aims to present a theoretical study of those protocols applied to Hazardous Areas and to perform a comparative analysis, highlighting their main characteristics, applications, functionalities, and limitations within those environments.

PROFIBUS PA is a protocol profile within the PROFIBUS family, designed to meet the specific demands of automation and process control while offering intrinsically safe transmission for use in hazardous areas [6, 7].

Its protocol architecture is based on the Open Systems Interconnection – OSI reference model as defined by the international standard ISO 7498. OSI model comprises seven layers; however, PROFIBUS PA utilizes only three levels: the physical layer (layer 1), the data link layer (layer 2), and the application layer (layer 7).

Fieldbus Foundation is a bidirectional multipoint communication protocol that enables real-time control between instruments and systems. This protocol stands out for its interoperability among field devices from different manufacturers. It was developed based on the OSI model, although it does not implement all of its layers. Instead, it is structured into physical and communication layers, which handle digital communication between devices.

Ethernet-APL is a physical layer network protocol based on IEEE and IEC standards that employs Ethernet technology for communication between devices and the controller network. It was designed to operate in hazardous areas and was developed to meet all the requirements for using Ethernet in industrial environments [9, 10].

TABLE I.
COMPARISON BETWEEN THE PROTOCOLS [2, 3, 9, 10].

	PROFIBUS PA	**Fieldbus Foundation – H1**	**Fieldbus Foundation – HSE**	**Ethernet-APL**
Communication rate	31.25kbps	31.25kbps	100Mbps	10Mbps
Total network distance	100m in intrinsically safe areas	1900 m in intrinsically safe areas.	100m	Trunk: 1000m
Application in hazardous areas	Possible	Possible	Possible	Drop-offs: 200m
Maximum number of devices	32 devices	12 devices	Up to 254 per network created	Possible
Power supply range of devices	Intrinsically safe areas: 13.5V	Intrinsically safe areas: 13.5V	Intrinsically safe areas: 13.5V	50 devices
Type of cable used	Non-intrinsically safe areas: 24V	Non-intrinsically safe areas: 24V	Non-intrinsically safe areas: 24V	9 >= 15 V, but the standard allows <= 17.5 V

Matlab Simulations in Performance Analysis of Storage Area Networks

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EXTENDED ABSTRACT

Storage Area Networks (SANs) have become fundamental components of modern data infrastructures, supporting the rapid growth of cloud computing, embedded systems, and data-intensive applications. As demands for scalability, real-time responsiveness, and fault tolerance increase, SANs are tasked with providing consistent high-throughput and low-latency access to shared storage resources across heterogeneous environments. However, the complexity introduced by diverse hardware configurations, variable traffic patterns, and unpredictable fault scenarios poses significant challenges for ensuring reliable performance.

This paper presents a detailed simulation-based performance evaluation of SAN architectures, focusing on the interactions between system design, workload characteristics, and operational reliability. Using a custom-built discrete-event simulation framework implemented in MATLAB, the study models a SAN composed of three storage controllers with differing server capacities, service rates, and buffer sizes. The simulation captures realistic conditions by introducing bursty arrival processes, priority-based request scheduling, and stochastic controller failure and recovery events.

The workload is generated as a superposition of baseline Poisson arrivals and randomly occurring bursts, mimicking real-world fluctuations caused by backups, batch jobs, or synchronized tasks. Requests are categorized into three priority classes—high, medium, and low—with strict non-preemptive priority scheduling implemented at the controller level. Failures occur independently on each controller with a predefined probability, and recovery times follow an exponential distribution.

The simulation collects fine-grained metrics at 0.1-second intervals over a 1000-second window, tracking controller utilization, throughput, queue lengths, average waiting time, service time, latency, and dropped requests due to queue overflows. The results highlight several critical performance behaviors.

First, controller utilization and throughput show strong correlation, confirming that processing efficiency is directly tied to the load distribution mechanism. However, the use of a naive shortest-queue load balancing policy proves insufficient, leading to disproportionate load on faster controllers, particularly during burst conditions and failure-induced traffic redistribution. Controllers with lower service capacity become saturated quickly, while more capable controllers are underutilized during certain periods due to delayed workload reallocation.

Second, queue length dynamics reveal system congestion patterns, with Controller 2 frequently reaching its queue limit. This leads to significant numbers of dropped requests, especially during failure periods when the remaining controllers are overloaded. Queue length spikes directly contribute to increases in waiting time and latency, emphasizing the importance of queue management in maintaining service quality.

Third, while the priority scheduling mechanism effectively ensures low latency for high-priority traffic—even during bursts—it results in unfair delays for medium- and low-priority requests. Starvation of lower-priority classes is particularly severe when bursts coincide with controller failures, revealing a trade-off between service differentiation and fairness.

The most alarming finding is the high volume of dropped requests—over 69% for each controller during the simulation period—primarily caused by queue overflows. This points to a lack of resilience in the current SAN configuration, underscoring the need for adaptive buffer sizing, dynamic admission control, and failure-aware load balancing.

The study concludes that while SANs are capable of delivering high performance under ideal or moderately variable conditions, they are vulnerable to instability under realistic workload and fault scenarios. Key recommendations include implementing smarter load balancing algorithms that incorporate priority, failure status, and controller capacity into routing decisions, as well as proactive fault mitigation strategies to redistribute workloads preemptively. Additionally, better workload forecasting and traffic shaping can help smooth demand spikes and reduce queue saturation.

This research provides valuable insights into SAN performance modeling and highlights crucial areas for architectural and algorithmic improvement. The simulation framework developed in this study can serve as a flexible testbed for further exploration of advanced resource allocation techniques, predictive failure models, and integration of emerging technologies such as NVMe-over-Fabrics or software-defined storage. Future work will extend this model to include network latencies, RAID-level behaviors, switch contention, and energy consumption, as well as investigate the use of reinforcement learning to enable self-optimizing SAN environments.

Index of Authors