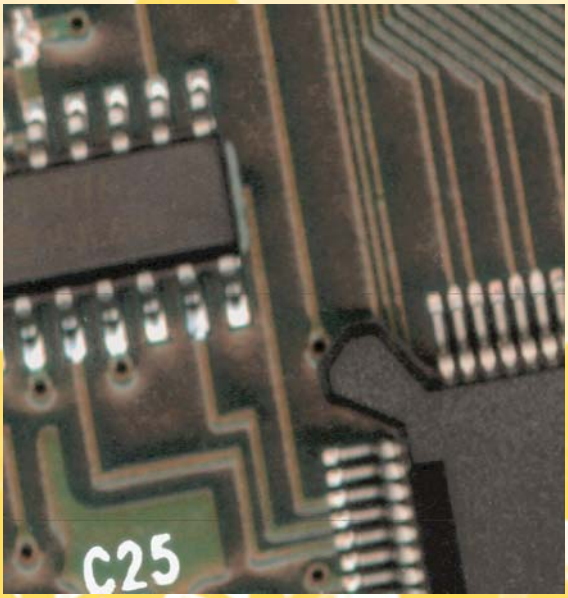
FINAL PROGRAMME

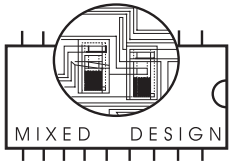
26th International Conference



MIXDES 2019

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

Rzeszów, Poland
27 - 29 June 2019



26th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Rzeszów, Poland 27 – 29 June 2019

MIXDES 2019 Timetable

Day 1	Thursday, June 27th, 2019		
	Room A	**Room B**	**Room C**
8:30	Conference Opening		
9:00	Plenary Session I		
10:00	Session 1 (Part 1)	Session 3 (Part 1)	Special Session I (Part 1)
11:00	*Coffee Break*		
11:15	Session 1 (Part 2)	Session 3 (Part 2)	Special Session I (Part 2)
13:00	*Lunch*		
14:00	Session 2	Session 3 (Part 3) & 7	Special Session II (Part 1)
15:20	Coffee Break		
15:40			Special Session II (Part 2)
19:00	*Welcome Party*		

Day 2	Friday, June 28th, 2019		
	Room A	**Room B**	**Room C**
8:30	Plenary Session II		
9:30	Session 1 (Part 3)	Session 8 (Part 1)	Special Session III (Part 1)
10:30	*Coffee Break*		
10:50	Session 1 (Part 4)	Session 8 (Part 2) & 5 (Part 1)	Special Session III (Part 2)
12:00	*Lunch*		
13:00	*Tourist Activities*		

Day 3	Saturday, June 29th, 2019		
	Room A	**Room B**	**Room C**
8:30	Plenary Session III		
9:30	Session 1 (Part 5)	Session 5 (Part 2)	Special Session IV (Part 1)
10:30	*Coffee Break*		
10:50	Session 1 (Part 6)	IEEE EDS Poland & PAN meeting	Special Session IV (Part 2)
13:00	*Lunch*		
14:00	Introduction to Poster Session		
15:00	*Coffee Break during the Poster Session*		
19:00	*Closing Ceremony & Conference Banquet*		

Additional session/meeting:
Day 1 (Thursday, June 27th, 2019), 15:40 - 17:00, Room B:
Methods for Human Balance Assessment and Rehabilitation

WELCOME TO MIXDES 2019

We are proud to present the 26th International Conference "Mixed Design of Integrated Circuits and Systems" - MIXDES 2019. We welcome you to Rzeszów and hope, that you find the conference professionally stimulating and personally enjoyable. For the past years, the conference has been a unique forum for promoting different approaches to mixed VLSI design and an esteemed venue for presenting multidisciplinary research.

In addition to the regular MIXDES 2019 programme, there are a number of special sessions, focusing on recent trends and advances on all aspects of main conference topics, reviewed and selected from all submissions from 28 countries. During the plenary lectures, the following 6 invited papers will be presented:

- *Advanced MOS Device Technology for Low Power Logic LSI*
  Shinichi Takagi (The University of Tokyo, Japan)
- *Quantum Bits and Quantum Computing Architecture*
  Farzan Jazaeri (EPFL, Switzerland)
- *Towards Energy-Autonomous Integrated Systems Through Ultra-low Voltage Analog IC Design*
  Viera Stopjaková (Slovak University of Technology in Bratislava, Slovakia)
- *THz Technologies and Applications*
  Thomas Skotnicki (Institute of High Pressure Physics PAS, Poland)
- *What is Killing Moore's Law? Challenges in Advanced FinFET Technology Integration*
  Arkadiusz Malinowski (GLOBALFOUNDRIES, USA)
- *Yield and Reliability Challenges at 7nm and Below*
  Andrzej Strojwąs (Carnegie Mellon University, USA)

The program includes 4 special sessions, aiming at complementing the regular program with emerging topics of interest to the circuit design community:

- *Compact Modeling for Nanoelectronics*
  organised by D. Tomaszewski (Institute of Electron Technology, Poland) and W Grabiński (GMC, Switzerland)
- *Intelligent Distributed Systems*
  organised by M. Drozd (LTC Sp. z o.o., Poland), R. Sztoch, P. Sztoch (FINN Sp. z o.o., Poland), B. Sakowicz and D. Makowski (Lodz University of Technology, Poland)
- *Large Scale Research Facilities*
  organised by A. Napieralski, W. Cichalewski (Lodz University of Technology, Poland)
- *Thermonuclear Fusion Projects*
  organised by S. Simrock (ITER, France), D. Makowski (Lodz University of Technology, Poland), D. Bocian and M. Scholz (Institute of Nuclear Physics, Poland)

In addition to the technical sessions, opportunities for the conference attendees will be (free of charge) EDS Distinguished Lecturer Mini-Colloquium: "Nanoelectronics - Technology, Design, Modeling", organized by ED Poland Chapter with collaboration of Institute of Electron Technology, Warsaw, Poland that will take place June 26, 2019 at the Conference hotel.

The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing the contributed papers.

This year Prof. Wiesław Kuźmicz has decided to pass the Programme Chairman function to Prof. Andrzej Pfitzner. We would like to thank Prof. Kuźmicz for the 25 years of hard work assuring proper quality of accepted papers and we are very grateful that he will still support us as a member of the Programme Committee.

We wish you a successful discussions and a pleasant stay in Rzeszów. Next year the Conference will take place in Wrocław to continue our tradition of visiting the most beautiful places in Poland.

Yours Sincerely,
MIXDES 2019 Organising Committee

ORGANIZED BY

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

IN COOPERATION WITH

Poland Section IEEE - ED & CAS Chapter

Section of Microelectronics and Electron Technology
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee of International Union of Radio Science - URSI

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Prof.	W. Kuźmicz	Institute of Micro- and Optoelectronics, Warsaw University of Technology, Poland

Ministry of Science and Higher Education
Republic of Poland

26th International Conference "Mixdes Design of Integrated Circuits and Systems" - MIXDES 2019 - zadanie finansowane w ramach umowy 849/P-DUN/2019 ze środków Ministra Nauki i Szkolnictwa Wyższego przeznaczonych na działalność upowszechniająca naukę

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Prof.	D. Sankowski	Lodz University of Technology, Poland
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Prof.	K. Wawryn	Technical University of Koszalin, Poland
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Prof.	S. Yoshitomi	Toshiba Corporation, Japan
Prof.	J. Zarębski	Gdynia Maritime University, Poland
Prof.	M. Zubert	Lodz University of Technology, Poland

MAIN TOPICS

1. **Design of Integrated Circuits and Microsystems**
   Design methodologies. Digital and analog synthesis. Hardware-software codesign. Reconfigurable hardware. Hardware description languages. Intellectual property-based design. Design reuse.
2. **Thermal Issues in Microelectronics**
   Thermal and electro-thermal modelling, simulation methods and tools. Thermal mapping. Thermal protection circuits.
3. **Analysis and Modelling of ICs and Microsystems**
   Simulation methods and algorithms. Behavioural modelling with VHDL-AMS and other advanced modelling languages. Microsystems modelling. Model reduction. Parameter identification.
4. **Microelectronics Technology and Packaging**
   New microelectronic technologies. Packaging. Sensors and actuators.
5. **Testing and Reliability**
   Design for testability and manufacturability. Measurement instruments and techniques.
6. **Power Electronics**
   Design, manufacturing, and simulation of power semiconductor devices. Hybrid and monolithic Smart Power circuits. Power integration.
7. **Signal Processing**
   Digital and analog filters, telecommunication circuits. Neural networks. Artificial intelligence. Fuzzy logic. Low voltage and low power solutions.
8. **Embedded Systems**
   Design, verification and applications.
9. **Medical Applications**
   Medical and biotechnology applications. Thermography in medicine.

CONFERENCE CENTER

The conference will take place in:

Grand Hotel Boutique
Dymnickiego 1A
35-030 Rzeszów
Tel. +48 17 250 00 00
e-mail: info@grand-hotel.pl

ACCOMMODATION

The accommodation will be offered for the Conference participants at conference site in Grand Hotel Boutique located in the Rzeszów city centre. Please note that the MIXDES 2019 Conference participants reserve the hotel rooms on their own.

REGISTRATION

The standard conference registration fee includes the admission to the conference, a copy of the Book of Abstracts, Conference Proceedings CD-ROM and other conference materials, tourist activities, all lunches, the Welcome Party, the Banquet, coffee and tea during the breaks. To encourage students to participate in the Conference, the student registration fee is available (Welcome Party and Banquet not included).

The Book of Abstract and other conference materials will be distributed to participants at the registration desk. The Conference Proceedings CD-ROM will be distributed to the participants after the conference.

The registration desk will be located in the conference center. It will be working during the following hours:

27 June (Thursday)	07:30 – 13:00 h, 14:00 – 17:00 h
28 June (Friday)	08:00 – 11:00 h
29 June (Saturday)	08:00 – 13:00 h, 14:00 – 15:00 h

GENERAL INFORMATION AND INQUIRIES

Dr. Mariusz Orlikowski

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THE CITY OF RZESZÓW

Rzeszów is the capital city of Subcarpathian Voivodship, the southeastern region of Poland, adjoining the territories of Ukraine and Slovakia. The city itself is about 100 km from the border with each neighbour, so it can be considered as the eastern outpost of the European Union. For centuries Rzeszow took advantage of its location on a major east-west route linking Krakow, Przemysl and Lwow (L'viv) with the Black Sea. The first recorded reference to Rzeszow dates from 1354, when it was granted a town charter by King Casimir the Great. In the 16th century the Wislok River up to Rzeszow was recognised as being navigable, giving the town a direct connection to the city of Gdansk and that of the Baltic Sea. The period of greatest prosperity was at the end of the 16th and the beginning of the 17th centuries, when it became an important centre of trade and craftsmanship. From the 17th to the 19th century, Rzeszow and its surrounding estates were the property of the Lubomirski magnate family.

With its population about 200 thousand inhabitants, occupying an area of 126 km square, Rzeszow is now one of the largest cities of the region and constitutes the economic, academic, cultural and recreational centre of south-eastern Poland. It serves as an important centre for aerospace, IT, chemical, commercial, construction and service industries. Rzeszów is the hub of the Aviation Valley – the largest industrial-technological cluster in Poland that concentrates more than 130 companies connected to the aviation industry. The city is also the main academic centre of the province, and well known for its polytechnic.

Main tourist attractions:

The central square is the Old Town Square with the City Hall and the well of the seventeenth century. The current market differs slightly from the original fifteenth-century appearance - only three frontages of houses are built, which over the centuries underwent reconstructions. They are hotels, restaurants, clubs, pubs, museums, various institutions.

Its historical centre is reminiscent of a village in Galicia and old town is worth a visit. The oldest monument is the 15th Century Parish Church of St. Stanislaus and Wojciech, with a Gothic chancel and three Renaissance headstones belonging to old Rzeszów families, the former owners of the town. One of the greatest attractions of Rzeszow is unique complex of underground cellars and corridors - Underground Tourist Route. With a length of 369 meters, runs under the tenements and the Market Square. It includes 25 basements and 15 corridors, reaching 10 meters into the ground, which have been given names related to the functions and history of the city. You can see the remnants of the medieval walls, traces of fire, residual iron bars and hinges, secret passages.

For more information see:

https://www.staypoland.com/about_rzeszow.htm
https://www.poland.travel/en-gb/cities/rzeszow

TOURIST ACTIVITIES

The guided tour will start at 13:00 in front of the conference site. Participants in coaches will be transported to Łańcut – one of the oldest cities in the region, which history stretches back to the early Middle Ages, founded as a town in 1349 under King Casmir the Great. The main attraction of region is Łańcut Castle - one of the most beautiful aristocratic residences in Poland. Former seat of the aristocratic families Lubomirski and Potocki was built in the years 1628-1641. The palace complex is surrounded by an old and picturesque park in the English style filled with pavilions and farm buildings, all part of the former the daily life of the castle. At the turn of the 19th and the 20th century numerous interesting interiors were arranged and majority of them remained in its original form. The palace complex also includes a small castle and a romantic carriage house, which is a unique collection of horse-drawn vehicles and a rich iconostasis. Today it is also the cultural centre, where one of the most famous chamber music festivals takes place.

After visiting the palace, the participants will return to Rzeszów aproximately at 4:30 pm, where we will see the main attractions of the city.

The guided tour will finish approximately at 7:00 pm.

TRANSPORT

The main conference building (**Grand Hotel Boutique**) is located about 800 m from Rzeszów Główny Railway Station and about 10 km from Rzeszów-Jasionka Airport.

To get to the hotel from the airport you can use buses number 51 or 53 (Piłsudskiego U. Wojewódzki stop). From the railway station use bus number 0A and get off at Lisa-Kuli Galeria stop. You can also use a Taxi. The average price of access to the centre of Rzeszów is about 50 PLN.

To find your way around Rzeszów you can use the page https://jakdojade.pl/rzeszow/. For public transport (buses) you can buy several types of tickets. You have to validate your ticket after you enter the bus.

- single-ride ticket for 3 PLN – valid on a single ride
- 60-minute ticket for 4 PLN – valid for 60 minutes from validation
- 24-hour ticket for 12 PLN – valid for 24 hour from validation

The tickets are available from the ticket machines, They are available on selected bus stops and selected buses. There is no ticket machine at the airport, but the buses from the airport are typically equipped with one.
You can also buy a ticket from the bus driver (60-minute, 4 PLN ticket only).

PROGRAMME OF THE CONFERENCE

The programme of the MIXDES 2019 Conference will include oral presentations of contributed and invited papers, special sessions and poster session.

Except for the plenary and poster sessions, the programme of the conference will be divided into three parallel sessions, in accordance with discussed topics. The language of the Conference is English, neither translation nor interpretation will be provided.

The time of oral presentations:

- for invited papers: 20-25 min. for presentation and 5-10 min. for questions,
- for regular papers: 15 min. for presentation and 5 min. for questions.

Poster presentations:
The authors presenting their papers at the poster sessions will have at their disposal an A0 panel with all the accessories necessary to attach your poster. On the third conference day (June 29th after lunch), an introduction to poster session is planned, in which the authors are asked to present their work very shortly in front of the audience: 2-3 slides, within 1-2 minutes. The questions and discussions will be continued at the poster panels.

Lunches:
Lunches will be served each day at the conference center at the times indicated in the programme.

Welcome Party and Conference Banquet:
The Welcome Party will be organised on Thursday (the first conference day) at 19:00. The Conference Banquet and the Awards Ceremony will take place on Saturday at 19:00.

Note that the Welcome Party and the Conference Banquet are not included in the student registration fee. The student award winners will get a special invitation to the Conference Banquet.

IMPORTANT PHONE NUMBERS

Ambulance	999	Fire Brigade	998
Police	997	Emergency phone	112

BANKING

Foreign exchange facilities are available at major airports and at larger hotels, as well as in many private offices, called “Kantor”. Credit cards can be used in many places such as banks, hotels, car-rental offices, restaurants, and large shops. Approximate currency exchange rate: 1 € = 4.27 PLN, 1 $ = 3.79 PLN (for the up-to-date information refer to **http://www.nbp.pl**).

Credit cards:
Visa and MasterCard are the most common cards. However, other cards might be accepted.

Currency:
Generally, everywhere in Poland you pay in Polish zlotys. The currency units are złoty (zł, PLN) and grosz (gr), 1 zł = 100 gr. The Polish zloty is a fully convertible currency internally in Poland.

WEATHER

June in Poland is generally sunny, with some showers, the temperatures can be typically 15 to 28 ˚C during days. During nights, the temperature can go down to 8-10 ˚C. So, we can suggest you to bring summer clothes, with a quite warm jacket or pullover, and an umbrella.

Time **Room A**

08:30 Conference Opening
Chairmen: Prof. Andrzej Napieralski, Prof. Gilbert De Mey and Prof. Andrzej Pfitzner

Centre for Microelectronics and Nanotechnology Rzeszów - Potential and Possibilities
M. Marchewka (Centre for Microelectronics and Nanotechnology Rzeszów, Poland)

09:00 Plenary Session I: General Invited Papers
Chairman: Prof. Andrzej Napieralski

Yield and Reliability Challenges at 7nm and Below Technology Nodes
A. Strójwąs (Carnegie Mellon University, USA)

Advanced MOS Device Technology for Low Power Logic LSI
S. Takagi, K. Kato, K. Sumita, K. Jo, C.-M. Lim, R. Takaguchi, D.-H. Ahn, J. Takeyasu, K. Toprasertpong, M. Takenaka (The Univ. of Tokyo, Japan)

10:00 Session 1 (Part 1): Design of Integrated Circuits and Microsystems
Chairman: Prof. Witold Pleskacz

A 130 nm CMOS Passive Mixer Utilizing Positive-Negative Feedback as the Input Transconductance
A. Zokaei, K. El-Sankary (Dalhousie Univ., Canada), D. Trukhachev, A. Amirabadi (Dalhousie Univ., Canada and South Tehran Branch Azad Univ., Iran)

A 4.5 fJ/Conversion-step 10-bit 0.6V Asynchronous SAR ADC for Battery-free Miniature Sensor Nodes in 65nm CMOS
A. Dadashi, Y. Berg, O. Mirmotahari (Univ. Oslo, Norway)

A Fast-Lock, Low Jitter, High-Speed Half-Rate CDR Architecture with a Composite Phase Detector (CPD)
Z. Kakehbra, M. Mousazadeh, A. Khoei (Urmia Univ., Iran), A. Dadashi (Univ. Oslo, Norway)

11:00 Coffee Break

11:15 Session 1 (Part 2): Design of Integrated Circuits and Microsystems
Chairman: Prof. Andrzej Pfitzner

A Dual Feedback Wideband Differential Low Noise Amplifier in 130 nm CMOS Process
A. Zokaei, K. El-Sankary (Dalhousie Univ., Canada), D. Trukhachev, A. Amirabadi (Dalhousie Univ., Canada and South Tehran Branch Azad Univ., Iran)

A High-resolution, Wide-range, Radiation-hard Clock Phase-shifter in a 65 nm CMOS Technology
S. Kulis (CERN, Switzerland), D. Yang (Southern Methodist Univ., USA and Univ. of Science and Techn. of China, China), D. Ghong (Southern Methodist Univ., USA), J. Fonseca (CERN, Switzerland), S. Biereigel (CERN, Switzerland, Katholieke Univ. Leuven, Belgium and Brandenburg Univ. of Techn., Germany), J. Ye (Southern Methodist Univ., USA), P. Moreira (CERN, Switzerland)

A Simple Ultra-low Power Opamp in 22 nm FDSOI
W. Kuźmicz (Warsaw Univ. of Techn., Poland)

A Wide Band Fractional-N Synthesizer in 0.18um CMOS Process
E. Hosseini, M. Mousazadeh (Urmia Univ., Iran), A. Dadashi (Univ. Oslo, Norway)

13:00 Lunch

14:00 Session 2: Thermal Issues in Microelectronics
Chairman: Prof. Gilbert De Mey

I*nvestigations of Influence of Properties of PCB on Thermal and Optical Parameters of the LED Module*
K. Górecki, P. Ptak (Gdynia Maritime Univ., Poland)

Modelling a Half-bridge DC-DC Converter Including the IGBT Module with Thermal Phenomena Taken into Account
P. Górecki, K. Górecki (Gdynia Maritime Univ., Poland)

Thermal Characterisation of Color Power LEDs
M. Janicki, Ł. Starzak, T. Torzewicz (Lodz Univ. of Techn., Poland), K. Górecki, P. Ptak (Gdynia Maritime Univ., Poland)

Using Compact Thermal Modelling for the Investigation of a Cooling System Dysfunction Applied to a Power Module with Double Sided Cooling
A. Cassou, P. Tounsi (LAAS-CNRS, France), J.-P. Fradin (ICAM, France)

15:20 Coffee Break

19:00 Welcome Party

Time **Room B**

10:00 Session 3 (Part 1): Analysis and Modelling of ICs and Microsystems
Chairman: Prof. Andrzej Kos

Development of SiC MOSFET Electrical Model and Experimental Validation: Improvement and Reduction of Parameter Number
Q.C. Nguyen (IRT Saint-Exupéry, LAAS-CNRS and ICAM Toulouse, France), P. Tounsi (LAAS-CNRS, France), J.-P. Fradin (ICAM Toulouse, France), J.-M. Reynes (IRT Saint-Exupéry and aPSI3D, France)

Energy Harvesting System Model Based on Reverse Electrowetting
D. Nikolov, R. Rusev, G. Angelov, M. Spasova (Tech. Univ. Sofia, Bulgaria)

Forward and Reverse Operation of Enclosed-gate MOSFETs and Sensitivity to High Total Ionizing Dose
A. Nikolaou, L. Chevas, A. Papadopoulou, N. Makris, M. Bucher (Tech. Univ. Crete, Greece), G. Borghello, F. Faccio (CERN, Switzerland)

11:00 Coffee Break

11:15 Session 3 (Part 2): Analysis and Modelling of ICs and Microsystems
Chairman: Dr. Paweł Śniatała

Fractional Order Circuit Elements Derived from Electromagnetism
T. Stefanski (Gdansk Univ. of Techn., Poland), J. Gulgowski (Univ. Gdansk, Poland)

Multiconductor Transmission Line System with Stochastically Affected Boundary Conditions
L. Brancik, E. Kolarova (Brno Univ. of Techn., Czech Republic)

Semiconductor Device Parameter Extraction Based on I-V Measurements and Simulation
D. Kasprowicz (Warsaw Univ. of Techn., Poland)

Simple Chaotic Oscillator with Filtering Passive Two-port Having Fractional-order Segments
J. Petrzela (Brno Univ. of Techn., Czech Republic)

13:00 Lunch

14:00 Session 3 (Part 3) & 5: Analysis and Modelling of ICs and Microsystems & Signal Processing
Chairman: Dr. Dariusz Makowski

Substrate Coupling of DMOS Transistors in High Voltage SOI processes
K. Hirmer, K. Hofmann (Tech. Univ. Darmstadt, Germany)

THz Response of a JLFET Detector - Interpretation by a Resistive Mixing Theory
D. Tomaszewski, M. Zaborowski, J. Marczewski (Institute of Electron Techn., Poland)

Novel Design Solution of Reconnection-less Electronically Reconfigurable Filter
L. Langhammer, R. Sotner, J. Dvorak (Brno Univ. of Techn., Czech Republic), T. Dostal (College of Polytechnics Jihlava, Czech Republic)

Stage-oriented, Mixed Design Methodology for Image Processing Using VHDL and Python
M. Chojnacki, P. Sękalski (Lodz Univ. of Techn., Poland)

15:20 Coffee Break

19:00 Welcome Party

Time **Room C**

10:00 Special Session I (Part 1): Large Scale Research Facilities
Chairman: Dr. Wojciech Cichalewski

Status, Highlights, and Achievements of the ESS Accelerator Project
A. Sunesson (European Spallation Source, Sweden)

Institute of Electronic Systems contribution to ESS's LLRF Control System
I. Rutkowski, M. Grzegrzolka, K. Czuba, K. Sąpór, B. Kola (Warsaw University of Technology, Institute of Electronic Systems, Poland)

Status of the Phase Reference Line for the European Spallation Source
K. Czuba, J. Berliński, Ł. Czuba, E. Fistek, M. Kalisiak, T. Leśniak, K. Oliwa, R. Papis, D. Sikora, W. Wierba, M. Żukociński (Warsaw Univ. of Techn., Poland), A. Sunesson, R. Zeng (European Spallation Source, Sweden)

11:00 Coffee Break

11:15 Special Session I (Part 2): Large Scale Research Facilities
Chairman: Prof. Anders Sunesson

FPGA-based Data Processing in the Neutron-Sensitive Beam Loss Monitoring System for the ESS Linac
G. Jabłoński (Lodz Univ. of Techn., Poland), I. Dolenc Kittelmann (European Spallation Source, Sweden), W. Jałmużna, R. Kiełbik, W. Cichalewski (Lodz Univ. of Techn., Poland), K. Rosengren, T. Shea, F. dos Santos Alves, V. Grishin (European Spallation Source, Sweden), L. Segui, T. Papaevangelou (IRFU, CEA, Universite Paris-Saclay, France), C. Zamantzas (CERN, Switzerland)

IFJ PAN Contribution to the European Spallation Source
D. Bocian, W. Gaj, E. Górnicki, L. Hajduk, P. Halczyński, K. Kasprzak, K. Myalski, T. Ostrowicz, M. Sienkiewicz, M. Skiba, J. Świerblewski (Inst. of Nuclear Physics PAS, Poland)

The Implementation of Thermal-Electrical Analogy to Quench Limit Determination of Superconducting Magnets
D. Bocian (Institute of Nuclear Physics PAS, Poland)

Upgrade of the Arc Interconnection Verification system for the Large Hadron Collider
M. Bednarski, P. Jurkiewicz, J. Ludwin, D. Wojas (IFJ PAN, Poland), M. Bednarek, G. D'Angelo (CERN, Switzerland)

Overview of Real-Time Redundancy Development in the Master Oscillator for European XFEL
B. Gąsowski, T. Owczarek, K. Czuba, Ł. Zembala (Warsaw Univ. of Tech., Poland), H. Pryschelski (DESY, Germany)

13:00 Lunch

14:00 Special Session II (Part 1): Compact Modeling for Nanoelectronics
Chairman: Dr. Mike Schwarz

Low Power Design in nm Moore to AI Technology (Invited Paper)
R.V. Joshi, M. Ziegler (IBM Research Division, USA)

FOSS Compact Model Prototyping with Verilog-A Equation-Defined Devices (VAEDD)
M. Brinson (London Metropolitan Univ., UK)

Closed-Form Modeling Approach of Trap-Assisted Tunneling Current for Use in Compact TFET Models
F. Horst, A. Farokhnejad (TH Mittelhessen Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), B. Iniguez (Univ. Rovira i Virgili, Spain), A. Kloes (TH Mittelhessen Univ. of Applied Sciences, Germany)

15:20 Coffee Break

15:40 Special Session II (Part 2): Compact Modeling for Nanoelectronics
Chairman: Prof. Mike Brinson

The Need of Simulation Methodologies for Active Semiconductor Devices in MEMS (Invited Paper)
M. Schwarz (Robert Bosch GmbH, Germany)

Characterization of the Charge-Trap Dynamics in Organic Thin-Film Transistors
G. Darbandy, C. Roemer, J.S. Leise, J. Pruefer (TH Mittelhessen Univ. of Applied Sciences, Germany), J.W. Borchert (Max Planck Inst. for Solid State Research and Univ. Stuttgart, Germany), H. Klauk (Max Planck Inst. for Solid State Research, Germany), A. Kloes (TH Mittelhessen Univ. of Applied Sciences, Germany)

Analytical Model for Threshold-Voltage Shift in Submicron Staggered Organic Thin-Film Transistors
J. Pruefer, J.S. Leise (TH Mittelhessen Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), G. Darbandy (TH Mittelhessen Univ. of Applied Sciences, Germany), J.W. Borchert (Max Planck Inst. for Solid State Research and Univ. Stuttgart, Germany), H. Klauk (Max Planck Inst. for Solid State Research, Germany), B. Iniguez (Univ. Rovira i Virgili, Spain), T. Gneiting (AdMOS GmbH, Germany), A. Kloes (TH Mittelhessen Univ. of Applied Sciences, Germany)

Current vs Substrate Bias Characteristics of MOSFETs as a Tool for Parameter Extraction
D. Tomaszewski, J. Malesińska, G. Głuszko, K. Kucharski (Łukasiewicz Research Network - Institute of Electron Techn., Poland)

19:00 Welcome Party

Time **Room A**

08:30 Plenary Session II: General Invited Papers
Chairman: Prof. Gilbert De Mey

Towards Energy-autonomous Integrated Systems Through Ultra-low Voltage Analog IC Design
V. Stopjaková, D. Arbet, M. Kováč, L. Nagy (Slovak Uni. of Techn. in Bratislava, Slovakia)

Terahertz Technologies and Applications
T. Skotnicki (Inst. of High Pressure Physics PAS and Warsaw Univ. of Techn., Poland), W. Knap (Inst. of High Pressure Physics PAS, Poland and Montpellier University and CNRS, France)

09:30 Session 1 (Part 3): Design of Integrated Circuits and Microsystems
Chairman: Prof. Witold Pleskacz

A New High-speed and Low Area Efficient Pipelined 128-bit Adder Based on Modified Carry Look-ahead Merging with Han-Carlson Tree Method
S. Ghafari, M. Mousazadeh, A. Khoei (Urmia Univ., Iran), A. Dadashi (Univ. Oslo, Norway)

Area Efficient High-voltage Charge Pump for Double Backplate MEMS Microphone
L. Zou (TDK Electronics AG, Denmark), T. Hanzlik (TDK Poland, Poland), G. Rocca (TDK Electronics AG, Denmark)

Flexible HLS-Based Implementation of the Karatsuba Multiplier Targeting Homomorphic Encryption Schemes
M. Foster, M. Łukowiak, S. Radziszowski (Rochester Inst. of Techn., USA)

10:30 Coffee Break

10:50 Session 1 (Part 4): Design of Integrated Circuits and Microsystems
Chairman: Dr. Daniel Tomaszewski

A New Very High-speed True 7-3 Compressor
S. Ghafari, M. Mousazadeh, A. Khoei (Urmia Univ., Iran), A. Dadashi (Univ. Oslo, Norway)

Implementation of Addition and Subtraction Operations in Multiple Precision Arithmetic
K. Rudnicki (Brightelligence Inc., UK), T. Stefanski (Gdansk Univ. of Techn., Poland)

Improving Dual-Slope A/D Converter with Noise-Shaping and Digital Filtering Techniques
P. Śniatała, D. Makowski (Poznan Univ. of Techn., Poland), J. Goes (Univ. Nova de Lisboa, Portugal), W. Machowski (AGH Univ. of Science and Techn., Poland), S. Salas Arriarán (Univ. Peruana de Ciencias Aplicadas, Peru)

12:00 Lunch

13:00 Tourist Acivities

Time **Room B**

09:30 Session 6 (Part 1): Embedded Systems
Chairman: Prof. Wiesław Kuźmicz

A Human Immunity Inspired Algorithm to Detect Infections in a Computer Program
K. Wawryn, P. Widulinski (Koszalin Univ. of Techn., Poland)

A Low-cost IoT System for Environmental Pollution Monitoring in Developing Countries
O.O. Flores-Cortez, R.A. Cortez, V.I. Rosa (Univ. Tecnologica San Salvador, El Salvador)

Implementation of an I2C to Profibus Serial Comunication Interface
T. Mussolini, F. Ramos, R. Moreno, T. Pimenta (Univ. Federal de Itajuba, Brazil)

10:30 Coffee Break

10:50 Session 6 (Part 2) & Session 4 (Part 1): Embedded Systems & Testing and Reliability
Chairman: Prof. Andrzej Kos

Formal Verification of Real-time Systems Developed for Single-processor Platform with Alvis
J. Baniewicz, M. Szpyrka (AGH Univ. of Science and Techn., Poland)

Minimization of SM-Covers of Petri Net Specifications of Control Systems
A. Karatkevich (AGH Univ. of Science and Techn., Poland), Ł. Stefanowicz (Univ. Zielona Gora, Poland)

Configurable MBIST Processor for Embedded Memories Testing
A. Wojciechowski (Warsaw Univ. of Techn., Poland), K. Marcinek (Warsaw Univ. of Techn. and ChipCraft, Poland), W. Pleskacz (Warsaw Univ. of Techn., Poland)

12:00 Lunch

13:00 Tourist Acivities

Time **Room C**

09:30 **Special Session III (Part 1): Intelligent Distributed Systems**
Chairman: Dr. Bartosz Sakowicz

Forecasting Interruptions in Power Supply Using Photovoltaics in Poland - Case Study of Safe Pedestrian Crossing
W. Marańda, P. Marciniak, R. Kotas, B. Sakowicz (Lodz Univ. of Techn., Poland), A. Tylman (Univ. of Lodz, Poland), P. Sztoch, M. Drozd (LTC Ltd, Poland)

Information Security in the Organization: Information Security Management System - ISO Standards
A. Stawinski, B. Sakowicz, D. Makowski (Lodz Univ. of Techn., Poland), M. Drozd, P. Sztoch (LTC Ltd, Poland)

Simulation Environment for Power Transfer States in Renewable Energy Systems
W. Tylman, W. Marańda, P. Marciniak, R. Kotas, B. Sakowicz (Lodz Univ. of Techn., Poland), P. Sztoch, M. Drozd (LTC Ltd., Poland)

10:30 **Coffee Break**

10:50 **Special Session III (Part 2): Intelligent Distributed Systems**
Chairman: Dr. Dariusz Makowski

Framework for Intelligent, Distributed Control Systems for Business and Industry
M. Drozd, P. Sztoch, K. Czerkas (LTC Ltd, Poland), B. Sakowicz, D. Makowski (Lodz Univ. of Techn., Poland)

Methods of Device Certification, FIPS 140-2 Standard
B. Sakowicz, A. Stawiński, D. Makowski (Lodz Univ. of Techn., Poland), M. Drozd, P. Sztoch (LTC Ltd, Poland)

12:00 **Lunch**

13:00 **Tourist Acivities**

Time **Room A**

08:30 Plenary Session III: General Invited Papers
Chairman: Prof. Andrzej Pfitzner

Quantum Bits and Quantum Computing Architecture
F. Jazaeri (EPFL, Switzerland)

What is Killing Moore's Law? Challenges in Advanced FinFET Technology Integration
A. Malinowski, J. Chen, E.H. Lim, D.K. Sohn (GLOBALFOUNDRIES, USA)

09:30 Session 1 (Part 5): Design of Integrated Circuits and Microsystems
Chairman: Prof. Paweł Gryboś

Cryptographic Coprocessor with Modular Architecture for Research and Development of Countermeasures Against Power-Based Side-Channel Attacks
M. Korona, T. Wojciechowski, M. Rawski, P. Tomaszawicz (Warsaw Univ. of Techn., Poland)

Decreasing Number of LUTs for Moore FSMs
A. Barkalov, L. Titarenko, K. Mielcarek (Univ. Zielona Gora, Poland), K. Krzywicki, W. Zajac (The Jacob of Paradies Univ., Poland)

Linear and Non-linear Decomposition of Index Generation Functions
T. Mazurkiewicz (Military Univ. of Techn., Poland), T. Łuba (Warsaw School of Computer Science, Poland)

10:30 Coffee Break

10:50 Session 1 (Part 6): Design of Integrated Circuits and Microsystems
Chairman: Dr. Paweł Śniatała

Design of an Energy-efficient Current-to-frequency Converter for a Wearable Sensor Platform
E. Voulgari, F. Krummenacher, M. Kayal (EPFL, Switzerland)

Lab-chip Diagnostic Device for the Rainwater Monitoring System in Wireless Sensors Network
O. Matviykiv, N. Bokla, T. Klymkovych, U. Marikutsa, I. Farmaha, M. Lobur (Lviv Polytechnic National Univ., Ukraine), M. Banaś (AGH Univ. of Science and Techn., Poland)

Non-disjoint Decomposition Using r-admissibility and Graph Coloring and Its Application in Index Generation Functions Minimization
T. Mazurkiewicz (Military Univ. of Techn., Poland), T. Łuba (Warsaw School of Computer Science, Poland)

Reducing the Bipolar Junction Transistor Vbe Non-Linearity
V. Bucur, G. Banarie (Analog Devices Inc., Ireland and Univ. Politehnica Bucharest, Romania), S. Marinca, M. Bodea (Univ. Politehnica Bucharest, Romania)

13:00 Lunch

14:00 Introduction to Poster Session
Chairman: Prof. Witold Pleskacz

A Clock-Free 200MS/s 10-bit Time-Interleaved SAR ADC
C.-H. Kuo, Z.-J. Luo (National Taiwan Normal Univ., Taiwan)

A Low Power, Low Chip Area, Two-stage Current-mode DAC Implemented in CMOS 130 nm Technology
J. Dalecki (UTP Univ. of Science and Techn., Poland), R. Długosz, T. Talaśka (UTP Univ. of Science and Techn. and Aptiv Services, Poland), G. Fischer (Innovations for High Performance Microelectronics, Germany)

Application of Offset Trimming Circuit for Reducing the Impact of Parasitics in Capacitive Sensor Readout Circuit
P. Zajac, M. Jankowski, P. Amrozik, M. Szermer (Lodz Univ. of Techn., Poland)

Continuous-Time Discriminator Designin in CMOS 28 nm Process
P. Kaczmarczyk, P. Kmon (AGH Univ. of Science and Techn., Poland)

DC/DC Buck Converter with Build-in Tuned Sawtooth Wave Generator Using CMOS Technology
A. Borkowski (Warsaw Univ. of Techn., Poland), T. Borejko (Warsaw Univ. of Techn., ChipCraft Sp. z o.o., Poland), W. Pleskacz (Warsaw Univ. of Techn., Poland)

Design and Verification Environment for RISC-V Processor Cores
A. Oleksiak, S. Cieślak, K. Marcinek, W. Pleskacz (Warsaw Univ. of Techn., Poland)

Highly Linear 4-bit Flash ADC Implemented in 22 nm FD-SOI Process
Z. Jaworski (Warsaw Univ. of Techn., Poland)

Implementation and Comparison of SPA and DPA Countermeasures for Elliptic Curve Point Multiplication
Ł. Ostrowski, K. Marcinek, W. Pleskacz (Warsaw Univ. of Techn., Poland)

Retargeting the MIPS-II CPU Core to the RISC-V Architecture
S. Cieślak, A. Oleksiak, K. Marcinek, W. Pleskacz (Warsaw Univ. of Techn., Poland)

Trade-offs and Other Challenges in CMOS Implementation of Parallel FIR Filters
K. Kubiak (Adam Mickiewicz Univ. and Aptiv Services, Poland), R. Długosz (UTP Univ. of Science and Techn. and Aptiv Services, Poland)

A Delta-Sigma Modulator with UPWM Quantizer for Digital Audio Class-D Amplifier
C.-H. Kuo, Y.-J. Liou (National Taiwan Normal Univ., Taiwan)

A Tool for Generating Test Scenarios for Automotive Active Safety Algorithms and ADAS Functions
Z. Długosz (Poznan Univ. of Techn. and Aptiv Services, Poland), D. Sasin (Aptiv Services, Poland), R. Długosz (UTP Univ. of Science and Techn. and Aptiv Services, Poland)

Software Tool for FAM-based Modeling and Simulation of Fuzzy Systems
A. Wielgus, P. Pruszczak (Warsaw Univ. of Techn., Poland)

Low Energy Precise Navigation System for the Blind with Infrared Sensors
P. Marzec, A. Kos (AGH Univ. of Science and Techn., Poland)

Methods to Assess Self-regulatory Mechanisms of the Cardiovascular System under Simulated Hypergravity Conditions
E. Sobotnicka, A. Sobotnicki, M. Czerw, G. Badura (Inst. of Medical Techn. and Equipment, Poland), M. Krej (WIML, Poland), L. Puchalska (Medical Univ. of Warsaw, Poland), K. Kowalczuk, S. Gaździński, Ł. Dziuda (WIML, Poland)

New Possibilities for Fetal Monitoring Using Unobtrusive Abdominal Electrocardiography
A. Matonia, T. Kupka, K. Horoba, J. Jezewski (Inst. of Medical Techn. and Equipment, Poland), R. Martinek (VSB-Technical Univ. Ostrava, Czech Republic), J. Wrobel (Inst. of Medical Techn. and Equipment, Poland), R. Kahankova (VSB-Technical Univ. Ostrava, Czech Republic), R. Czabanski (Silesian Univ. of Techn., Gliwice, Poland), S. Graczyk (President Stanislaw Wojciechowski State Univ. of Applied Sciences in Kalisz, Poland)

Recognition of Atrial Fibrilation Episodes in Heart Rate Variability Signals Using a Machine Learning Approach
K. Horoba (Inst. of Medical Techn. and Equipment, Poland), R. Czabanski (Silesian Univ. of Techn., Gliwice, Poland), J. Wrobel, A. Matonia (Inst. of Medical Techn. and Equipment, Poland), R. Martinek (VSB-Technical Univ. Ostrava, Czech Republic), T. Kupka (Inst. of Medical Techn. and Equipment, Poland), R. Kahankova (VSB-Technical Univ. Ostrava, Czech Republic), J.M. Leski (Silesian Univ. of Techn., Gliwice, Poland), S. Graczyk (President Stanislaw Wojciechowski State Univ. of Applied Sciences in Kalisz, Poland)

Wireless System for Diagnostics of Wound Healing
D. Obrębski, M. Zbieć (Łukasiewicz Research Network - Institute of Electron Techn., Poland), A. Pepłowski, D. Janczak (Warsaw Univ. of Techn. and Centre for Advanced Materials and Technologies, Poland), M. Zych (Warsaw Univ. of Techn., Poland), M. Jakubowska (Warsaw Univ. of Techn. and Centre for Advanced Materials and Technologies, Poland)

15:00 Coffee Break during the Poster Session

19:00 Closing Ceremony & Conference Banquet

Time **Room B**

09:30 Session 4 (Part 2): Testing and Reliability
Chairman: Prof. Gilbert De Mey

Detecting PCB Assembly Defects Using Infrared Thermal Signatures
N. El Belghiti Alaoui (ACTIA Automotive and LAAS-CNRS, France), P. Tounsi, A. Boyer (LAAS-CNRS, France), A. Viard (ACTIA Automotive, France)

Estimation of the Operating Range of Automotive Key Fobs during a Radiated Emissions Test under a Low Frequency Band
G. Oleszek (AGH Univ. of Science and Techn., Poland)

High-Level Functional Test Generation for Microprocessor Modules
A. Oyeniran, R. Ubar (Tallinn Univ. of Techn., Estonia)

10:30 Coffee Break

10:50 IEEE EDS Poland meeting

13:00 Lunch

19:00 Closing Ceremony & Conference Banquet

Time	Room C

09:30 Special Session IV (Part 1): Thermonuclear Fusion Projects
Chairman: Dr. Dariusz Makowski

Plasma Diagnostics at ITER
M. Walsh (ITER Organization, France)

Instrumentation and Control Development for ITER Diagnostics and Integration with Central CODAC
S. Simrock (ITER, France)

IFJ PAN Contribution to the ITER Radial Neutron Camera
D. Bocian, J. Kotuła (Institute of Nuclear Physics PAS, Poland), R. Kantor, P. Młynarczyk (Cracow University of Technology, Poland)

10:30 Coffee Break

10:50 Special Session IV (Part 2): Thermonuclear Fusion Projects
Chairman: Dr. Dariusz Bocian

Diagnostics Integration into W7-X CoDaC for OP2
A. Winter (IPP Greifswald, Germany)

Application of ITER Diagnostics I&C Design Methodology to the ITER Upper Visible/Infrared Wide Angle Viewing System
S. Esquembri (Univ. Politécnica de Madrid, Spain), V. Martin, C. Awanzino (Bertin Techn., France), J. Nieto, A. de Gracia, M. Ruiz (Univ. Politécnica de Madrid, Spain), R. Reichle (ITER, France)

Magnetics Diagnostics at ITER Using Field Programmable Gate Array Technology
M. Baldris, R. Martí, I. Siewiera (GTD Sistemas de Información, Spain)

Impact of Low- and High-Z Ion-induced Damage on the Reflectivity of Molybdenum Mirrors and Sub-surface Microstructure
Ł. Ciupiński (Warsaw Univ. Tech., Poland)

Fast Digital X-ray Detection System Based on Hybrid Pixel Detectors
P. Maj (AGH Univ. of Science and Techn., Poland)

Overview of Soft X-ray GEM Diagnostic System for Tokamak Impurities Monitoring
A. Wojeński (Warsaw Univ. Techn., Poland)

Data Acquisition and Processing for Plasma Diagnostics
D. Makowski (Lodz Univ. of Techn., Poland)

13:00 Lunch

19:00 Closing Ceremony & Conference Banquet

Rzeszów City Map