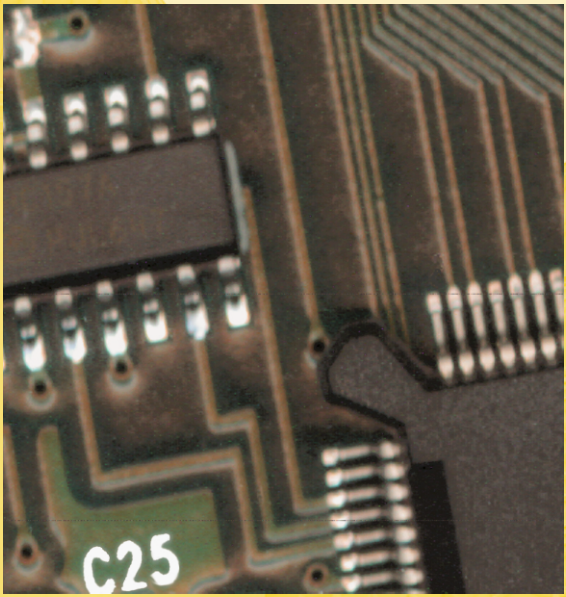
FINAL PROGRAMME

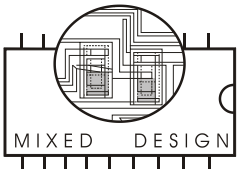
32nd International Conference



MIXDES 2025

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

Szczecin, Poland
26 - 27 June, 2025



32nd International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Szczecin, Poland, 26-27 June 2025

MIXDES 2025 Timetable

Day 1	Thursday, June 26th, 2025		
	Room A	**Room B**	**Room C**
9:00	Conference Opening		
9:05	Plenary Session I		
10:50	Coffee Break		
11:20	Session 1 (Part 1)	Session 2	Session 4
13:00	*Lunch*		
14:00	Session 1 (Part 2)	Session 3	Session 5
19:00	*Welcome Party*		

Day 2	Friday, June 27th, 2025		
	Room A	**Room B**	**Room C**
9:00	Plenary Session II		
10:00	Session 1 (Part 3)	Session 6 (Part 1)	IEEE ED&EP Poland Meeting
11:00	*Coffee Break*		
11:30	Session 1 (Part 4)	Session 6 (Part 2)	Special Session I
13:00	*Lunch*		
14:00	*Tourist Activities*		
19:00	*Closing Ceremony*		

WELCOME TO MIXDES 2025

This year the International Conference "Mixed Design of Integrated Circuits and Systems" celebrates its 32nd edition. For the past thirty one years the conference has been a unique forum for promoting different approaches to mixed VLSI design and an esteemed venue for presenting multidisciplinary research. This year we meet together in Szczecin, the western port city in Poland. As this is the first conference after passing away of Prof. Andrzej Napieralski, its founder, we will be commemorating His life and achievements during a presentation given on the first day.

MIXDES 2025 consists of plenary lectures, regular and special sessions focusing on recent trends and advances on all aspects of main conference topics, reviewed and selected from all paper submissions from 12 countries. During the plenary and AI special session, the following 5 invited papers will be presented:

- *AI for Processors, Processors for AI: Going New Ways for Processor Architectures*
  M. Hübner (Brandenburg Univ. of Techn. Cottbus - Senftenberg, Germany)
- *Electronic Control Systems for Ion Trap Quantum Computers*
  G. Kasprowicz (Warsaw Univ. of Techn., Poland)
- *Mixed Mode: More than Analog and Digital*
  R.S. Murphy, R. Torres (INAOE, Mexico)
- *Modern Challenges in Hardware Design*
  M. Zmuda (Intel Technology, Poland)
- *Video-assisted Dentistry with Deep Neural Networks*
  D. Węsierski (Gdansk Univ. of Techn., Poland)

The program includes two special sessions, aiming at complementing the regular program with emerging topics of interest to the circuit design community:

- *Advancing FOSS Compact Modelling: From OTF Transistors to Mott Memristors*
  organized by A. Kloes, M. Schwarz (Technische Hochschule Mittelhessen, Germany), W. Grabiński (GMC, Switzerland) and D. Tomaszewski (Lukasiewicz - IMiF, Warsaw, Poland)
- *Artificial Intelligence in Electronic Systems*
  organized by T. Stefański (Gdańsk Univ. of Techn., Poland) and R. Długosz (Bydgoszcz Univ. of Science and Techn., Poland)

The organisers would like to thank all the distinguished scientists who have supported the conference by taking part in the International Programme Committee and reviewing the contributed papers.

We hope that you will enjoy your visit to Szczecin and for the next year we invite you to Poznań, one of the oldest and largest cities on the western side of Poland.

Yours Sincerely,
MIXDES 2025 Organising Committee

ORGANIZED BY

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

IN COOPERATION WITH

Poland Section IEEE - ED & CAS Chapter

Section of Microelectronics and Electron Technology
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee of International Union of Radio Science - URSI

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Dr. M. Orlikowski (Secretary) Department of Microelectronics and Computer Science
Dr. G. Jabłoński Lodz University of Technology, Poland

PROGRAMME COMMITTEE

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Prof. S. Yoshitomi	GigaChip, Japan
Prof. J. Zarębski	Gdynia Maritime Academy, Poland
Prof. M. Zubert	Lodz University of Technology, Poland

MAIN TOPICS

1. **Design of Integrated Circuits and Microsystems**
   Design methodologies. Digital and analog synthesis. Hardware-software codesign. Reconfigurable hardware. Hardware description languages. Intellectual property-based design. Design reuse.
2. **Analysis and Modelling of ICs and Microsystems**
   Simulation methods and algorithms. Behavioural modelling with VHDL-AMS and other advanced modelling languages. Microsystems modelling. Model reduction. Parameter identification.
3. **Power Electronics**
   Design, manufacturing, and simulation of power semiconductor devices. Hybrid and monolithic Smart Power circuits. Power integration.
4. **Signal Processing**
   Digital and analogue filters, telecommunication circuits. Neural networks. Artificial intelligence. Fuzzy logic. Low voltage and low power solutions.
5. **Embedded Systems**
   Design, verification and applications.

CONFERENCE CENTER

The conference will take place in:

Courtyard by Marriott Szczecin City
Brama Portowa 2
70-225 Szczecin, Poland
tel.: +48 91 823 3050, e-mail: rezerwacja@courtyardszczecin.pl

REGISTRATION

The standard conference registration fee includes the admission to the conference, a copy of the Book of Abstracts, Conference Proceedings CD-ROM and other conference materials, tourist activities, all lunches, the welcome party, the banquet, coffee and tea during the breaks. To encourage students to participate in the Conference, the student registration fee is available.

The Book of Abstracts and other conference materials will be distributed to participants at the registration desk. The Conference Proceedings CD-ROM will be distributed to the participants after the conference.

The registration desk will be located in the conference center. It will be working during the following hours:

26 June (Thursday)	08:00 – 13:00 h, 14:00 – 17:00 h
27 June (Friday)	08:00 – 13:00 h

GENERAL INFORMATION AND INQUIRIES

Dr. Mariusz Orlikowski

Lodz University of Technology,
Department of Microelectronics and Computer Science
ul. Wólczańska 221 (building B18), 93-005 Łódź, Poland

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THE CITY OF SZCZECIN

Szczecin is a city situated in the north-west of Poland, where the river Odra meets the Baltic Sea. For centuries this location has been the junction for major European transit routes, from the west to the east and from to the north to the east, through the Baltic Sea. Szczecin is a city with over a thousand years of tradition and turbulent history, and is also the historical capital of Western Pomerania. Its most illustrious period was the time of the reign of the dukes of the Griffin dynasty, when the city belonged to the Hanseatic League. More information about Szczecin can be found at the City web page:

https://visitszczecin.eu/en

TOURIST ACTIVITIES

Szczecin's recorded history dates back over 1300 years, when diverse tribes and peoples such as the Vikings and Lechites erected strongholds in the vicinity. It subsequently served as the seat of the Dukes of Pomerania and the House of Griffin. In the course of the millennium, Szczecin was part of Piast Poland, Denmark, the Holy Roman Empire, Sweden, Prussia, Germany and modern-day Poland. The city's architecture and cultural heritage reflects these periods, with excellent examples of Brick Gothic, Gründerzeit, Neoclassical, socialist realist and contemporary styles. The planned urban landscape was based on the Orion constellation, with avenues, roundabouts and extensive parkland. The city's chief landmarks include the Szczecin Cathedral, the Ducal Castle, the National Museum and the Szczecin Philharmonic.

This year’s sightseeing tour will take us through the historic and cultural highlights of Szczecin. We will begin with a meeting at the hotel at 14:00, followed by a visit to the Port Gate, one of Szczecin’s most recognizable historical monuments. Nearby, we will see the Szczecin Main Post Office and the Palace of the Pomeranian Land. Our walk will continue to the Mieczysław Karłowicz Philharmonic in Szczecin, a striking example of contemporary architecture, where we will explore the building and its surroundings. At 15:00, we will take part in a cruise on Lake Dąbie, offering scenic views of the region’s natural beauty and industrial heritage. Upon returning, our walking tour will continue along the Chrobry Embankments, a picturesque riverside

promenade offering panoramic views of the Oder River and city landmarks. We will then visit the Pomeranian Dukes' Castle, the historical seat of the ruling dynasty, and explore the Sienny Market along with the Old Town Hall. The tour will conclude with a visit to the Archcathedral Basilica of St. James the Apostle, one of the tallest churches in Poland and a significant example of Gothic architecture. We expect to return to the hotel between 18:00 and 18:30.

TRANSPORT

Szczecin can be reached by train or road, you can also use Szczecin Goleniów airport serving connections with Warsaw, Dublin, London Stansted, Oslo and Liverpool (https://airport.com.pl/en). For all airline passengers there are transfer buses available. One ticket costs approx. 25 PLN and is available to buy online. Currently two bus companies operate between the airport and Szczecin: Follow Me! (https://followme.pl/en/) and PKS (https://pks.szczecin.pl/). Additionally, also Regio trains depart from the terminal directly to Szczecin (https://rozklad.pkp.pl/en). The train ticket costs 17.50 PLN. Taxis are also available from outside the terminal and served by Airport Taxi Group (tel. +48 91 481 7690). The estimated travel time is 30 minutes and the journey costs up to 200 PLN. Please mind that the train station located on the airport is named "PORT LOTNICZY SZCZECIN GOLENIÓW" and Szczecin main railway station translates to "SZCZECIN GŁÓWNY".

To move around Szczecin you can use the city public transport (https://www.zditm.szczecin.pl/en). The departure times for the local transport are clearly posted at all stops. Tickets can be bought from any kiosk selling newspapers or from the ticket machine inside every vehicle. The tickets are valid for a limited period, timed from when validated in the ticket validator inside a tram or a bus. Note that on both buses and trams, night tickets have specific rules regarding time limit. Luggage doesn't require tickets.

Ticket type	normal/night lines	fast lines
15-minute	3.00 PLN	6.00 PLN
30-minute	4.00 PLN	8.00 PLN
1-hour	6.00 PLN	12.00 PLN
24-hour	15.00 PLN	15.00 PLN

There are several taxi corporations in Szczecin, which may be requested by a phone call:

- CITY TAXI +48 914 335 335
- RADIO TAXI +48 914 875 875
- MIX TAXI +48 918 120 130
- TAKSA TAXI +48 794 222 230
- TAXI 4 YOU +48 914 833 833
- VIUP TAXI +48 913 131 131
- TAXI Prawobrzeże +48 914 615 615
- AIR Taxi Szczecin +48 91 313 13 33

Alternatives to taxis include the Bolt and Uber apps.

PROGRAMME OF THE CONFERENCE

The programme of the MIXDES 2025 Conference will include oral presentations of contributed and invited papers and special sessions. Except for the plenary sessions, the programme of the conference will be divided into three parallel sessions, in accordance with discussed topics. The language of the Conference is English, neither translation nor interpretation will be provided.

The time of oral presentations:

- invited papers: 20-25 min. for presentation and 5-10 min. for questions,
- regular papers: 15 min. for presentation and 5 min. for questions.

Lunches:

Lunches will be served each day at the conference center at the times indicated in the programme.

Welcome Party and Conference Banquet:

The Welcome Party will be organised on Thursday (the first conference day) at 19:00. The Conference Banquet and the Closing Ceremony will take place on Friday at 19:00. Both events will take place at the conference center.

IMPORTANT PHONE NUMBERS

Ambulance	999	Fire Brigade	998
Police	997	Emergency phone	112

BANKING

Foreign exchange facilities are available at major airports and at larger hotels, as well as in many private offices, called “Kantor”. Credit cards can be used in most of the places such as banks, hotels, car-rental offices, restaurants, and shops. Approximate currency exchange rate: 1 € = 4.27 PLN, 1 $ = 3.74 PLN (for the up-to-date information refer to http://www.nbp.pl).

Credit cards:

Visa and MasterCard are the most common cards. However, other cards might be accepted.

Currency:

Generally, everywhere in Poland you pay in Polish zlotys. The currency units are złoty (zł, PLN) and grosz (gr), 1 zł = 100 gr. The Polish zloty is a fully convertible currency internally in Poland.

WEATHER

June in Poland is generally sunny, with some showers, the temperatures can be typically 15 to 28 ˚C during days. During nights, the temperature can go down to 8-10 ˚C. So, we can suggest you to bring summer clothes, with a quite warm jacket or pullover, and an umbrella.

Time **Room A**

09:00 Conference Opening
Chairmen: Prof. Wojciech Tylman and Prof. Andrzej Pfitzner

09:05 Plenary Session I
Chairman: Prof. Wojciech Tylman

Presentation Commemorating Life and Achievements of Prof. Andrzej Napieralski
W. Tylman (Lodz Univ. of Techn., Poland), W. Kuźmicz, A. Pfitzner (Warsaw Univ. of Techn., Poland), K. Górecki (Gdynia Maritime Univ., Poland)

Mixed Mode: More than Analog and Digital
R.S. Murphy - EDS Distinguished Lecturer, R. Torres (INAOE, Mexico)

Modern Challenges in Hardware Design
M. Zmuda (Intel Technology, Poland)

10:50 Coffee Break

11:20 Session 1 (Part 1): Design of Integrated Circuits and Microsystems
Chairman: Prof. Andrzej Pfitzner

CMOS OTA for Detector Readout Electronics Integrator in the ALICE FIT Project
J. Miszczyński, P. Otfinowski, A. Laczewski, M. Grzegorzek, I. Brzozowski, C. Worek, P. Wiącek, P. Russek, J. Kitowski (AGH Univ. of Krakow, Poland), J. Otwinowski (Inst. of Nuclear Physics, Poland)

Design and Optimization of OTA-C Filters with Shared CMFB and Output Stages: Performance, Power, and Area Analysis
H. Aleksiuk, O. Bogucki, P. Halman, B. Pankiewicz (Gdansk Univ. of Techn., Poland)

Design Considerations for Integrated SiGe BiCMOS Phase-Locked Loops in the Millimeter-Wave Band
F. Herzel, A. Ergintav, C. Carta, G. Fischer (IHP Frankfurt (Oder), Germany)

13:00 Lunch

14:00 Session 1 (Part 2): Design of Integrated Circuits and Microsystems
Chairman: Prof. Witold Pleskacz

Enhancing Test-Driven Development for Reconfigurable Hardware through High-Level Synthesis and Early-Stage Validation
R. Diachok, H. Klym (Lviv Polytechnic National Univ., Ukraine)

FSMLock: Sequential Logic Locking Case Study
J. LaPietra, M. Kurdziel (L3Harris Technologies, USA), M. Łukowiak (Rochester Inst. of Techn., USA)

Recording Channel Parameters Influence Analysis on Time-Related X-ray Based Measurements in CMOS 40 nm
F. Księżyc, P. Kmon (AGH Univ. of Krakow, Poland)

19:00 Welcome Party

Time **Room B**

11:20 Session 2: Signal Processing
Chairman: Prof. Wojciech Tylman

Azure Kubernetes Service Design Principles in Machine Learning Systems
Y. Bershchanskyi, H. Klym (Lviv Polytechnic National Univ., Ukraine)

High-Accuracy ECG Signal Acquisition Using a Power-Efficient 6-bit Level-Crossing ADC
A. Amini (Univ. of Pavia, Italy), H. Norouzi Kalehsar (Urmia Univ., Iran)

Low Voltage, High Power Electronic Load Design for FPGA Current Draw Reproducing
S. Przybył, P. Sarna, Z. Kulesza, M. Zubert (Lodz Univ. of Techn., Poland)

Recurrent LSTM Neural Networks for Language Modelling and Speech Recognition
P. Kłosowski (Silesian Univ. of Techn., Poland)

13:00 Lunch

14:00 Session 3: Analysis and Modelling of ICs and Microsystems
Chairman: Prof. Alexander Kloes

Fractional Spurious Tones Analysis of the Space-Time Averaging PLL
R. Wiliński, P. Gryboś (AGH Univ. of Krakow, Poland)

High-Level Modeling of RF Power Amplifiers and Antenna Arrays for Efficient Over-the-Air Power Combination in RF Transceivers
M. Diacu (Univ. Nova de Lisboa, Portugal), J. Guerreiro (Univ. Nova de Lisboa and Inst. de Telecomunicações, Portugal), J.P. Oliveira (Univ. Nova de Lisboa and UNINOVA-CTS, Portugal), P. Montezuma (Univ. Nova de Lisboa, Inst. de Telecomunicações and Koala Tech, Portugal), P. Viegas (Koala Tech, Portugal)

Reliability Analyses of Ultra-Low Voltage Analog Spiking Neurons
G. Brandsteert, L. Van Brandt, D. Flandre (Univ. Catholique de Louvain, Belgium)

19:00 Welcome Party

Time **Room C**

11:20 Session 4: Power Electronics
Chairman: Prof. Witold Pleskacz

A Thermal Behavior of Lateral (VESTIC) BJTs on SOI Substrate
P. Mierzwiński (Warsaw Univ. of Techn., Poland)

Considerations on the Importance of Proper Modeling of Heat Transfer Coefficient Values
M. Janicki (Lodz Univ. of Techn., Poland)

Influence of the Cooling System on Characteristics of Power LEDs in COB Packages
K. Górecki, P. Ptak, D. Płokarz (Gdynia Maritime Univ., Poland)

13:00 Lunch

14:00 Session 5: Embedded Systems
Chairman: Prof. Paweł Śniatała

A Survey and Practical Application of Ethernet-APL, PROFINET Network and HMI
A. Lugli, A. Aragão, E.R. Neto, G.A. Vizotto, J.A. Barbosa, J.P. Paiva (INATEL, Brazil), T. Pimenta (Univ. Federal de Itajuba, Brazil)

Comparative Survey Between Industrial Communication Protocols Applied in Hazardous Areas
A. Lugli, A. Teixeira, J.P. Henriques, J.P. Paiva, J. Azevedo (INATEL, Brazil), T. Pimenta (Univ. Federal de Itajuba, Brazil)

Analysis of Selected Cryptographic Algorithms for Data Transmission in Airborne Networks
S. Baliński, P. Śniatała, M. Sobieraj, A. Grocholewska-Czuryło (Poznan Univ. of Techn., Poland), J. Xie, S. Ren (San Diego State Univ., USA)

Matlab Simulations in Performance Analysis of Storage Area Networks
J. Nazdrowicz (Lodz Univ. of Techn., Poland), M. Tuszyńska (Cracow Univ. of Techn., Poland)

19:00 Welcome Party

Time **Room A**

09:00 Plenary Session II
Chairman: Prof. Andrzej Pfitzner

AI for Processors, Processors for AI: Going New Ways for Processor Architectures
M. Hübner (Brandenburg Univ. of Techn. Cottbus - Senftenberg, Germany)

Electronic Control Systems for Ion Trap Quantum Computers
G. Kasprowicz (Warsaw Univ. of Techn., Poland)

10:00 Session 1 (Part 3): Design of Integrated Circuits and Microsystems
Chairman: Prof. Andrzej Pfitzner

Design of the Charge-Sampling Multiplying PLL in CMOS 40 nm
J. Zając, P. Kmon (AGH Univ. of Krakow, Poland)

Optimum Design of a Mostly-Digital Fleischer-Laker Switched-Capacitor Bilinear Bandpass Filter in Standard CMOS Technology
H. Serra, J.P. Oliveira, J. Goes (UNINOVA-CTS and NOVA FCT, Portugal)

Practical Implementation of Voltage-to-Current and Current-to-Voltage Converter in High Voltage SOI Technology
M. Jankowski (Lodz Univ. of Techn., Poland)

11:00 Coffee Break

11:30 Session 1 (Part 4): Design of Integrated Circuits and Microsystems
Chairman: Prof. Wojciech Tylman

Implementation of a PLL Loop Circuit for Frequency Synthesis in 65 nm CMOS Technology
M. Tymińska (Warsaw Univ. of Techn., Poland), M. Kucharski (OmniChip Sp. z o.o., Poland), W. Pleskacz (Warsaw Univ. of Techn., Poland)

SHA-256 Hash Generator in Verilog HDL
B. Rulka, P. Pieńczuk (Łukasiewicz - Inst. of Microeletronics and Photonics and Warsaw Univ. of Techn., Poland), W. Pleskacz (Warsaw Univ. of Techn., Poland)

SYNAPSE - A New Approach to Semi-automated Design of Ultra-low-power Application-specific Embedded Processors
X. Ji, T. Kazmierski, B. Halak (Univ. of Southampton, UK)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony

Time **Room B**

10:00 Session 6 (Part 1): Artificial Intelligence in Electronic Systems
Chairman: Prof. Tomasz Stefański

Video-assisted Dentistry with Deep Neural Networks (invited paper)
D. Węsierski (Gdansk Univ. of Techn., Poland)

Application of Modified Particle Swarm Optimization Algorithm in FIR Filter Design
K. Pipka (Gdańsk Univ. of Techn., Poland), T. Talaśka (Gdańsk Univ. of Techn. and Bydgoszcz Univ. of Science and Techn., Poland), R. Długosz (Bydgoszcz Univ. of Science and Techn. and Aptiv Services, Poland), W. Pedrycz (Univ. of Alberta, Poland)

Edge Computing of Human Poselet
T. Byrwa, J. Kłopotek Główczewski, M. Czubenko (Gdansk Univ. of Techn., Poland)

11:00 Coffee Break

11:30 Session 6 (Part 2): Artificial Intelligence in Electronic Systems
Chairman: Prof. Rafał Długosz

Anomaly Detection on the Edge: Comparison of Reconstruction and Classification Based Approaches
Ł. Grzymkowski, T. Cejrowski (Arrow Electronics, Poland), T. Stefański (Gdansk University of Technology, Poland)

Application of Dual-Q TQWT for Atrial Fibrillation Detection with Three-Layered Neural Network
T. Pander (Silesian Univ. of Techn., Poland)

Design Flow for AI-driven Medical Systems Demonstrated through an Example in Dental Imaging Analysis
M. Fechner, K. Śniatała, P. Śniatała (Poznan Univ. of Techn., Poland), S. Ren (San Diego State Univ., USA), R. Śniatała, T. Pawlaczyk (Poznan Univ. of Medical Sciences, Poland)

Evaluating Device Variability in RRAM-Based Single- and Multi-Layer Perceptrons
A. Blumenstein (THM Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), E. Pérez, C. Wenger (IHP Frankfurt (Oder) and Brandenburg Univ. of Techn. Cottbus - Senftenberg, Germany), N. Dersch (THM Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), A. Kloes (THM Univ. of Applied Sciences, Germany), B. Iñíguez (Univ. Rovira i Virgili, Spain), M. Schwarz (THM Univ. of Applied Sciences, Germany)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony

Time **Room C**

10:00 IEEE ED&EP Poland Section Technical Meeting

11:00 Coffee Break

11:30 Special Session I: Advancing FOSS Compact Modelling: From OTF Transistors to Mott Memristors

Chairmen: Dr. Daniel Tomaszewski and Dr. Władysław Grabiński

A Generic Approach for Compact Modeling of Variability and Low-Frequency Noise in Organic Thin-Film Transistors
A. Kloes, G. Darbandy (THM Univ. of Applied Sciences, Germany), B. Iñíguez (Univ. Rovira i Virgili, Spain), A. Nikolaou (THM Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain)

Extraction of Open-Access-PDK Active Inductance Parameters with FOSS Tools
M. Brinson (London Metropolitan Univ., UK)

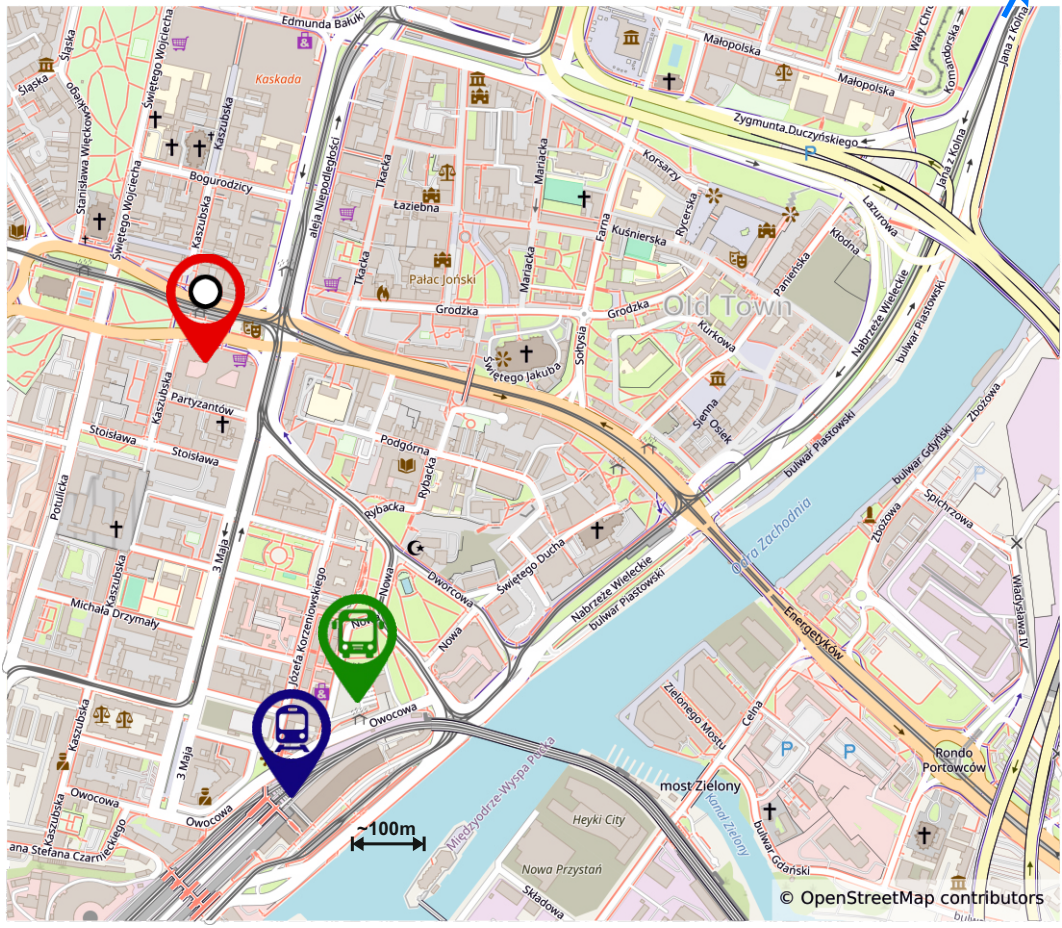
Spiking Neurons Demystified by a Dynamical Model of Mott Memristors
L. Van Brandt, N. Bidoul, T. Ratier, J.-C. Delvenne, D. Flandre (Univ. Catholique de Louvain, Belgium)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony

Szczecin Center Map



Courtyard by Marriott / Moxy hotels
The Conference Site
Brama Portowa 2

Szczecin
Bus terminal

Szczecin Główny
Train Station

Tourist activities (sailing part)
The mooring place
Jana z Kolna 7