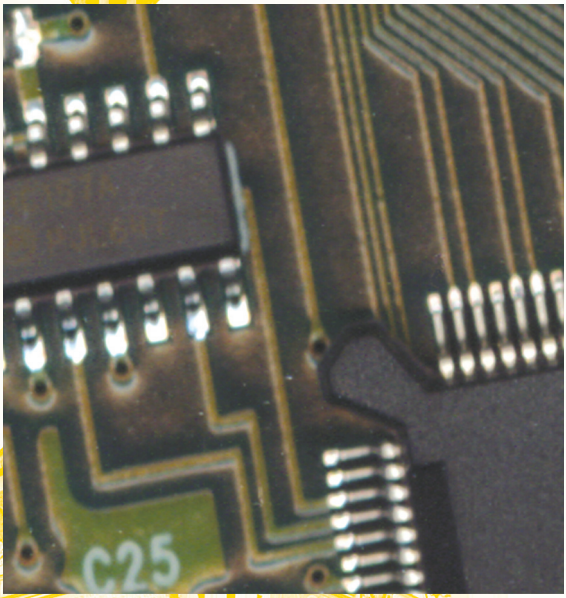
FINAL PROGRAMME

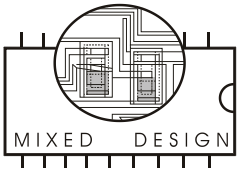
33rd International Conference



MIXDES 2026

MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS

Poznań, Poland
25 - 26 June, 2026



33rd International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Poznań, Poland, 25-26 June 2026

MIXDES 2026 Timetable

Day 1	Thursday, June 25th, 2026		
	Room A	**Room B**	**Room C**
8:30	Conference Opening		
8:40	Plenary Session I		
9:40	Vendor Session I		
10:40	*Coffee Break*		
11:00	Session 1 (Part 1)	Session 2	Special Session 3
13:00	*Lunch*		
14:00	Session 1 (Part 2)	Session 3	Special Session 2
15:20	*Coffee Break*		
15:40	Session 1 (Part 3)	Session 5	Session 7
19:00	*Welcome Party*		

Day 2	Friday, June 26th, 2026			
	Room A	**Room B**	**Room C**	**Room D**
8:30	Plenary Session II			
9:00	Vendor Session II			
9:20	Session 1 (Part 4)	Session 4	Special Session 1 (Part 1)	Tutorial
10:40	*Coffee Break*			
11:10	Session 1 (Part 5)	Session 7	Special Session 1 (Part 2)	Special Session 4
13:00	Lunch			
14:00	*Tourist Activities*			
19:00	*Closing Ceremony & Conference Banquet*			

WELCOME TO MIXDES 2026

We are proud to present the 33rd International Conference "Mixed Design of Integrated Circuits and Systems" - MIXDES 2026. For the past thirty two years the conference has been a unique forum for promoting different approaches to mixed VLSI design and an esteemed venue for presenting multidisciplinary research. This year we meet together in Poznań, one of the oldest and largest cities in western Poland.

MIXDES 2026 program consists of plenary lectures, regular and special sessions focusing on recent trends and advances on all aspects of main conference topics, reviewed and selected from all paper submissions from 16 countries. During the plenary sessions, the following invited papers will be presented:

- *Digital Education in Engineering Practical Work*
  Prof. T.D. Drysdale (University of Edinburgh, UK)
- *Photonic Integration for Optical Interconnect and Sensing Applications*
  Prof. S.-.Lee (National Taiwan University of Science and Techn., Taiwan)
- *TSRI Platform for Advanced Packaging and Silicon Photonics*
  Prof. Chien-Nan Liu (Taiwan Semiconductor Research Institute, Taiwan)

The program includes four special sessions, aiming at complementing the regular program with emerging topics of interest to the circuit design community:

- *Advances in Smart Electronics for Artificial Intelligence and Future Technologies*
  organised by Prof. C.-Y. Yao (National Taiwan Univ. of Science and Techn., Taiwan) and Prof. C.-W. Lu (National Tsing Hua Univ., Taiwan)
- *FAMES Pilot Line Highlights – Current Developments in FD SOI Technology and RRAM Applications*
  organised by Dr. P. Wiśniewski (CEZAMAT, Poland)
- *Open-source Silicon Ecosystem*
  organised by Dr. K. Herman and Dr. W. Grabiński (IHP (Oder), Germany)
- *UAV as a Platform for Various Applications*
  organised by Prof. Paweł Śniatała (Poznań Univ. of Techn., Poland)

The conference program is enriched by two accompanying events: *Analog IC Design Using Open Source Tools and IHP-Open-PDK* (all-day workshop organized on June 24, 2026) and *Considerations on the Design of Resilient 2.5-3D Heterogeneous, Multilayer Interposer Systems for Chip Lifecycle Management* (45 min tutorial organized on June 26, 2026). Both events are organized by IHP - Leibniz Institute for High Performance Microelectronics, Germany.

We hope that you will enjoy your visit to Poznań and that the conference will provide a valuable opportunity for fruitful discussions, inspiring exchanges of ideas, and the establishment of new scientific collaboration.

Yours Sincerely,
MIXDES 2026 Organising Committee

ORGANIZED BY

Department of Microelectronics and Computer Science,
Lodz University of Technology, Poland

Institute of Computer Science,
Poznan University of Technology, Poland

Institute of Microelectronics and Optoelectronics,
Warsaw University of Technology, Poland

IN COOPERATION WITH

Intel Technology Poland

Openchip

Chimera Technology

Poland Section IEEE - ED & CAS Chapter

SEMI

Section of Microelectronics and Electron Technology
of the Committee of Electronics and Telecommunication
of the Polish Academy of Sciences

Commission of Electronics and Photonics
of Polish National Committee of International Union of Radio Science - URSI

MEDIA PATRONAGE

Mikrokontroler.pl

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Prof.	P. Śniatała	Institute of Computer Science,
Mgr.	M. Fechner	Poznan University of Technology, Poland

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Dr. J.-M. Sallese	Swiss Federal Institute of Technology, Switzerland
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Prof. B. Więcek	Lodz University of Technology, Poland
Prof. S. Yoshitomi	GigaChip, Japan
Prof. J. Zarębski	Gdynia Maritime Academy, Poland
Prof. M. Zubert	Lodz University of Technology, Poland

MAIN TOPICS

1. **Design of Integrated Circuits and Microsystems**
   Design methodologies. Digital and analog synthesis. Hardware-software codesign. Reconfigurable hardware. Hardware description languages. Intellectual property-based design. Design reuse.
2. **Analysis and Modelling of ICs and Microsystems**
   Simulation methods and algorithms. Behavioural modelling with VHDL-AMS and other advanced modelling languages. Microsystems modelling. Model reduction. Parameter identification.
3. **Power Electronics**
   Design, manufacturing, and simulation of power semiconductor devices. Hybrid and monolithic Smart Power circuits. Power integration.
4. **Signal Processing**
   Digital and analogue filters, telecommunication circuits. Neural networks. Artificial intelligence. Fuzzy logic. Low voltage and low power solutions.
5. **Embedded Systems**
   Design, verification and applications.
6. **Medical Applications**
   Medical and biotechnology applications. Thermography in medicine.
7. **Artificial Intelligence in Electronic Systems**
   AI-driven design. AI-driven signal and data processing. Edge AI.

CONFERENCE CENTER

The conference will take place in:

Mercure Poznań Centrum Hotel
Roosevelta 20
60-829 Poznań, Poland
tel.: +48 60 855 8000, e-mail: H3393@accor.com

REGISTRATION

The standard conference registration fee includes the admission to the conference, a copy of the Book of Abstracts, Conference Proceedings CD-ROM and other conference materials, tourist activities, all lunches, the welcome party, the banquet, coffee and tea during the breaks. To encourage students to participate in the Conference, the student registration fee is available.

The Book of Abstracts and other conference materials will be distributed to participants at the registration desk. The Conference Proceedings CD-ROM will be distributed to the participants after the conference.

The registration desk will be located in the conference center. It will be working during the following hours:

25 June (Thursday)	08:00 – 13:00 h, 14:00 – 17:00 h
26 June (Friday)	08:00 – 13:00 h

GENERAL INFORMATION AND INQUIRIES

Dr. Mariusz Orlikowski

Lodz University of Technology, Department of Microelectronics and Computer Science
ul. Wólczańska 221 (building B18), 93-005 Łódź, Poland

e-mail: mixdes2026@dmcs.p.lodz.pl tel.: +48 604 397 239
www: https://www.mixdes.org fax: +48 42 636 0327

THE CITY OF POZNAŃ

Poznań, situated on Warta river, is one of the oldest and largest (around 550 000 inhabitants) cities in western Poland. The city possesses many unique, impressive historical monuments. One of the most precious monuments is the gothic cathedral on Ostrów Tumski island, which is famous for its Golden Chapel and the tombs of the first Polish rulers. Another interesting sight is the Old Market Square with the Town Hall - the pearl of renaissance architecture. This building, with its beautiful facade, arcades and clock with two fighting goats appearing at noon, is a real tourist attraction. One of the most valuable sacral monuments is the baroque Paris Church. Among other interesting sights are Działyński Palace and Royal Castle. For centuries, Poznań has been a very important trade center with its over seventy-yearold Poznań International Fair. In Poznań, as a cultural center, there are Opera and Philharmonic Houses, famous Boy's Choir and several theaters. In the environs of Poznań, there are beautiful Kórnik Castle and Rogalin Palace. More information about Szczecin can be found at the City web page:

https://visitpoznan.pl/en

TOURIST ACTIVITIES

This year's sightseeing tour presents the highlights of Poznań along its main historic route. We will begin with a meeting at the hotel at 14:00. Then we walk through the Imperial District, a prestigious early 20th century area built under Prussian rule, featuring monumental architecture such as the Imperial Castle and Opera House, reflecting diverse European styles.

Next, the group visits Freedom Square, established in the late 18th century as a military parade ground and later transformed into a cultural and civic centre, closely linked to events of the Greater Poland Uprising. The route then leads to the Old Market Square, the historic heart of the city, with the Town Hall - built around 1300 and redesigned in the 16th century - famous for its mechanical goats and ornate façade. Continuing to Przemysł Hill, participants see the Royal Castle and remnants of medieval fortifications, illustrating Poznań's early history. Nearby, the Parish Church (Fara) and former Jesuit College showcase impressive Baroque architecture and the city's academic traditions.

The final part of the walk highlights modern Poznań at Stary Browar and Anders Square, where a former brewery has been transformed into an award winning cultural and commercial space. The tour ends with a return to the hotel.

TRANSPORT

Poznań can be reached by train or road, and you can also use Poznań-Ławica Airport (https://poznanairport.pl/en/) serving connections with many European cities. For all airline passengers, public transport and taxis are available. Bus lines no. 159 and 148 operate between the airport and the city centre. The buses stop at Poznań Główny / Dworzec Zachodni, located close to the hotel. Taxis are also available from outside the terminal. The estimated travel time is 15–20 minutes, and the journey costs up to 40-60 PLN, depending on traffic. App-based services such as Bolt, Uber or FreeNow are also available at the airport. Poznań main railway station ("Poznań Główny") is located within walking distance of the hotel. The conference hotel (Mercure Poznań Centrum) can be reached on foot in approximately 5-10 minutes from the station.

To move around Poznań you can use the public transport (https://www.ztm.poznan.pl). The departure times for the local transport are clearly posted at all stops. Tickets can be purchased in the ticket sales network including Customer Service Points, Ticket Sales Points and stationary ticket machines. Electronic tickets bought in the tram or bus are assigned to your credit card or NFC phone used for payment and are valid for a chosen period after payment. Printed tickets are timed from when validated in the ticket validator inside a tram or a bus. Luggage up to 90 x 75 x 40 cm does not require tickets.

Ticket type	Normal tariff	Reduced fare
Up to 15 minutes	5.00 PLN	2.50 PLN
Up to 45 minutes	7.00 PLN	3.50 PLN
Up to 90 minutes	9.00 PLN	4.50 PLN
24-hour	24.00 PLN	12.00 PLN

There are taxi corporations in Poznań, which may be requested by a phone call, e.g. with the best user ratings:

- Taxi 519 +48 618 519 519
- Multi Taxi +48 538 775 553
- OptiTaxi +48 608 300 500
- Radio Taxi RMI +48 794 222 230
- Super Taxi +48 61 196 22

Alternatives to taxis include the iTaxi, Uber, Bolt or FreeNow apps.

IMPORTANT PHONE NUMBERS

Ambulance	999	Fire Brigade	998
Police	997	Emergency phone	112

PROGRAMME OF THE CONFERENCE

The programme of the MIXDES 2026 Conference will include oral presentations of contributed and invited papers and special sessions. Except for the plenary sessions, the programme of the conference will be divided into parallel sessions, in accordance with discussed topics. The language of the Conference is English, neither translation nor interpretation will be provided.

The time of oral presentations:

- invited papers: 20-25 min. for presentation and 5-10 min. for questions,
- regular papers: 15 min. for presentation and 5 min. for questions.

Lunches:

Lunches will be served each day at the conference center at the times indicated in the programme.

Welcome Party and Conference Banquet:

The Welcome Party will be organised on Thursday (the first conference day) at 19:00. The Conference Banquet and the Closing Ceremony will take place on Friday at 19:00. Both events will take place at the conference center.

BANKING

Foreign exchange facilities are available at major airports and at larger hotels, as well as in many private offices, called “Kantor”. Credit cards can be used in most of the places such as banks, hotels, car-rental offices, restaurants, and shops. Approximate currency exchange rate: 1 € = 4.25 PLN, 1 $ = 3.69 PLN (for the up-to-date information refer to http://www.nbp.pl).

Credit cards:

Visa and MasterCard are the most common cards. However, other cards might be accepted.

Currency:

Generally, everywhere in Poland you pay in Polish zlotys. The currency units are złoty (zł, PLN) and grosz (gr), 1 zł = 100 gr. The Polish zloty is a fully convertible currency internally in Poland.

WEATHER

June in Poland is generally sunny, with some showers, the temperatures can be typically 15 to 28 ˚C during days. During nights, the temperature can go down to 8-10 ˚C. So, we can suggest you to bring summer clothes, with a quite warm jacket or pullover, and an umbrella.

Time — Room A

08:30 Conference Opening
Chairmen: Prof. Wojciech Tylman and Prof. Andrzej Pfitzner

08:40 Plenary Session I
Chairman: Prof. Wojciech Tylman

Digital Education in Engineering Practical Work
T.D. Drysdale (Univ. of Edinburgh, UK)

TSRI Platform for Advanced Packaging and Silicon Photonics - Ecosystem for Industry–Academia–Research Collaboration
C.-N. Liu, H.-H. Tsai (Taiwan Semiconductor Research Inst., Taiwan)

09:40 Vendor Session I
Chairman: Prof. Wojciech Tylman

Challenges in HPC, AI for RISC-V Accelerator Chips
P. Kołodziej (Openchip, Poland)

AI-Driven On-Wafer Measurement: Integrated Probing Solutions from DC to 330 GHz, Silicon Photonics, 1/f and High-Power
A. Lord (Chimera Technology, Czech Republic)

10:40 Coffee Break

11:00 Session 1 (Part 1): Design of Integrated Circuits and Microsystems
Chairman: Prof. Wojciech Tylman

A CMOS Double Balanced Mixer Using Current Bleeding and Negative Impedance Techniques
S. Kumar, H. Shrimali (Indian Inst. of Techn. Mandi, India)

A Multi-PLL Approach to Low-Spur, Low-Jitter Frequency Synthesis for Millimeter-Wave Bands
F. Herzel, N. Maletic, C. Carta, G. Fischer (IHP Frankfurt (Oder), Germany)

An Integrated Phase Noise Generator for Sensitivity Measurements on Superconducting Qubits
F. Herzel, G. Fischer, C. Carta (IHP Frankfurt (Oder), Germany)

13:00 Lunch

14:00 Session 1 (Part 2): Design of Integrated Circuits and Microsystems
Chairman: Prof. Paweł Śniatała

A Sub-300-pW Voltage Reference with -227-dB PSR Using ΔV_{GS} and Multi-Loop Regulation
F. Gagliardi (Univ. of Pisa, Italy), I. Nannipieri, S. Contardi (Univ. of Pisa and Sensichips, Italy), P. Bruschi, M. Piotto, M. Dei (Univ. of Pisa, Italy)

An Active-Passive 2nd-order CTΣΔM Using Single FIR Feedback for Battery Monitoring
P. Peres, N. Paulino (NOVA School of Science and Techn., Portugal), B. Nowacki (Renesas, Portugal)

An Asynchronous Circuit for Pattern Comparison Based on Programmable Gates and Asynchronous Incrementers and Decrementers
M. Kolasa (Bydgoszcz Univ. of Science and Techn., Poland), M. Długosz (Poznan Univ. of Techn., Poland), T. Talaśka (Bydgoszcz Univ. of Science and Techn. and Gdansk Univ. of Techn., Poland), R. Długosz (Bydgoszcz Univ. of Science and Techn. and Aptiv Services, Poland)

Digital Signal Tuning System for MEMS Excitation
P. Wiegand, R. Rieger, A.A. Ahmad, B. Spetzler (Kiel Univ., Germany)

15:20 Coffee Break

15:40 Session 1 (Part 3): Design of Integrated Circuits and Microsystems
Chairman: Prof. Krzysztof Górecki

A 400 fs Resolution Vernier TDC with Adaptive Voltage Scaling
D. Manuel (NOVA School of Science and Techn., Portugal), L. Rodovalho, H. Gonçalves (Synopsys, Portugal), L. Oliveira (NOVA School of Science and Techn., Portugal)

A Design Strategy Based on g_m/I_D Method for Critically Damped Ring Amplifiers
J. Soares, N. Paulino (NOVA School of Science and Techn., Portugal), M. Rodrigues (Renesas, Portugal)

An LDO with 1 A at 1 Ω Load, 3.95 fs of FoM and 70 dB PSRR for TEC Controller Applications
A. Kumar, H. Shrimali (Indian Inst. of Techn. Mandi, India)

Design of a Soft-processor for Educational Purposes
M. Heimowski, P. Buluk, A. Bruździak, J. Komoszewski, B. Pankiewicz (Gdansk Univ. of Techn., Poland)

19:00 Welcome Party

Time **Room B**

11:00 Session 2: Analysis and Modelling of ICs and Microsystemsg
Chairman: Prof. Andrzej Pfitzner

An Overview of the Latest Quantum Technologies and Their Accessibility for Science
P. Duniec, M. Zubert, K. Hałagan (Lodz Univ. of Techn., Poland)

Comparison of BJT and MOSFET Astable Multivibrators: A Theoretical and Simulation Study for Teaching Basic Electronics
P. Pawłowski, A. Dąbrowski (Poznan Univ. of Techn., Poland), R. Długosz (Bydgoszcz Univ. of Science and Techn., Poland)

Comprehensive Harmonic-Domain Simulation of a Thermally-Driven MEMS Accelerometer with Full Noise Characterization
J. Nazdrowicz, M. Szermer (Lodz Univ. of Techn., Poland), M. Tuszyńska (Cracow Univ. of Techn., Poland)

Realisation of Simple Logic Circuits Using a Quantum Processing Unit - A Case Study
M. Zubert, P. Duniec, K. Hałagan (Lodz Univ. of Techn., Poland)

Impact of Data Patterns and Interface Data Rates on DRAM Retention Reliability
J. Warmbier, P. Pawłowski, M. Szymkowiak (Poznan Univ. of Techn., Poland)

13:00 Lunch

14:00 Session 3: Power Electronics
Chairman: Prof. Alexander Kloes

Mapping of Temperature Dependent Heat Transfer Coefficient Values in Power Hybrid Electronic Circuits Cooled by Natural Convection
M. Janicki (Lodz Univ. of Techn., Poland)

Numerical Modeling-Enabled High-Temperature Characterization of Boron Doped Diamond Ohmic Contact and Material Resistivity Using a Simplified TLM Structure
M. Pietrzyk (CEA en Occitanie and LAAS-CNRS, France), D. Trémouilles (LAAS-CNRS, France), E. Marcault (CEA en Occitanie, France), K. Isoird (LAAS-CNRS, France)

Reliability-Oriented TCAD Modelling of Low-Voltage Schottky p-GaN Gate Power HEMT Using $C_{RSS}(V_{DS})$ Curve as a Relevant Trapping Diagnosis
N. Essobai Meftah (LAAS-CNRS, Univ. of Toulouse and CNRS, France), D. Trémouilles (LAAS-CNRS, France), F. Richardeau (Univ. of Toulouse, France)

Tools for Analyzing the Daily Performance of a Photovoltaic Installation Containing Bifacial Modules
A. Urbanowicz, K. Górecki (Gdynia Maritime Univ., Poland)

15:20 Coffee Break

15:40 Session 5: Embedded Systems
Chairman: Dr. Mike Schwarz

Evolution of Photonic Infrastructure in the IOWN Concept: Architecture, Experimental Results, and Real-Time Applications
J. Nazdrowicz (Lodz Univ. of Techn. and Fujitsu, Poland), S. Siminski (Fujitsu, Poland)

PCB Modeled by a Lossy Three-Conductor Transmission Line
G. Angelov (Tech. Univ. of Sofia, Bulgaria)

Reliability Analysis of SAN Topologies under Variable Workloads Using Hybrid Simulation Techniques
J. Nazdrowicz (Lodz Univ. of Techn. and Fujitsu, Poland), M. Tuszyńska (Cracow Univ. of Techn., Poland)

Study of the Ethernet-APL Communication Standard: A New Revolution for Industrial Automation
M.S. Moreira (Federal Univ. of Itajubá, Brazil), A.B. Lugli (National Inst. of Telecommunications, Brazil), T. Pimenta (Federal Univ. of Itajubá, Brazil), J.A.P. Azevedo (National Inst. of Telecommunications, Brazil)

19:00 Welcome Party

Time **Room C**

11:00 Special Session 3: Open-source Silicon Ecosystem
Chairman: Dr. Władysław Grabiński

OpenPDK as a Strategic FOSS IC Design Enabler
W. Grabiński, K. Herman, S. Andreev, R. Scholz (IHP Frankfurt (Oder), Germany)

Teaching Integrated Circuit Design with Open Source Electronic Design Automation Tools and Open Process Design Kits
P. Mierzwiński, B. Dec (Warsaw Univ. of Techn., Poland)

Architectural Evaluation of Iterative and Unrolled AES-128 in 45 nm Using an Open-Source Flow
D. Santos, J. Cabacinho (NOVA School of Science and Techn., Portugal), J. Casaleiro (Lisbon School of Engineering, Portugal), L. Oliveira (NOVA School of Science and Techn., Portugal)

Broadening Participation in Open-Source Integrated Circuit Design and Fabrication Through IEEE Activities
J.S. Moya (International Iberian Nanotechnology Laboratory, Portugal)

Analysis of the Behavior of a Memristive Device within a One-Transistor-One-Resistor Structure
N. Dersch (THM Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), T. Rizzi, M. Uhlmann, E. Perez-Bosch Quesada, K. Dorai Swamy Reddy (IHP Frankfurt (Oder), Germany), E. Perez, C. Wenger (IHP Frankfurt (Oder) and Brandenburg Univ. of Techn. Cottbus-Senftenberg, Germany), M. Schwarz (THM Univ. of Applied Sciences, Germany), B. Iniguez (Univ. Rovira i Virgili, Spain), A. Kloes (THM Univ. of Applied Sciences, Germany)

13:00 Lunch

14:00 Special Session 2: FAMES Pilot Line Highlights - Current Developments in FD SOI PDK and RRAM Applications
Chairman: Prof. Witold Pleskacz

A Pathfinding PDK Toward 10nm FD-SOI Technology
O. Billoint, M. Alepidis, Y. Andee, K. Azizi-Mourier, A. Boujnah, P. Chausse, H. Chazot-Ranquet, J.-F. Christmann, O. Cueto, E. De-Foucauld, H. Jacquinot, J. Lacord, G. Largiller, D. Ly, Y. Maneglia, M. Mouhdach, A.-A. Ndiaye, O. Rozeau, A. Vaysset, T. Poiroux (Univ. Grenoble Alpes, France)

RRAM Physical Unclonable Functions: Compact Modeling, Array Design, and Optimal Control Schemes for Security Applications
K. Ber (CEZAMAT and Warsaw Univ. of Techn., Poland), P. Wiśniewski (CEZAMAT, Poland), P. Jeżak (CEZAMAT and Warsaw Univ. of Techn., Poland), A. Małkowski, M. Jarosik (CEZAMAT, Poland), A. Pawłowski, J. Ślubowski, K. Sobolewski (CEZAMAT and Warsaw Univ. of Techn., Poland), T. Borejko, W. Pleskacz (Warsaw Univ. of Techn., Poland)

A Low-area, Digitally Controlled Low Dropout Regulator with Calibration Logic Optimized for RRAM Control
J. Ślubowski, A. Pawłowski, K. Sobolewski, K. Ber (CEZAMAT and Warsaw Univ. of Techn., Poland), P. Wiśniewski (CEZAMAT, Poland), T. Borejko, W. Pleskacz (Warsaw Univ. of Techn., Poland)

A Low Power, Low Area, Current Sampling Based Sense Amplifier Optimized for RRAM Readout Logic
A. Pawłowski, J. Ślubowski, K. Sobolewski, K. Ber (CEZAMAT and Warsaw Univ. of Techn., Poland), P. Wiśniewski (CEZAMAT, Poland), T. Borejko, W. Pleskacz (Warsaw Univ. of Techn., Poland)

15:20 Coffee Break

15:40 Session 7: Medical Applications
Chairman: Prof. Marcin Janicki

A Low-Power Low-Offset DAC-Less LC-ADC for Biomedical Signal Acquisition
F. Modarresi (Islamic Azad Univ., Iran), A. Amini (Univ. of Pavia, Italy)

A Low-Power Compact HV TX/RX Switch Composed of Three HV-MOS Transistors for Ultrasound Imaging Front-End ASICs
A. Amini (Univ. of Pavia, Italy)

Comparison of EWT and OVMD Techniques for Left and Right Hand Motor Imagery Classification in EEG Signals
P. Zych, P. Śniatała (Poznan Univ. of Techn., Poland)

Design of a Neurorehabilitation System for Patients with Parkinson's Disease, with a Focus on Therapy outside the Clinical Setting
M. Fechner (Poznan Univ. of Techn., Poland), E. Kozielewska-Zwierska, A. Krawczyński (Poznan Univ. of Medical Sciences, Poland)

Fast-Recovery Capacitive ECG Front-End Based on Reverse-Connected Zener Diodes
Z. Sajadi, R. Rieger (Kiel Univ., Germany)

19:00 Welcome Party

Time — Room A

08:30 Plenary Session II
Chairman: Prof. Andrzej Pfitzner

Photonic Integration for Optical Interconnect and Sensing Applications
S.-L. Lee, Y.-H. Chung (National Taiwan Univ. of Science and Techn. and HiSiPIC Research Center, Taiwan), V. Prajzler, V. Jerabek, D. Mares (Czech Tech. Univ. in Prague, Czech Republic)

09:00 Vendor Session II
Chairman: Prof. Andrzej Pfitzner

From Cloud to Edge: The Rise of Intelligent, Distributed AI Systems
M. Zmuda (Intel, Poland)

09:20 Session 1 (Part 4): Design of Integrated Circuits and Microsystems
Chairman: Prof. Witold Pleskacz

Implementation of a Universal IP CORDIC Algorithm in Serial and Parallel Architectures
I. Cintra, G. Piedade, L. Pires, N. Souza, R. Macedo, M. Morais, C. Cunha, L. Souza, E. Pereira, F. Rocha, F. Portelinha (National Inst. of Telecommunications, Brazil), T. Pimenta (Federal Univ. of Itajuba, Brazil)

IP Release and Cross-Foundry Design Migration for 3D-MRAM Technology
Q. Zhu (International Technological Univ., USA)

Low-Voltage Low-Power Current-Mode Squaring and Multiplier/Divider Circuits
C.R. Popa (National Univ. of Science and Techn. Politehnica, Romania)

Memory Cost Analysis for Sequential Logic Locking FSMLock
J. Evans, M. Łukowiak (Rochester Inst. of Techn., USA)

10:40 Coffee Break

11:10 Session 1 (Part 5): Design of Integrated Circuits and Microsystems
Chairman: Prof. Krzysztof Górecki

Low Power Low Phase Noise Stacked Quadrature Ring Oscillator
D. Novais, J. Santa-Rita, L. Oliveira, J. Oliveira, H. Serra (NOVA School of Science and Techn., Portugal), J. Casaleiro (Lisbon School of Engineering, Portugal)

QoE-Aware Switch Architecture for MPEG-2 Transport Stream Digital TV Broadcast
M. Albuquerque, M. Santos, E. Lima (National Inst. of Telecommunications, Brazil), J. Oliveira Filho (Cadence, Brazil), E. Pereira, L. Souza, F. Rocha, F. Portelinha Junior (National Inst. of Telecommunications, Brazil), T. Pimenta (Federal Univ. of Itajuba, Brazil)

RC Time-Constant Calibration Scheme Using a DPLL
J.P. Carvalho, N. Paulino (NOVA School of Science and Techn., Portugal), B. Nowacki (Renesas, Portugal)

Single-ended to Differential Mode Voltage-to-Current and Current-to-Voltage Converter in High Voltage SOI Technology
M. Jankowski (Lodz Univ. of Techn., Poland)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony & Conference Banquet

Time **Room B**

09:20 **Session 4: Signal Processing**
Chairman: Prof. Tomasz Talaśka

Analysis of Multivariate Industrial Process Data for Quality Pattern Detection in Masterbatch Coloring
L. Hisgen (THM Univ. of Applied Sciences, Germany and Univ. Rovira i Virgili, Spain), T. Kubik (THM Univ. of Applied Sciences, Germany), S. Garbe (G.E. Habich's Söhne GmbH, Germany), J. Fischer (superus Datenmanagement GmbH, Germany), A. Kloes (THM Univ. of Applied Sciences, Germany), B. Iniguez (Univ. Rovira i Virgili, Spain), M. Schwarz (THM Univ. of Applied Sciences, Germany)

Envelope Identification Method for Guitar Amplifier Modelling with Wiener-Hammerstein Models
T. Fernandes, N. Paulino (NOVA School of Science and Techn., Portugal)

One Crossbar, Two Functions: Analogue Image Obfuscation and Feature Extraction via Memristors
P. Janiszyn (SEMIQA and Wroclaw Univ. of Science and Techn., Poland), A. Wąsiak-Maciejak, P. Sitarz, T. Matusiak (SEMIQA, Poland)

Readout Board for the CBM Silicon Tracking System: Design Constraints, Powering Concept and Functional Validation
P. Semeniuk (GSI Helmholtzzentrum für Schwerionenforschung GmbH and Goethe Univ. Frankfurt, Germany and AGH University of Krakow, Poland), J. Lehnert, R. Kapell (GSI Helmholtzzentrum für Schwerionenforschung GmbH, Germany)

10:40 **Coffee Break**

11:10 **Session 7: Artificial Intelligence in Electronic Systems**
Chairman: Prof. Tomasz Stefański

Application of Large-Scale Foundation Models and Multimodal Fusion for Stress Detection in Glider Pilots under Real-World Flight Conditions
A. Wolszczak (Poznan Univ. of Techn., Poland), M. De Marsico (Sapienza Univ. of Rome, Italy)

Design of a Gaussian Activation Function Generator for Neural Network Applications
C.R. Popa (National Univ. of Science and Techn. Politehnica, Romania)

Hardware Implementation of a Bfloat16 Exponential Function for Softmax Computation
R. Feiglewicz, A. Kos (AGH Univ. of Krakow, Poland)

ML-Based Error Mitigation Approach for Overcoming NISQ Hardware Constraints in Fermionic Nanoelectronic Simulations
M. Przygocki, R. Kotas, M. Zubert (Lodz Univ. of Techn., Poland)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony

Time **Room C**

09:20 Special Session 1 (Part 1): Advances in Smart Electronics for AI and Future Technologies

Chairman: Prof. Chih-Wen Lu

A 30 μW 2.4-GHz LNA With 5.6 dB NF Exploiting Trifilar Transformer Coupling for Smart AIoT Electronics
K.-C. Tai, K.-W. Cheng (National Cheng Kung Univ., Taiwan)

A Nonlinear OTA Simulation Model for the Design of a Switched-Capacitor DSM
C.-Y. Yao, J.-Y. Wu (National Taiwan Univ. of Science and Techn., Taiwan)

Charge-Modulated Conductance and Synaptic Behavior in Access-Region WSe_2/h-BN/Gr van der Waals Floating-Gate Transistors for Nonvolatile Memory
S.-P. Lin (National Yang Ming Chiao Tung Univ. and National Chung Hsing Univ., Taiwan)

Leveraging Semiconductor Eco-systems to MEMS
W. Fang (National Tsing Hua Univ., Taiwan)

10:40 Coffee Break

11:10 Special Session 1 (Part 1): Advances in Smart Electronics for AI and Future Technologies

Chairman: Prof. Chia-Yu Yao

MEMS-PMU Co-Simulation of an Electrostatic Energy Harvesting Interface for Battery-Free IoT Devices
Y.-Y. Huang (National Yang Ming Chiao Tung Univ., Taiwan), M. Babka, J. Luci, V. Janicek (Czech Tech. Univ. in Prague, Czech Republic), Y.-T. Liao (National Yang Ming Chiao Tung Univ., Taiwan), P.-H. Hsieh (National Tsing Hua Univ., Taiwan), P.-H. Chen (National Yang Ming Chiao Tung Univ., Taiwan)

Review of High-PPI Micro-LED Display Drivers with Current-Mode PWM and Compact Pixel Circuits for Near-Eye Applications
C.-W. Lu, T.-H. Lo (National Tsing Hua Univ., Taiwan)

Secure IoT Platform with Advanced Key Generation and Robust Cybersecurity
L.-Y. Chiou, Z.-F. Chen, J.Q. Choy, H.-Y. Chen, C.-Y. Chang, Y.-Y. Shen (National Cheng Kung Univ., Taiwan), R. Holý, M. Vaniš, M. Šrotýř (Czech Tech. Univ. in Prague, Czech Republic)

Simulation Analysis of a ±180° Phase Shifter Circuit Model
C.-K. Lin, D.-B. Lin (National Taiwan Univ. of Science and Techn., Taiwan)

Time Room D

09:20 Tutorial

Considerations on the Design of Resilient 2.5-3D Heterogeneous, Multilayer Interposer Systems for Chip Lifecycle Management
F. Vargas (IHP Frankfurt (Oder), Germany)

10:00 IEEE EDS Poland Meeting

10:40 Coffee Break

11:00 Special Session 4: UAV as a Platform for Various Applications
Chairman: Prof. Paweł Śniatała

Enhancing UAV Data Security Using Lightweight Cryptography Module
S. Baliński, P. Śniatała, M. Sobieraj (Poznan Univ. of Techn., Poland), J. Xie (San Diego State Univ., USA)

P4-Programmable Raspberry Pi Nodes for Multi-Interface Edge Networking in Networked Airborne Computing
J. Piechocka, J. Grzelski, M. Żal (Poznan Univ. of Techn., Poland)

Topology-Aware Offloading of DAG Tasks for Multi-UAV-Assisted Mobile Edge Computing
K. Ma, J. Xie, S. Ren (San Diego State Univ., USA), P. Śniatała (Poznan Univ. of Techn., USA)

Towards Autonomous Detection and Hot Patching of Binary Vulnerabilities in UAV Software
I. Stopochkina, M. Ilin, O. Novikov, A. Voitsekhovskyi (Igor Sikorsky Kyiv Polytechnic Inst., Ukraine)

13:00 Lunch

14:00 Tourist Activities

19:00 Closing Ceremony

Poznań City Center Map